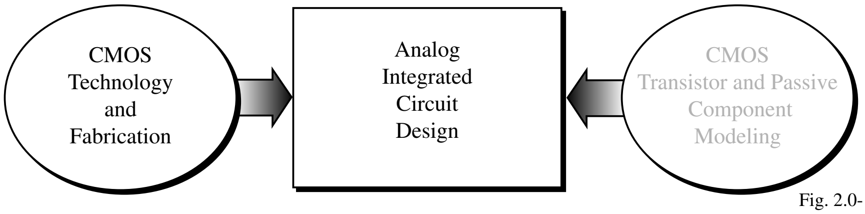
CHAPTER 2 - CMOS TECHNOLOGY

Chapter Outline

2.1 Basic MOS Semiconductor Fabrication Processes
2.2 CMOS Technology
2.3 PN Junction
2.4 MOS Transistor
2.5 Passive Components
2.6 Other Considerations of CMOS Technology
2.7 Bipolar Transistor (optional)
2.8 BiCMOS Technology (optional)

Perspective



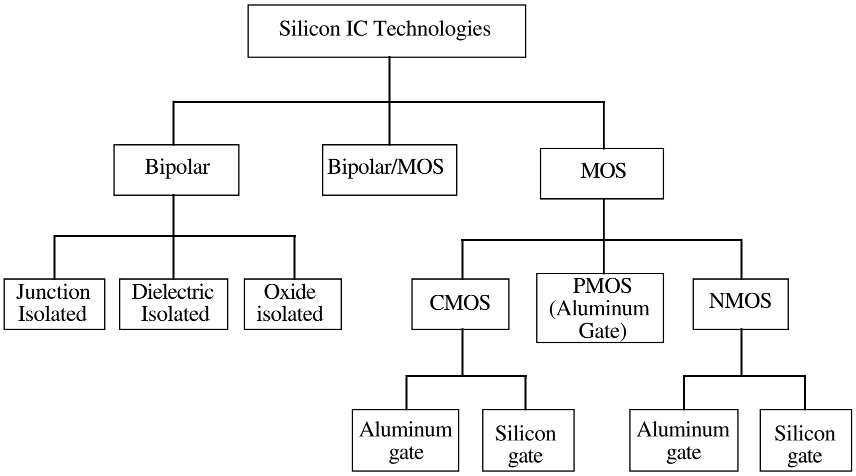
CMOS Technology and Fabrication

Analog Integrated Circuit Design

CMOS Transistor and Passive Component Modeling

Fig. 2.0-1

Classification of Silicon Technology



Silicon IC Technologies

Bipolar

Bipolar/MOS

MOS

Junction Isolated

Dielectric Isolated

Oxide isolated

CMOS

PMOS (Aluminum Gate)

NMOS

Aluminum gate

Silicon gate

Aluminum gate

Silicon gate

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz (0.25μm)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor Implementation	Voltage dependent	Reasonably good

Therefore,

- Almost every comparison favors the BJT, *however* a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

Other factors:

- The potential for technology improvement for CMOS is greater than for BJT
- Performance generally increases with decreasing channel length

SECTION 2.1 - BASIC MOS SEMICONDUCTOR PROCESSES

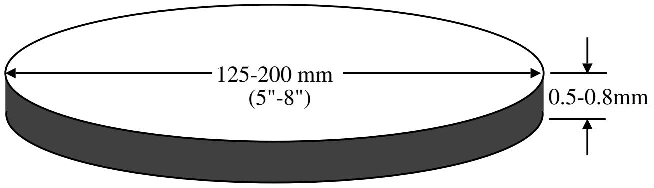
Basic steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon wafer



n-type: 3-5 Ω-cm
p-type: 14-16 Ω-cm

Fig. 2.1-1r

Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

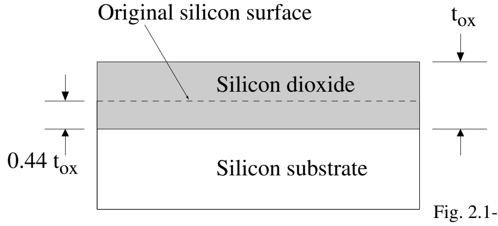


Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.

Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

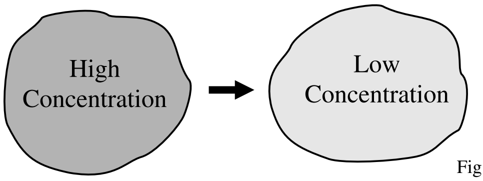
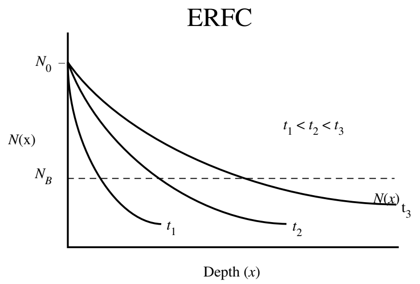
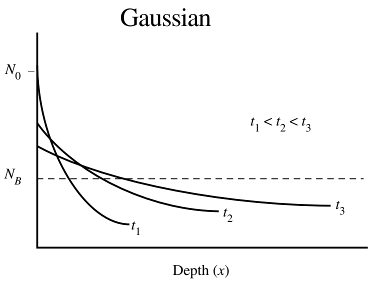


Fig. 2.1-3

Diffusion is typically done at high temperatures: 800 to 1400°C



(a) Infinite source of impurities at the surface.



(b) a finite source of impurities at the surface.)

Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

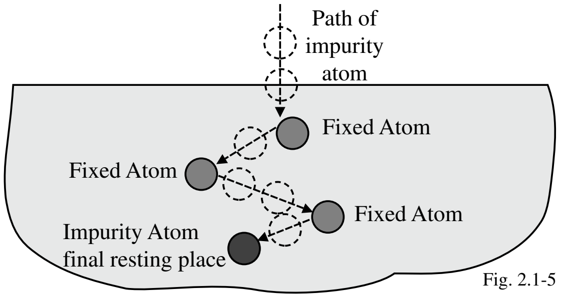


Fig. 2.1-5

- Anneal is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.

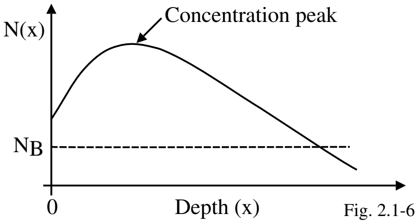


Fig. 2.1-6

Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Material that is being deposited using these techniques cover the entire wafer.

Etching

Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer

Important considerations:

- *Anisotropy* of the etch is defined as,

  A = 1-(lateral etch rate/vertical etch rate)

- *Selectivity* of the etch (film to mask and film to substrate) is defined as,

$$S_{\text{film-mask}} = \frac{\text{film etch rate}}{\text{mask etch rate}}$$

A = 1 and $S_{\text{film-mask}} = \infty$ are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

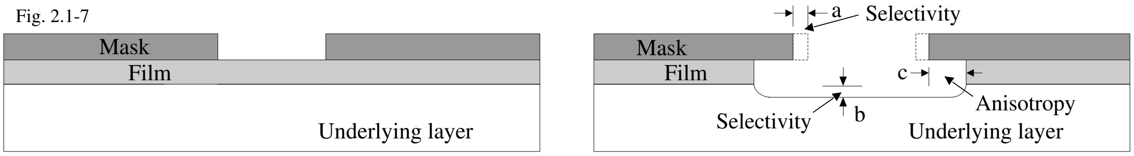


Fig. 2.1-7

(a) Portion of the top layer ready for etching. (b) Horizontal etching and etching of underlying layer.

Epitaxy

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even oppositely, of the material on which it grown
- It accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

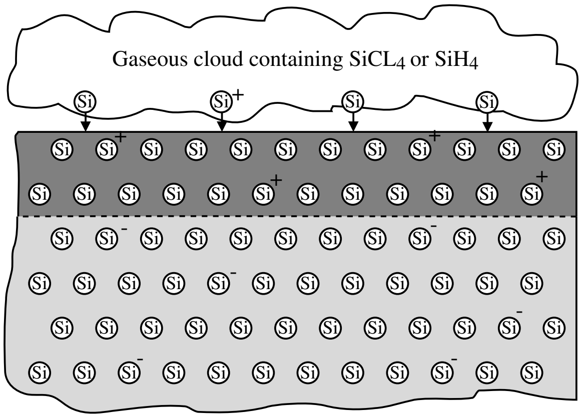


Fig. 2.1-7.5

Photolithography

Components

- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist

Areas exposed to UV light are soluble in the developer

Negative photoresist

Areas not exposed to UV light are soluble in the developer

Steps

1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake (≈ 100°C)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photomask is called *printing*.

Types of printing include:

- Contact printing
- Proximity printing
- Projection printing

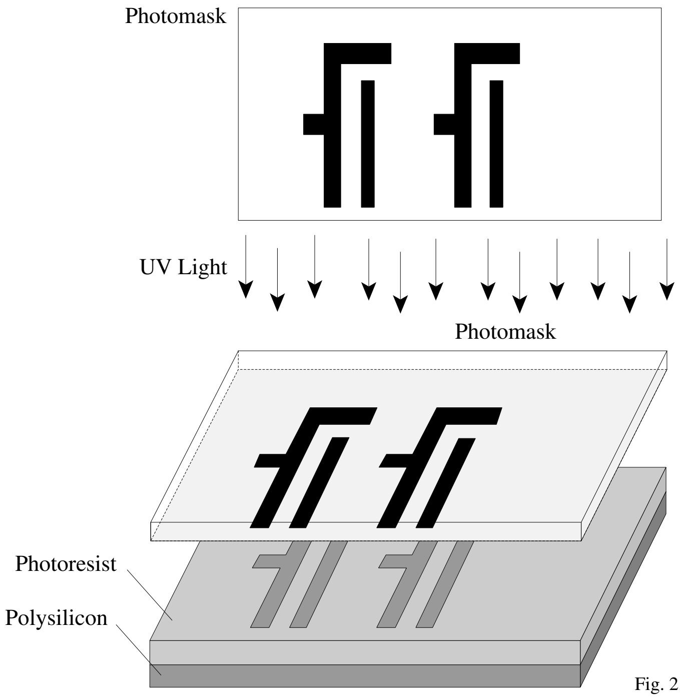


Fig. 2.1-8

Illustration of Photolithography - Positive Photoresist

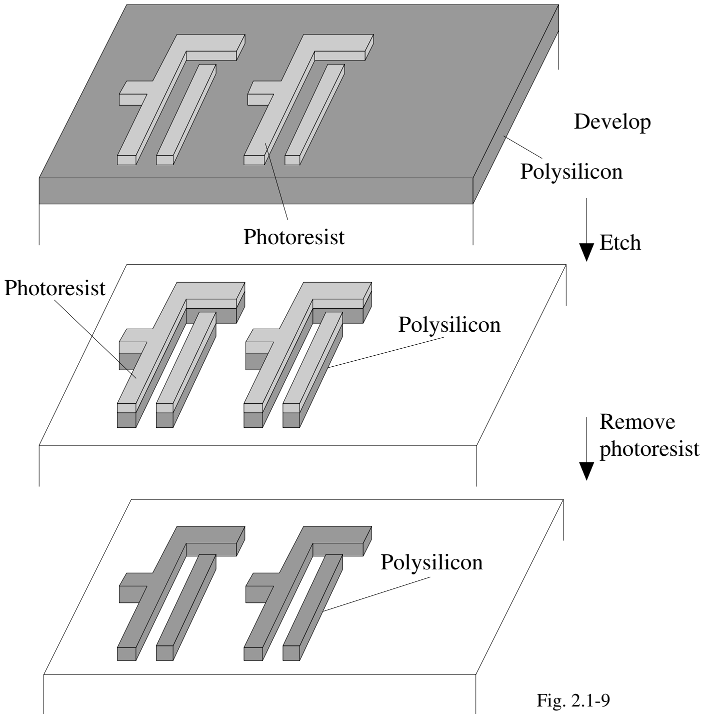


Fig. 2.1-9

Illustration of Photolithography - Negative Photoresist

(Not used much any more)

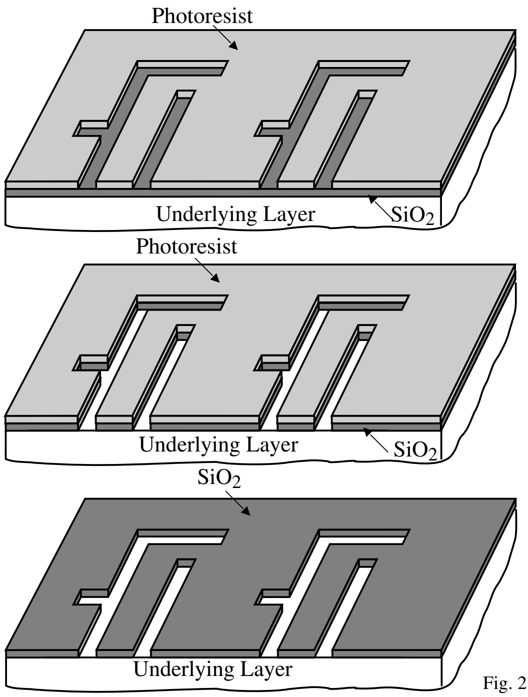


Fig. 2.1-10

SECTION 2.2 - CMOS TECHNOLOGY

Fabrication

Fabrication involves the implementation of semiconductor processes to build a MOSFET transistor and compatible passive components as an integrated circuit.

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias and deposit second level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

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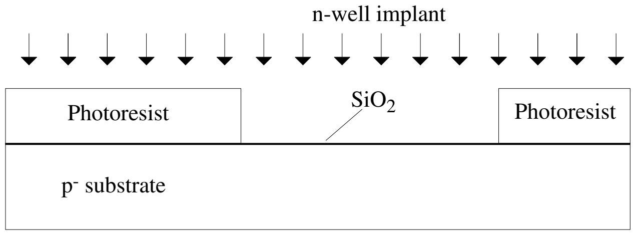
Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride

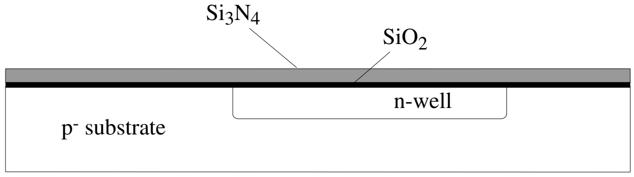
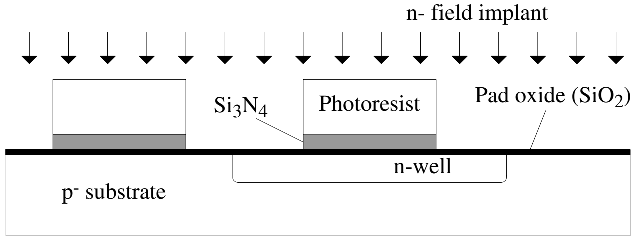


Fig. 2.2-1

Major CMOS Process Steps - Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop

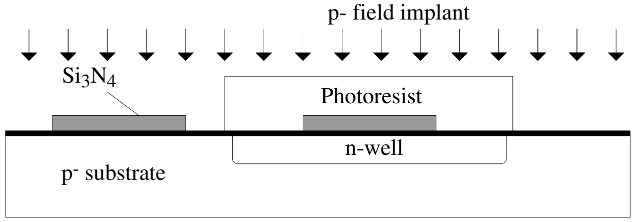


Fig. 2.2-2

Major CMOS Process Steps - Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)

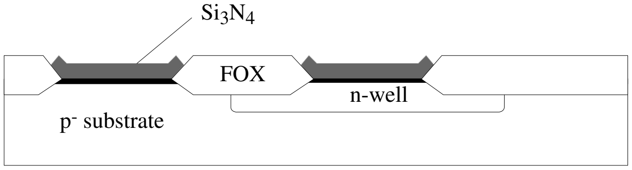


Fig. 2.2-3A

After removing the Si_3N_4, threshold adjustments can be made to balance the V_T's.

- Increase the V_{TN} from near zero to 0.5-0.6V (dope the p-substrate heavier)
- Increase the V_{TP} from around –1.5V to –0.5-0.6V (dope the n-substrate lighter)

Step 6.) Growth of the gate thin oxide and deposition of polysilicon

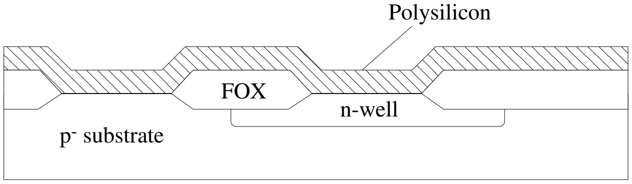
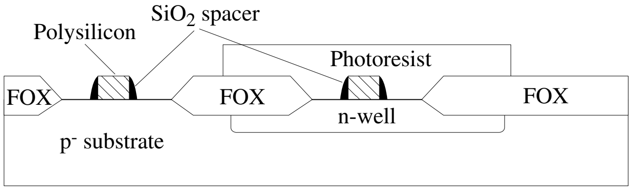


Fig. 2.2-3B

Major CMOS Process Steps - Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)

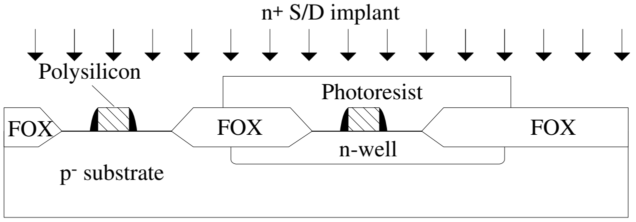
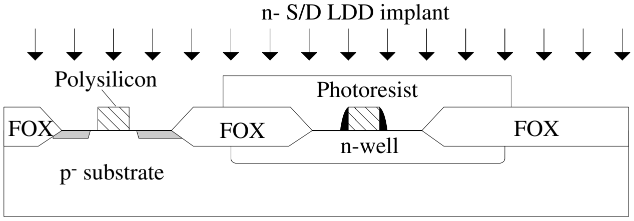


Fig. 2.2-4

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p$^-$ substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

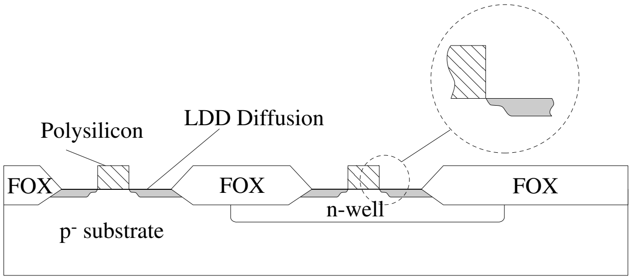
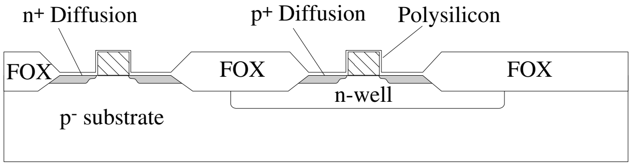


Fig. 2.2-5

Major CMOS Process Steps - Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

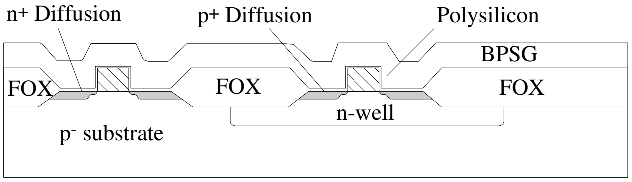
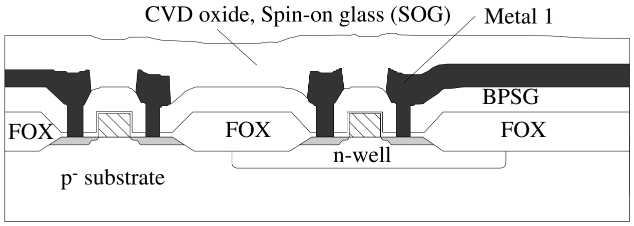


Fig. 2.2-6

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metall

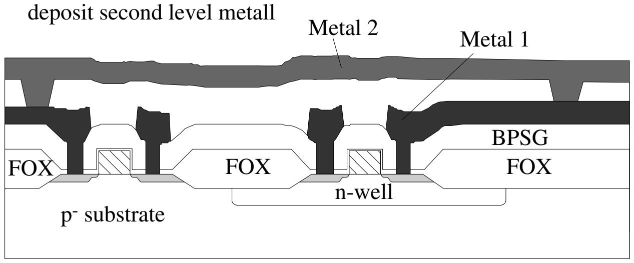


Fig. 2.2-7

Major CMOS Process Steps - Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

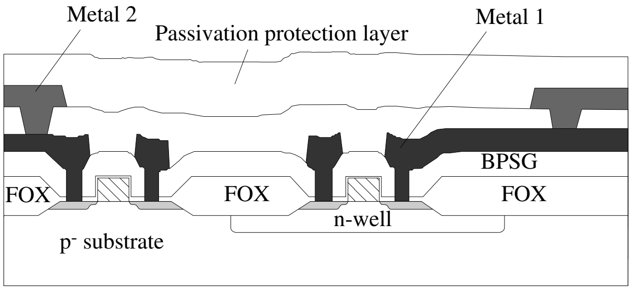


Fig. 2.2-8

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

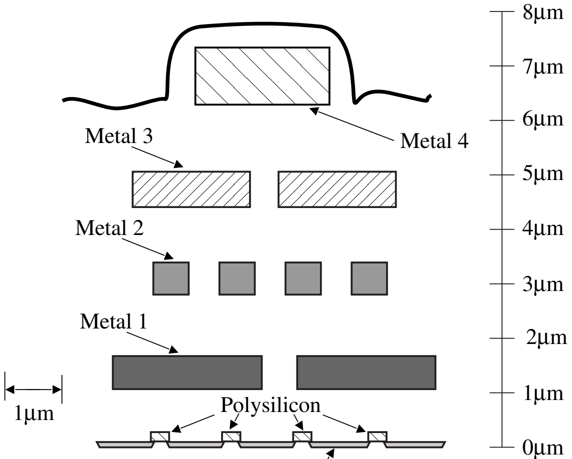
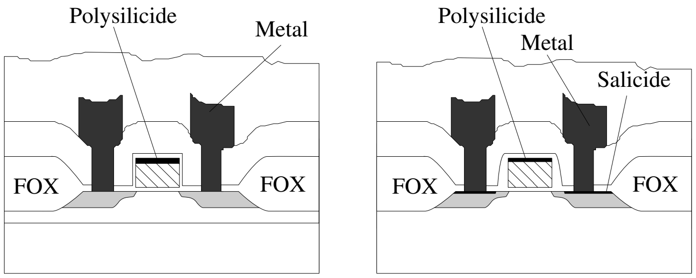


Figure 2.2-9A

Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

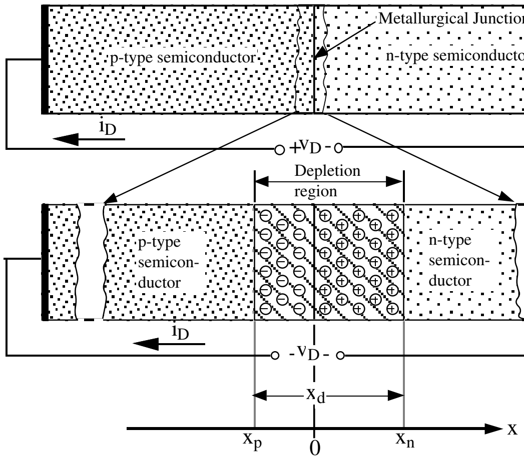
Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure Salicide structure Fig2.2-10

SECTION 2.3 - THE PN JUNCTION

Concept

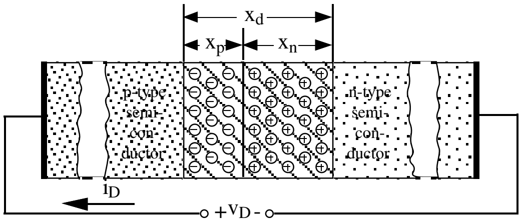


1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:

$$\boxed{\text{Current due to diffusion} = \text{Current due to electric field}}$$

PN Junction Characterization

Cross section of an ideal pn junction:



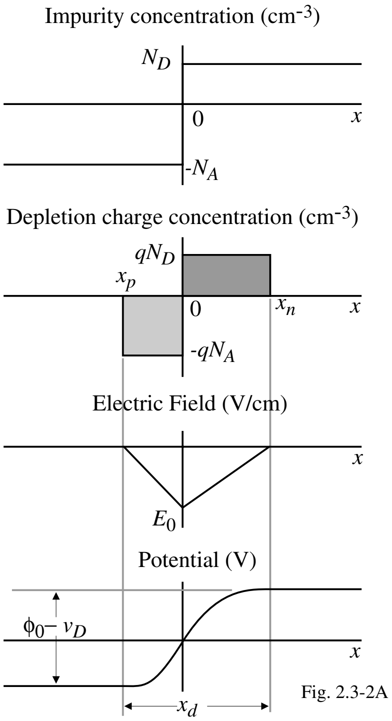


Fig. 2.3-2A

Summary of PN Junction Analysis

Barrier potential-

$$\phi_o = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = V_t \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Depletion region widths-

$$\left.\begin{aligned} x_n = W_2 &= \sqrt{\frac{2\varepsilon_{si}(\psi_o - v_D)N_A}{qN_D(N_A+N_D)}} \\ x_p = W_1 &= -\sqrt{\frac{2\varepsilon_{si}(\psi_o - v_D)N_D}{qN_A(N_A+N_D)}} \end{aligned}\right\} \qquad x \propto \sqrt{\frac{1}{N}}$$

Depletion capacitance-

$$C_j = A\sqrt{\frac{\varepsilon_{si} q N_A N_D}{2(N_A+N_D)}}\ \frac{1}{\sqrt{\phi_o - v_D}} = \frac{C_{j0}}{\sqrt{1 - \frac{v_D}{\phi_o}}}$$

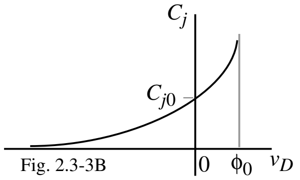


Fig. 2.3-3B

Breakdown voltage-

$$BV = \frac{\varepsilon_{si}(N_A+N_D)}{2qN_AN_D}\ E_{max}^2 \propto \frac{1}{N}$$

Summary of PN Junction Analysis - Continued

Graded junction:

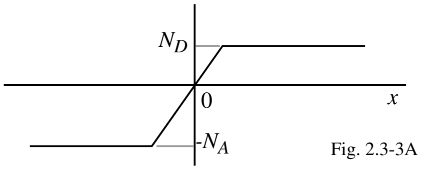


Fig. 2.3-3A

Above expressions become:

Depletion region widths-

$$\left.\begin{aligned} x_n = W_2 &= \left(\frac{2\varepsilon_{si}(\phi_o - v_D)N_A}{qN_D(N_A+N_D)}\right)^m \\ x_p = W_1 &= -\left(\frac{2\varepsilon_{si}(\phi_o - v_D)N_D}{qN_A(N_A+N_D)}\right)^m \end{aligned}\right\} \quad x \propto \left(\frac{1}{N}\right)^m$$

Depletion capacitance-

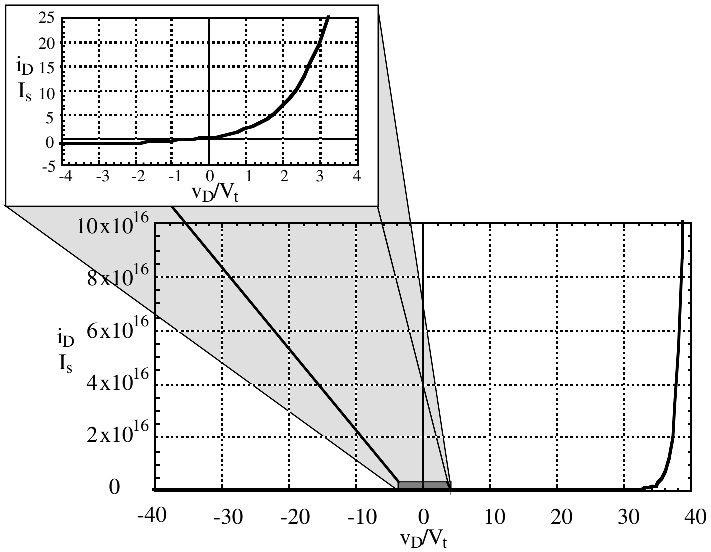
$$C_j = A\left(\frac{\varepsilon_{si} q N_A N_D}{2(N_A+N_D)}\right)^m \frac{1}{(\phi_o - v_D)^m} = \frac{C_{j0}}{\left(1 - \frac{v_D}{\phi_o}\right)^m}$$

where $0.33 \leq m \leq 0.5$.

Summary of PN Junction Analysis - Continued

Current-Voltage Relationship-

$$i_D = I_s\left[\exp\left(\frac{v_D}{V_t}\right) - 1\right] \quad \text{where} \quad I_s = qA\left[\frac{D_p p_{no}}{L_p} + \frac{D_n n_{po}}{L_n}\right] \approx \frac{qAD}{L}\frac{n_i^2}{N} = KT^3\exp\left(\frac{-V_{GO}}{V_t}\right)$$



Metal-Semiconductor Junctions

Ohmic Junctions: A pn junction formed by a highly doped semiconductor and metal.

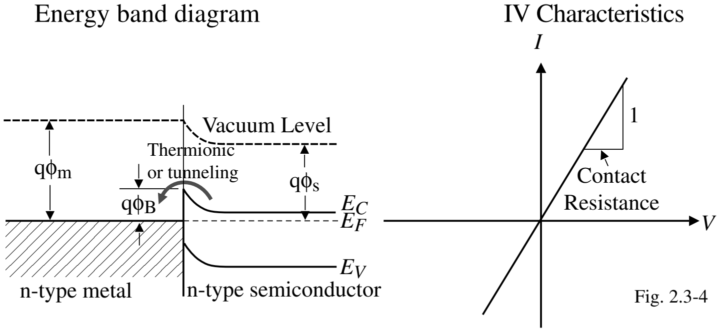


Fig. 2.3-4

Schottky Junctions: A pn junction formed by a lightly doped semiconductor and metal.

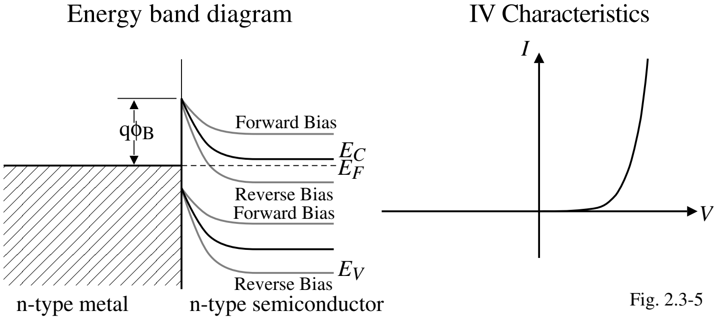


Fig. 2.3-5

SECTION 2.4 - THE MOS TRANSISTOR

Physical Structure of the n-channel and p-channel transistor in an n-well technology

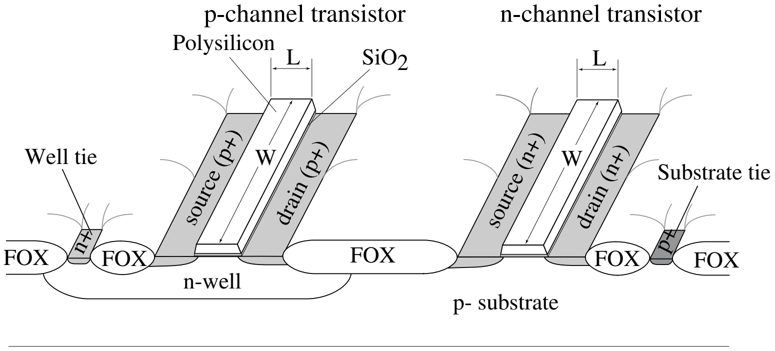


Fig. 2.4-1

How does the transistor work?

Consider the enhancement n-channel MOSFET:

When the gate is made positive with respect to the substrate a depletion region is formed beneath the gate resulting from holes being pushed away from the silicon-silicon dioxide interface.

When the gate voltage is sufficiently large (0.5-0.7V), the region beneath the gate inverts and a n-channel is formed between the source and drain.

The MOSFET Threshold Voltage

When the gate voltage reaches a value called the *threshold voltage* (V_T), the substrate beneath the gate becomes inverted (it changes from p-type to n-type).

$$V_T = \phi_{MS} + \left(-2\phi_F - \frac{Q_b}{C_{ox}}\right) + \left(\frac{-Q_{SS}}{C_{ox}}\right)$$

where

$\phi_{MS} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$

ϕ_F = Equilibrium electrostatic potential (Femi potential)

$$\phi_F(\text{PMOS}) = -\frac{kT}{q}\, ln(N_A/n_i) = -V_t\, ln(N_A/n_i)$$

$$\phi_F(\text{NMOS}) = \frac{kT}{q}\, ln(N_D/n_i) = V_t\, ln(N_D/n_i)$$

$$Q_b \approx \sqrt{2q\mathrm{N}_A\varepsilon_{si}(|-2\phi_F + v_{SB}|)}$$

Q_{SS} = undesired positive charge present in the interface between the oxide and the bulk silicon

Rewriting the threshold voltage expression gives,

$$V_T = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \qquad \text{and} \qquad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Signs for the Quantities in the Threshold Voltage Expression

Parameter	N-Channel	P-Channel
Substrate	p-type	n-type
ϕ_{MS}		
Metal	−	−
n^+ Si Gate	−	−
p^+ Si Gate	+	+
ϕ_F	−	+
Q_{b0},Q_b	−	+
Q_{ss}	+	+
V_{SB}	+	−
γ	+	−

Example 2.4-1 Calculation of the Threshold Voltage

Find the threshold voltage and body factor γ for an n-channel transistor with an n$^+$ silicon gate if t_{ox} = 200 Å, $N_A = 3 \times 10^{16}$ cm^{-3}, gate doping, $N_D = 4 \times 10^{19}$ cm^{-3}, and if the positively-charged ions at the oxide-silicon interface per area is 10^{10} cm^{-2}.

Solution

From above, ϕ_F(substrate) is given as

$$\phi_F(\text{substrate}) = -0.0259 \ln\left[\frac{3\times 10^{16}}{1.45 \times 10^{10}}\right] = -0.377 \text{ V}$$

The equilibrium electrostatic potential for the n$^+$ polysilicon gate is found from as

$$\phi_F(\text{gate}) = 0.0259 \ln\left[\frac{4 \times 10^{19}}{1.45 \times 10^{10}}\right] = 0.563 \text{ V}$$

Therefore, the potential ϕ_{MS} is found to be

$$\phi_F(\text{substrate}) - \phi_F(\text{gate}) = -0.940 \text{ V}.$$

The oxide capacitance is given as

$$C_{ox} = \varepsilon_{ox}/t_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{200 \times 10^{-8}} = 1.727 \times 10^{-7} \text{ F/cm}^2$$

The fixed charge in the depletion region, Q_{b0}, is given as

$$Q_{b0} = -\,[2 \times 1.6 \times 10^{-19} \times 11.7 \times 8.854 \times 10^{-14} \times 2 \times 0.377 \times 3 \times 10^{16}]^{1/2} = -\,8.66 \times 10^{-8} \text{ C/cm}^2.$$

Example 2.4-1 - Continued

Dividing Q_{b0} by C_{ox} gives -0.501 V. Finally, Q_{ss}/C_{ox} is given as

$$\frac{Q_{SS}}{C_{ox}} = \frac{10^{10} \cdot 1.60 \cdot 10^{-19}}{1.727 \cdot 10^{-7}} = 9.3 \cdot 10^{-3} \text{ V}$$

Substituting these values for V_{T0} gives

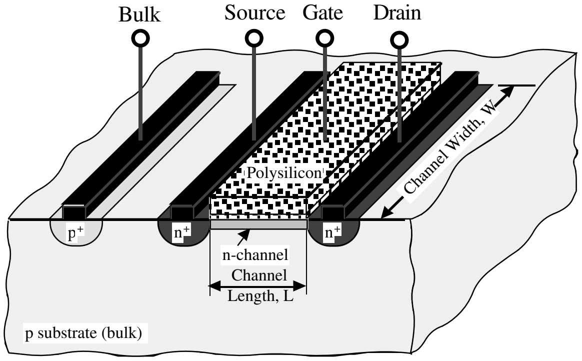
$$V_{T0} = -\,0.940 + 0.754 + 0.501 - 9.3 \text{ x } 10^{-3} = 0.306 \text{ V}$$

The body factor is found as

$$\gamma = \frac{\left[2 \cdot 1.6 \cdot 10^{-19} \cdot 11.7 \cdot 8.854 \cdot 10^{-14} \cdot 3 \cdot 10^{16}\right]^{1/2}}{1.727 \cdot 10^{-7}} = 0.577 \quad \text{V}^{1/2}$$

Depletion Mode MOSFET

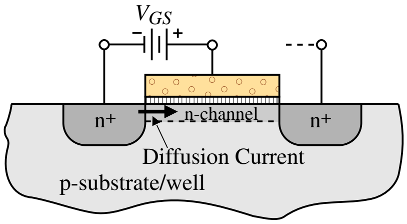
The channel is diffused into the substrate so that a channel exists between the source and drain with no external gate potential.



The threshold voltage for a depletion mode NMOS transistor will be negative (a negative gate potential is necessary to attract enough holes underneath the gate to cause this region to invert to p-type material).

Weak Inversion Operation

Weak inversion operation occurs when the applied gate voltage is below V_T and pertains to when the surface of the substrate beneath the gate is weakly inverted.



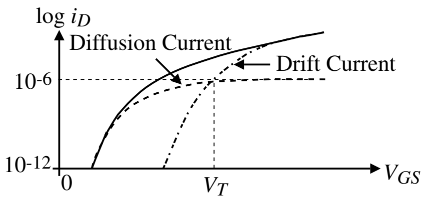
Regions of operation according to the surface potential, ϕ_S.

$\phi_S < \phi_F$: Substrate not inverted

$\phi_F < \phi_S < 2\phi_F$: Channel is weakly inverted (diffusion current)

$2\phi_F < \phi_S$: Strong inversion (drift current)

Drift current versus diffusion current in a MOSFET:



SECTION 2.5 PASSIVE COMPONENTS COMPATIBLE WITH CMOS TECHNOLOGY

CAPACITORS

Types of Capacitors Considered

- pn junction capacitors
- Standard MOS capacitors
- Accumulation mode MOS capacitors
- Poly-poly capacitors
- Metal-metal capacitors

Characterization of Capacitors[†]

- C is the desired capacitance
- Dissipation of a capacitor

$$Q = \omega C R_p$$

Where R_p is the equivalent parallel resistance associated with the capacitor, C

- A varactor is a variable capacitor
- C_{max}/C_{min} ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a varactor.
- Parasitic capacitors are the capacitors to ac ground from both terminals of the desired capacitance.

[†] E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001

PN Junction Capacitors

Generally made by diffusion into the well.

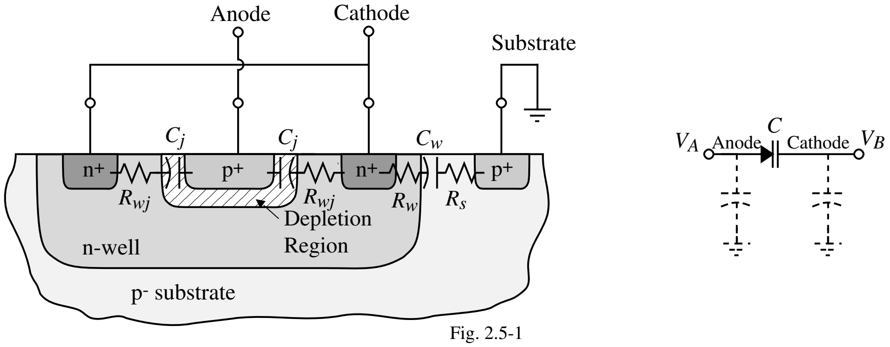


Fig. 2.5-1

Layout:

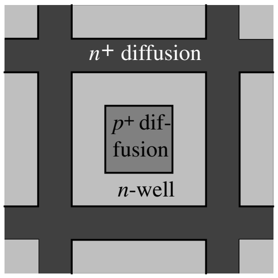


Fig. 2.5-1A

Minimize the distance between the p^+ and n^+ diffusions.

Two different versions have been tested.

1.) Large islands – 9µm on a side

2.) Small islands – 1.2µm on a side

PN-Junction Capacitors – Continued

It can be shown that the anode should be the floating node and the cathode must be connected to ac ground.

Experimental data (Q at 2GHz, 0.5µm CMOS):

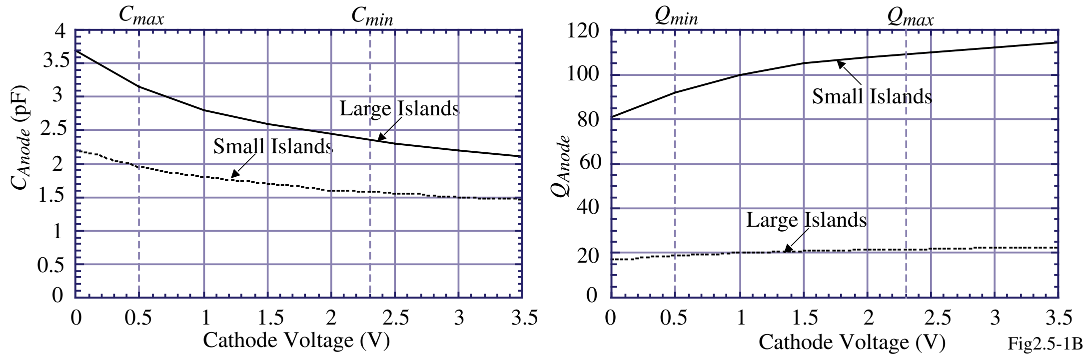


Fig2.5-1B

Summary:

Terminal Under Test	Small Islands (598 1.2µm x1.2µm islands)			Large Islands (42 9µm x 9µm islands)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

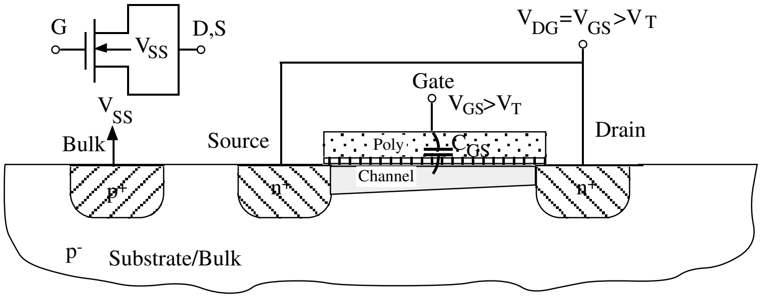
Electrons as majority carriers lead to higher Q because of their higher mobility.

Also, the resistance, R_{wj}, is reduced in the small islands compared with the large islands giving higher Q.

Standard MOS Capacitors

Polysilicon-Oxide-Channel for Enhancement MOSFETs

Bulk connected to V_{SS}



Comments:

- The capacitance variation is achieved by changing the mode of operation from depletion (minimum capacitance) to inversion (maximum capacitance).
- Capacitance = $C_{GS} \approx C_{ox}W{\cdot}L$
- Channel must be formed, therefore $V_{GS} > V_T$
- With $V_{GS} > V_T$ and $V_{DS} = 0$, the transistor is in the active region.
- LDD transistors will give lower Q because of the increase of series resistance.

Standard MOS Capacitors - Continued

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35μm CMOS)

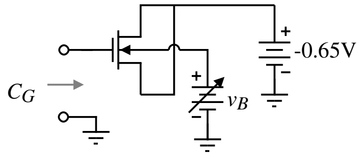
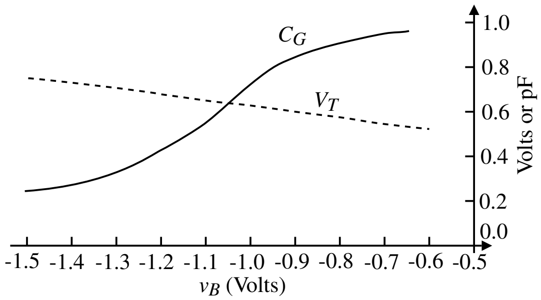


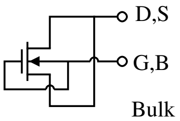
Fig. 2.5-3



$C_{max}/C_{min} \approx 4$

Standard MOS Capacitors - Continued

Bulk connected to Source-Drain



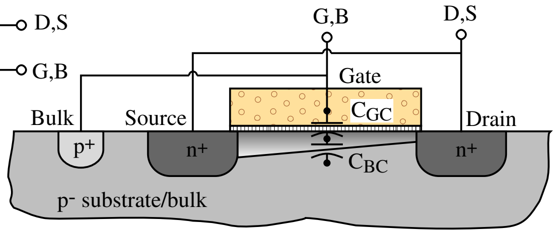
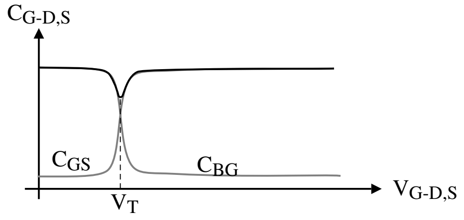


Fig. 2.0-035



$C_{G\text{-}D,S} = C_{GS} + C_{GB}$

Comments:

- Capacitance is more constant as a function of $V_{G\text{-}D,S}$
- Still not a good capacitor for large voltage swings
- Increased parasitics from the gate/bulk terminal

Standard Mode NMOS Varactor – Continued

More Detail - Includes the LDD transistor

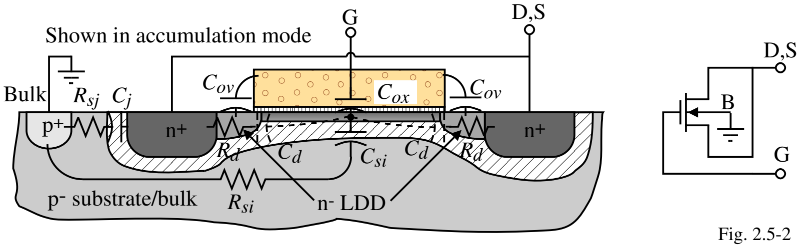


Fig. 2.5-2

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

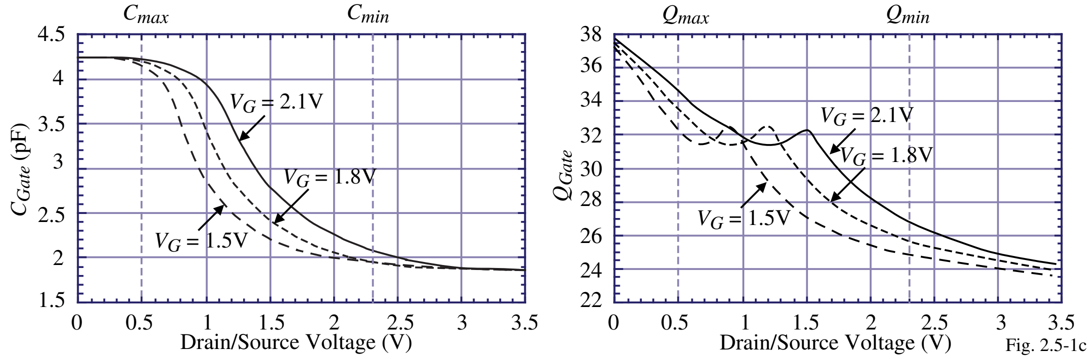


Fig. 2.5-1c

V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

MOS Capacitors - Continued

Accumulation-Mode Capacitor[†] [††]

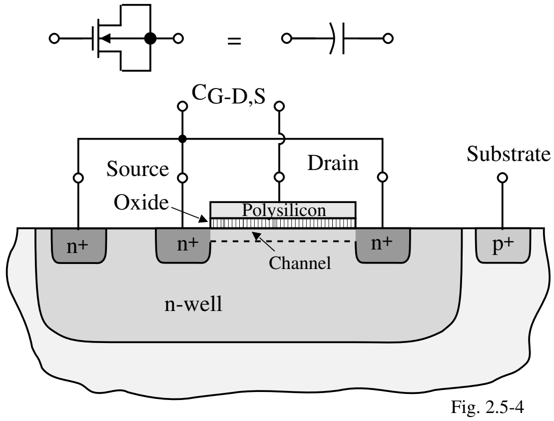


Fig. 2.5-4

Comments:

- Again, the capacitor variation is achieved by moving from the depletion (min. C) to accumulation (max. C)
- ±30% tuning range
- $Q \approx 25$ for 3.1pF at 1.8 GHz (optimization leads to Qs of 200 or greater)

[†] T. Soorapanth, et. al., "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 32-33, 1998.

[††] R. Castello, et. al., "A ±30% Tuning Range Varactor Compatible with future Scaled Technologies," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 34-35, 1998.

Accumulation Capacitor – More Detail

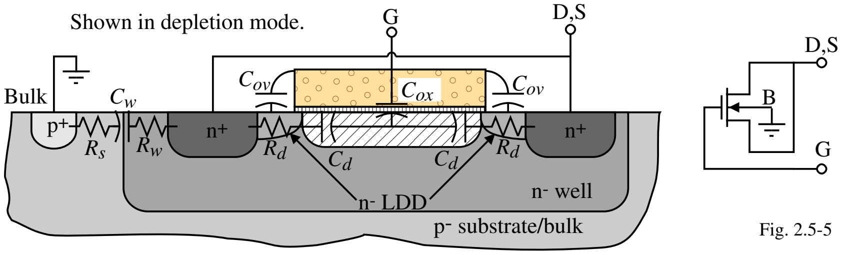


Fig. 2.5-5

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

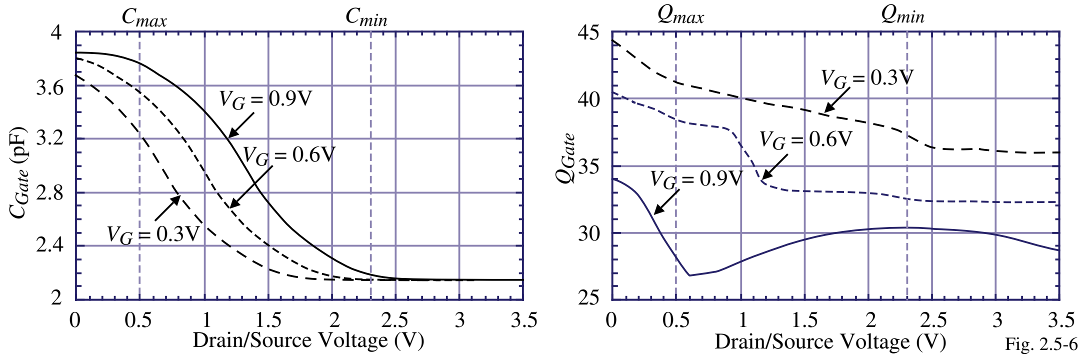
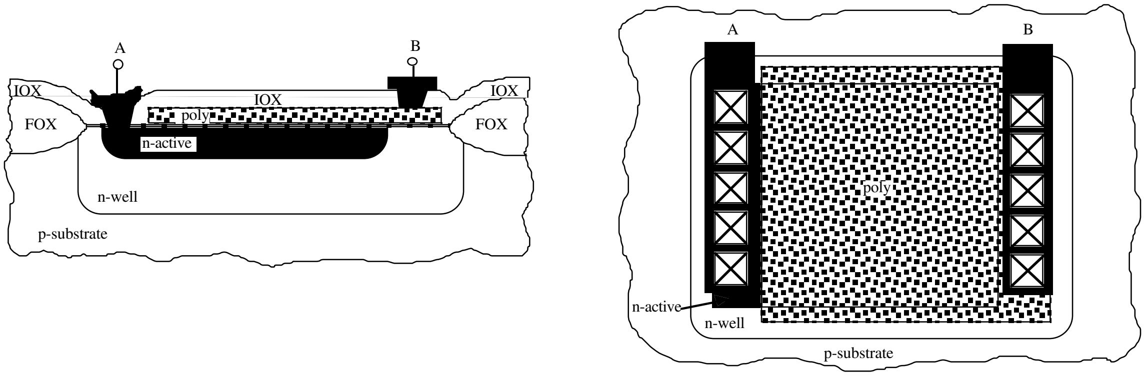


Fig. 2.5-6

$V_G = 0.6$V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

MOS Capacitors - Continued

Polysilicon-Oxide Diffusion/Active for Enhanced MOSFETs



Unit capacitance ≈ 1.2 fF/µm^2

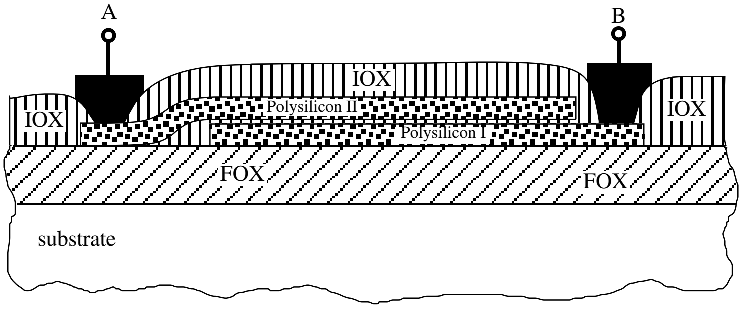
Voltage dependence:

$C(V) \approx C(0) + a_1V + a_2V^2$, where $a_1 \approx 0$ and $a_2 \approx 210$ ppm/V^2

(Not as good linearity as poly-poly capacitors)

MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly)

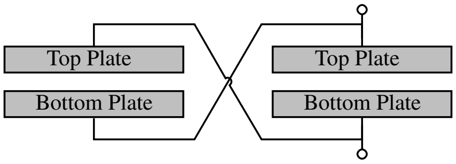


Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Possible approach for increasing the voltage linearity:



Implementation of Capacitors using Available Interconnect Layers

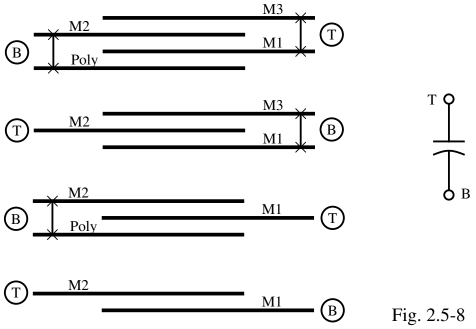
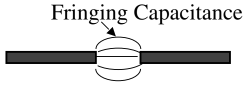


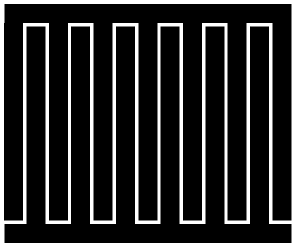
Fig. 2.5-8

Fringing (Fractal) Capacitors

Capacitance between conductors on the same level and use lateral flux..



Top View of a Lateral Flux Capacitor



PC10

These capacitors are called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

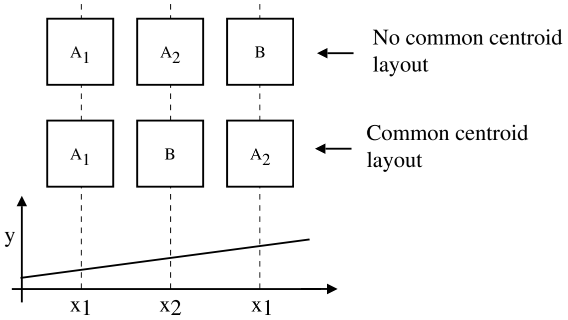
In certain cases, the capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

Capacitor Errors

1.) Oxide gradients
2.) Edge effects
3.) Parasitics
4.) Voltage dependence
5.) Temperature dependence

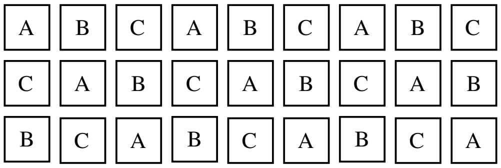
Capacitor Errors - Oxide Gradients

Error due to a variation in oxide thickness across the wafer.



Only good for one-dimensional errors.

An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.



A	B	C	A	B	C	A	B	C
C	A	B	C	A	B	C	A	B
B	C	A	B	C	A	B	C	A

0.2% matching of poly resistors was achieved using an array of 50 unit resistors.

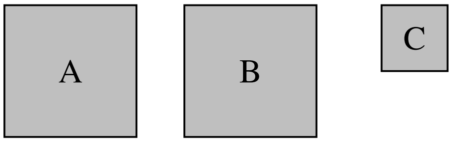
Capacitor Errors - Edge Effects

There will always be a randomness on the definition of the edge.

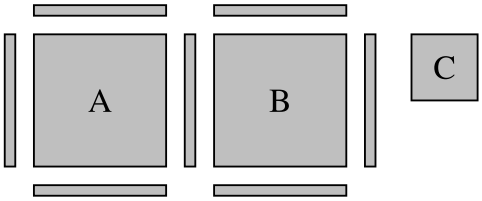
However, etching can be influenced by the presence of adjacent structures.

For example,

Matching of A and B are disturbed by the presence of C.



Improved matching achieve by matching the surroundings of A and B.



Capacitor Errors - Area/Periphery Ratio

The best match between two structures occurs when their area-to-periphery ratios are identical.

Let $C'_1 = C_1 \pm \Delta C_1$ and $C'_2 = C_2 \pm \Delta C_2$

where

C' = the actual capacitance

C = the desired capacitance (which is proportional to *area*)

ΔC = edge uncertainty (which is proportional to the *periphery*)

Solve for the ratio of C'_2/C'_1,

$$\frac{C'_2}{C'_1} = \frac{C_2 \pm \Delta C_2}{C_1 \pm \Delta C_1} = \frac{C_2}{C_1}\left(\frac{1 \pm \frac{\Delta C_2}{C_2}}{1 \pm \frac{\Delta C_1}{C_1}}\right)$$

$$\approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2}\right)\left(1 \mp \frac{\Delta C_1}{C_1}\right) \approx \frac{C_2}{C_1}\left(1 \pm \frac{\Delta C_2}{C_2} \mp \frac{\Delta C_1}{C_1}\right)$$

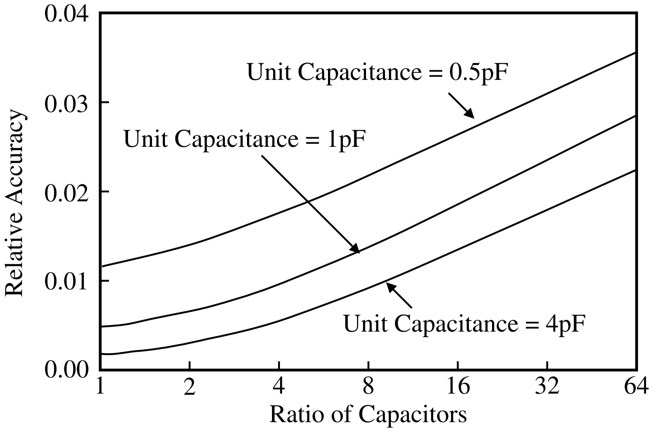
If $\frac{\Delta C_2}{C_2} = \frac{\Delta C_1}{C_1}$, then $\boxed{\frac{C'_2}{C'_1} = \frac{C_2}{C_1}}$

Therefore, the best matching results are obtained when the area/periphery ratio of C_2 is equal to the area/periphery ratio of C_1.

Capacitor Errors - Relative Accuracy

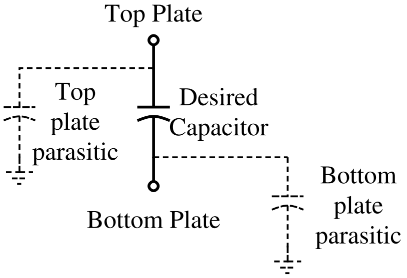
Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,



Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

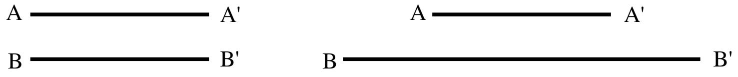


Top plate parasitic is 0.01 to 0.001 of $C_{desired}$

Bottom plate parasitic is 0.05 to 0.2 $C_{desired}$

Other Considerations on Capacitor Accuracy

Decreasing Sensitivity to Edge Variation:



Sensitive to edge variation in both upper andlower plates

Sensitive to edge varation in upper plate only.

Fig. 2.6-13

A structure that minimizes the ratio of perimeter to area (circle is best).

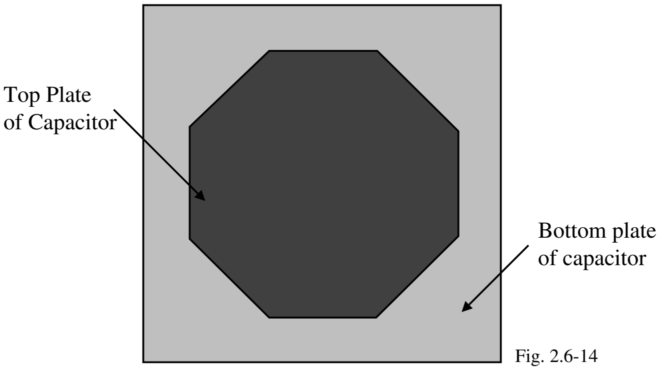


Fig. 2.6-14

Capacitor Errors - Temperature and Voltage Dependence

Polysilicon-Oxide-Semiconductor Capacitors

Absolute accuracy ≈ ±10%

Relative accuracy ≈ ±0.2%

Temperature coefficient ≈ +25 ppm/C°

Voltage coefficient ≈ -50ppm/V

Polysilicon-Oxide-Polysilicon Capacitors

Absolute accuracy ≈ ±10%

Relative accuracy ≈ ±0.2%

Temperature coefficient ≈ +25 ppm/C°

Voltage coefficient ≈ -20ppm/V

Accuracies depend upon the size of the capacitors.

RESISTORS

MOS Resistors - Source/Drain Resistor

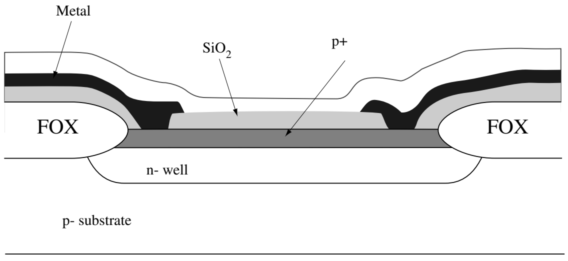


Fig. 2.5-16

Diffusion:

10-100 ohms/square

Absolute accuracy = ±35%

Relative accuracy = 2% (5 µm), 0.2% (50 µm)

Temperature coefficient = +1500 ppm/°C

Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square

Absolute accuracy = ±15%

Relative accuracy = 2% (5 µm), 0.15% (50 µm)

Temperature coefficient = +400 ppm/°C

Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

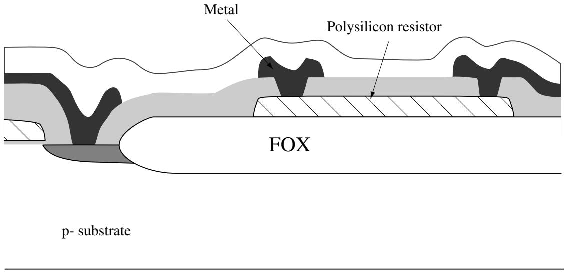


Fig. 2.5-17

30-100 ohms/square (unshielded)

100-500 ohms/square (shielded)

Absolute accuracy = ±30%

Relative accuracy = 2% (5 µm)

Temperature coefficient = 500-1000 ppm/°C

Voltage coefficient ≈ 100 ppm/V

Comments:

- Used for fuzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor

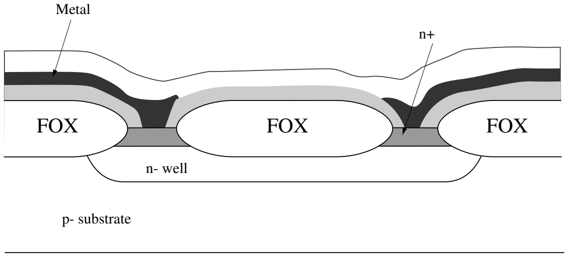


Fig. 2.5-18

1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

MOS Passive Component Performance Summary

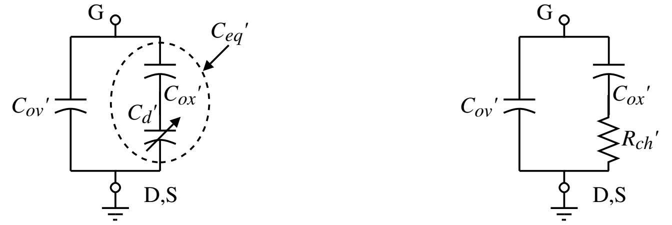
Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semiconductor Capacitor	0.35-0.5 fF/μm^2	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm^2	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

Future Technology Impact on Passive RC Components

What will be the impact of down scaling in CMOS technology?

- Resistors – probably little impact
- Capacitors – a different story

Consider the following simplified equivalent circuits of the MOS capacitors (PN junction C_{max}/C_{min} too small):



Depletion Mode MOS Varactor Inversion and accumulation mode MOS Varactor

Fig. 2.5-7

The primed components represent the capacitance and resistance per unit gate width (W).

$\therefore\ C' = C/W$ and $R' = R/W$

1.) Depletion mode NMOS capacitance.

$$C_G' = C_{OV}' + \frac{C_{ox}' \cdot C_d'}{C_{ox}' + C_d'} = C_{OV}' + C_{eq}'$$ where C_{OV}' is the gate overlap and fringing capacitance

2.) Inversion mode NMOS capacitance and depletion mode accumulation NMOS capacitance.

$$C_{G,max}' = C_{OV}' + C_{eq,max}' = C_{OV}' + C_{ox}'$$

Future Technology Impact on Passive RC Components – Continued

What is the influence of scaling on C_{max}/C_{min} and Q?

1.) The C_{max}/C_{min} ratio becomes,

$$\frac{C_{G,max}'}{C_{G,min}'} = \frac{C_{OV}' + C_{ox}'}{C_{OV}' + C_{eq,min}'}$$

We note that $C_{ox}' \propto \dfrac{l}{t_{ox}}$ = constant and $C_{OV}' \propto \dfrac{1}{t_{ox}} = \dfrac{1}{l}$

$$\therefore \quad \frac{C_{G,max}'}{C_{G,min}'} \rightarrow \frac{C_{OV}'}{C_{OV}'} = 1 \text{ as } l \rightarrow 0 \qquad \Rightarrow \qquad \boxed{\frac{C_{max}}{C_{min}} \text{ decreases as the channel length decreases}}$$

2.) Influence of channel scaling on Q.

R_{ch}' represents the main contribution to the losses and therefore determines Q

$$R_{ch}' \propto \text{Gate length, } l \quad \Rightarrow \quad R_{ch}' \text{ decreases as } l \text{ decreases} \quad \Rightarrow \quad \boxed{Q \text{ increases as } l \text{ decreases}}$$

Best capacitor for future scaled CMOS?

The standard mode CMOS depeletion capacitor because C_{max}/C_{min} is larger than that for the accumulation mode and Q should be sufficient.

INDUCTORS

Inductors

What is the range of values for on-chip inductors?

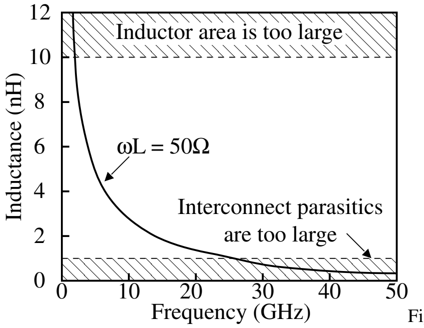


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi\cdot 10^9)^2 \cdot 5\text{x}10^{-12}} = 5\text{nH}$$

Note: Off-chip connections will result in inductance as well.

Candidates for inductors in CMOS technology are:

1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

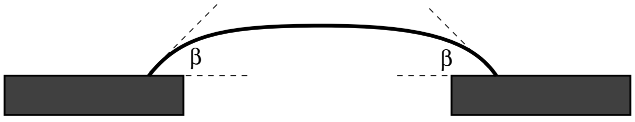


Fig.6-6

- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors

Spiral Inductors on a Lossy Substrate:

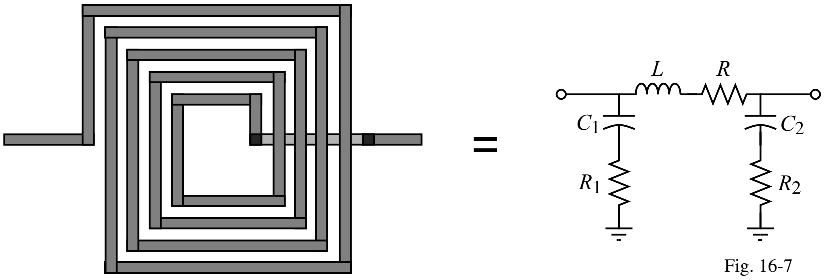


Fig. 16-7

- Design Parameters:

  Inductance, $L = \Sigma(L_{self} + L_{mutual})$

  Quality factor, $Q = \dfrac{\omega L}{R}$

  Self-resonant frequency: $f_{self} = \dfrac{1}{\sqrt{LC}}$

- Trade-off exists between the Q and self-resonant frequency
- Typical values are L = 1-8nH and Q = 3-6 at 2GHz

Planar Spiral Inductors - Continued

Inductor Design

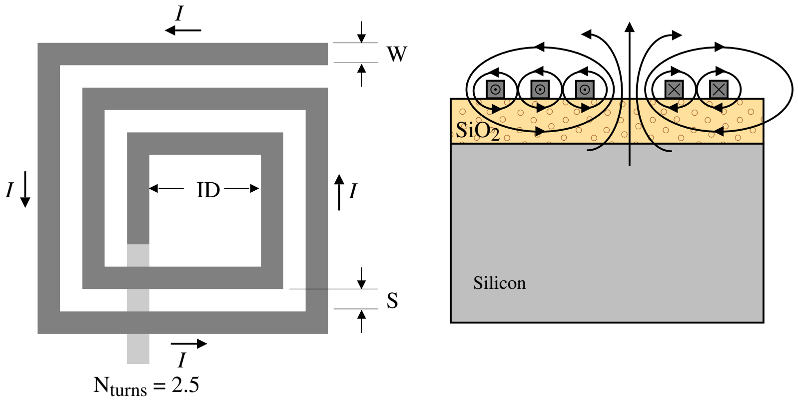


Fig. 6-9

Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Planar Spiral Inductors - Continued

Influence of a Lossy Substrate

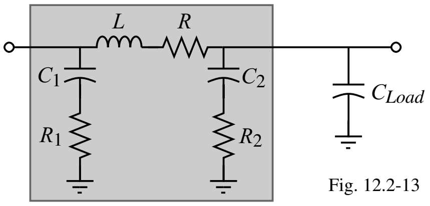


Fig. 12.2-13

where:

L is the desired inductance

R is the series resistance

C_1 and C_2 are the capacitance from the inductor to the ground plane

R_1 and R_2 are the eddy current losses in the silicon

Guidelines for using spiral inductors on chip:

- Lossy substrate degrades Q at frequencies close to f_{self}
- To achieve an inductor, one must select frequencies less than f_{self}
- The Q of the capacitors associated with the inductor should be very high

Planar Spiral Inductors - Continued

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and furtherest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example:

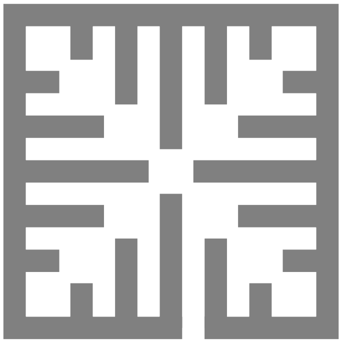


Fig. 6-10

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance)

Solenoid Inductors

Example:

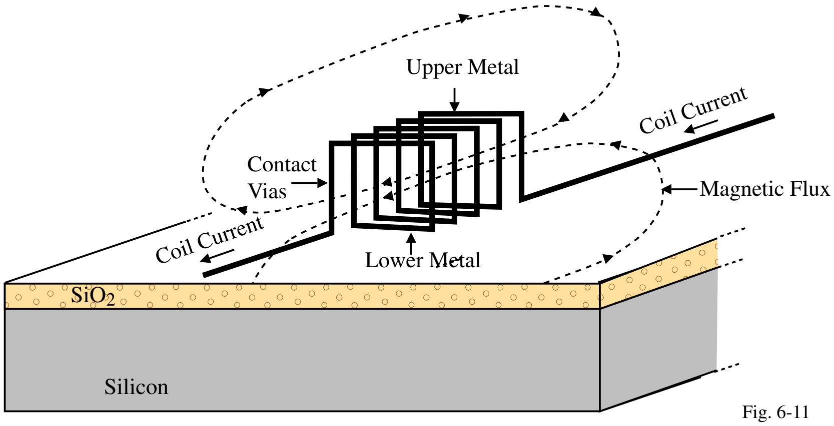


Fig. 6-11

Comments:

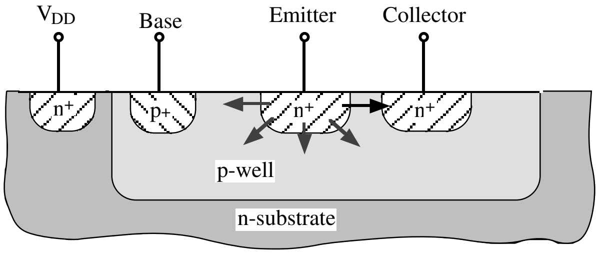
- Magnetic flux is small due to planar structure
- Capacitive coupling to substrate is still present
- Potentially best with a ferromagnetic core

SECTION 2.6 - OTHER CONSIDERATIONS OF CMOS TECHNOLOGY

Lateral Bipolar Junction Transistor

P-Well Process

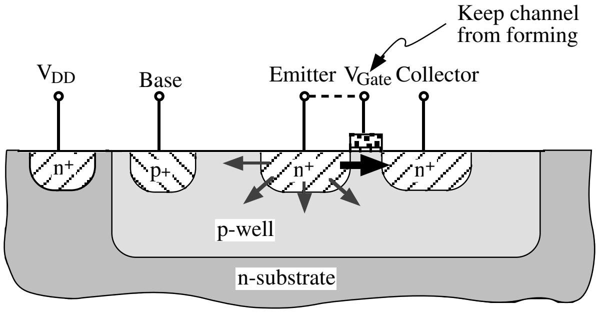
NPN Lateral-



Lateral Bipolar Junction Transistor - Continued

Field-aided Lateral-

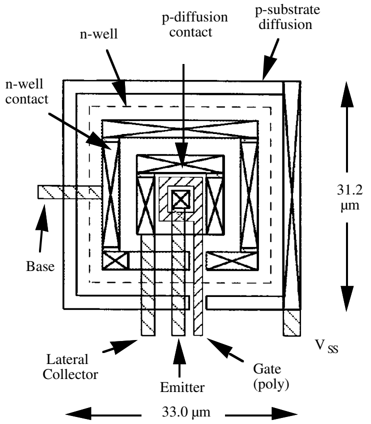
$ß_F \approx 50$ to 100 depending on the process



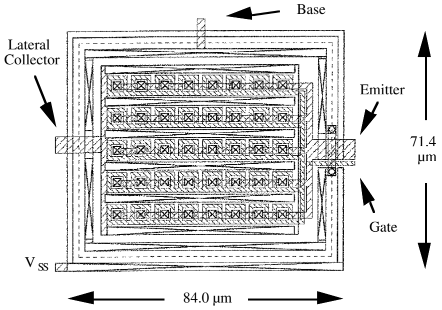
- Good geometry matching
- Low 1/f noise (if channel doesn't form)
- Acts like a photodetector with good efficiency

Geometry of the Lateral PNP BJT

Minimum Size layout of a single emitter dot lateral PNP BJT:

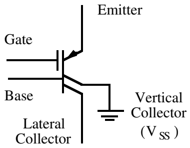


40 emitter dot LPNP transistor (total device area is 0.006mm^2 in a 1.2μm CMOS process):

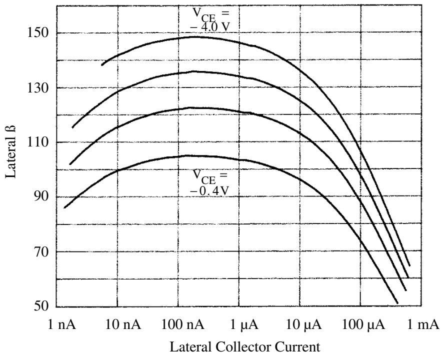


Performance of the Lateral PNP BJT

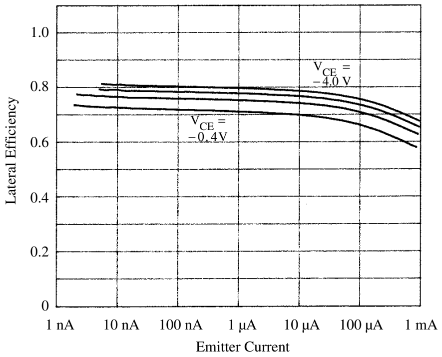
Schematic:



$ß_L$ vs I_{CL} for the 40 emitter dot LPNP BJT:



Lateral efficiency versus I_E for the 40 emitter dot LPNP BJT:



Performance of the Lateral PNP BJT - Continued

Typical Performance for the 40 emitter dot LPNP BJT:

Transistor area	0.006 mm^2
Lateral ß	90
Lateral efficiency	0.70
Base resistance	150 Ω
E_n @ 5 Hz	2.46 nV / $\sqrt{\text{Hz}}$
E_n (midband)	1.92 nV / $\sqrt{\text{Hz}}$
f_c (E_n)	3.2 Hz
I_n @ 5 Hz	3.53 pA / $\sqrt{\text{Hz}}$
I_n (midband)	0.61 pA / $\sqrt{\text{Hz}}$
f_c (I_n)	162 Hz
f_T	85 MHz
Early voltage	16 V

High Voltage MOS Transistor

The well can be substituted for the drain giving a lower conductivity drain and therefore higher breakdown voltage.

NMOS in n-well example:

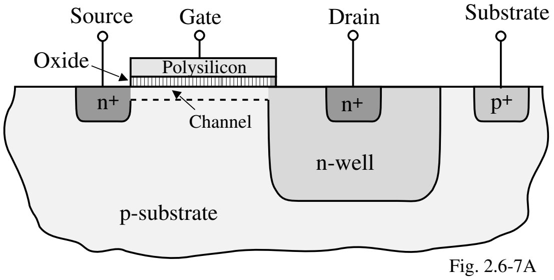


Fig. 2.6-7A

Drain-substrate/channel can be as large as 20V or more.

Latch-up in CMOS Technology

Latch-up Mechanisms

1. SCR regenerative switching action.
2. Secondary breakdown.
3. Sustaining voltage breakdown.

Parasitic lateral PNP and vertical NPN BJTs in a p-well CMOS technology:

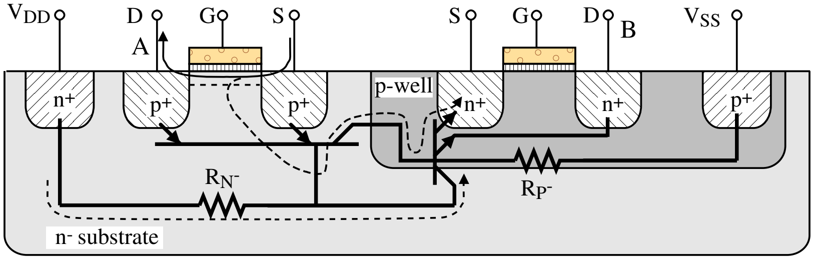


Fig. 2.6-8

Equivalent circuit of the SCR formed from the parasitic BJTs:

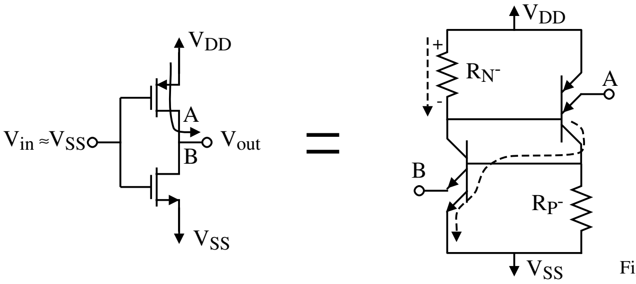


Fig. 2.6-9

Preventing Latch-Up in a P-Well Technology

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of R_{N^-} and R_{P^-}. This requires more current before latch-up can occur.

3.) Make a p^- diffusion around the p-well. This shorts the collector of Q1 to ground.

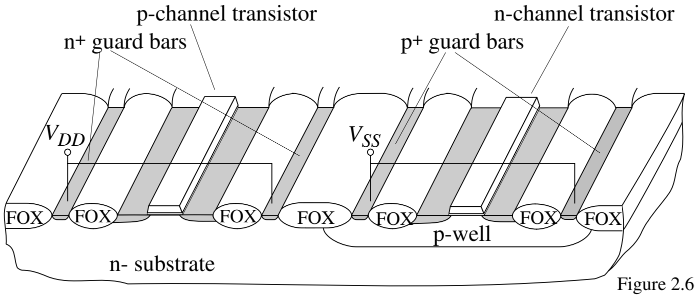


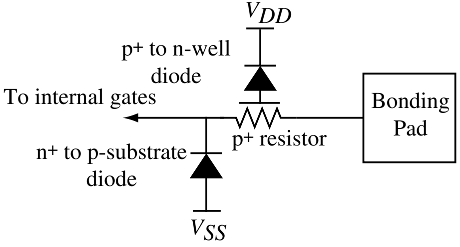
Figure 2.6-10

For more information see R. Troutman, “CMOS Latchup”, Kluwer Academic Publishers.

Electrostatic Discharge Protection (ESD)

Objective: To prevent large external voltages from destroying the gate oxide.

Electrical equivalent circuit



Implementation in CMOS technology

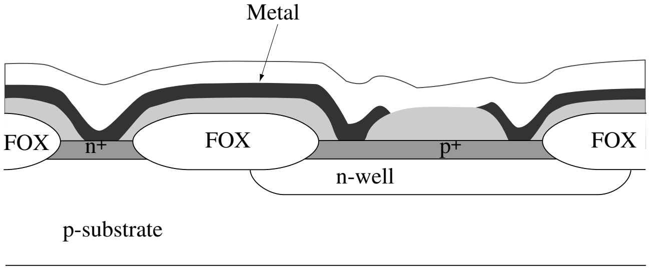


Fig. 2.6-11

Resistor Layout

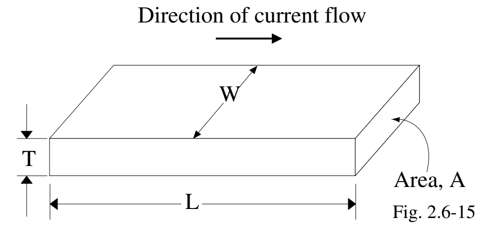


Fig. 2.6-15

Resistance of a conductive sheet is expressed in terms of

$$R = \frac{\rho L}{A} = \frac{\rho L}{WT}\ (\Omega)$$

where

ρ = resistivity in Ω-m

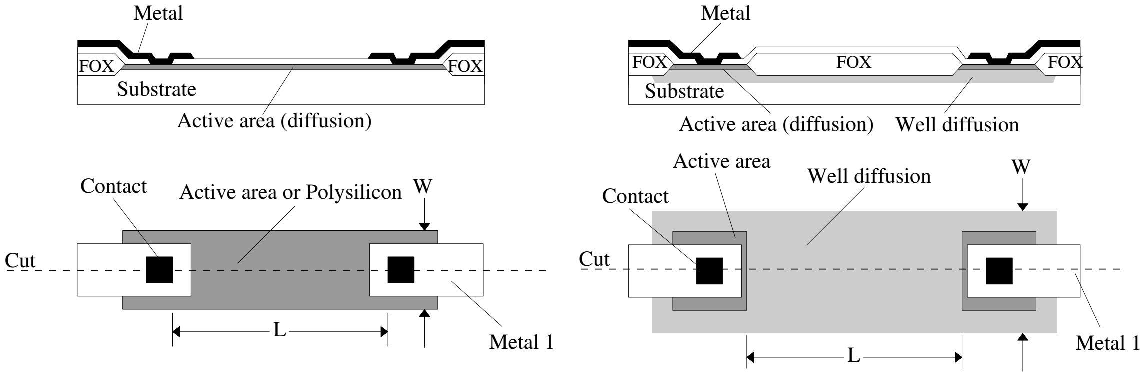
Ohms/square:

$$R = \left(\frac{\rho}{T}\right)\frac{L}{W} = \rho_S\,\frac{L}{W}\ (\Omega)$$

where

ρ_S is a sheet resistivity and has the units of ohms/square

Example of Resistor Layouts



Diffusion or polysilicon resistor

Well resistor

Fig. 2.6-16

Corner corrections:

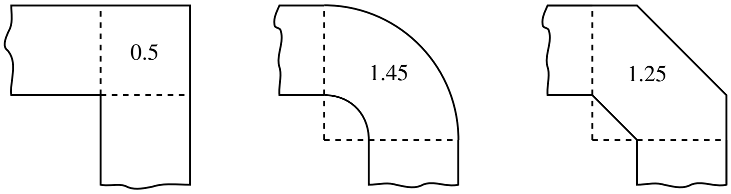


Fig. 2.6-16B

Example 2.6-1 Resistance Calculation

Given a polysilicon resistor like that drawn above with W=0.8μm and L=20μm, calculate ρ_S (in $\Omega/\square$), the number of squares of resistance, and the resistance value. Assume that ρ for polysilicon is 9×10^{-4} Ω-cm and polysilicon is 3000 Å thick. Ignore any contact resistance.

Solution

First calculate ρ_S.

$$\rho_S = \frac{\rho}{T} = \frac{9 \times 10^{-4}\ \Omega\text{-cm}}{3000 \times 10^{-8}\ \text{cm}} = 30\ \Omega/\square$$

The number of squares of resistance, N, is

$$N = \frac{L}{W} = \frac{20\mu\text{m}}{0.8\mu\text{m}} = 25$$

giving the total resistance as

$$R = \rho_S \times N = 30 \times 25 = 750\ \Omega$$

Capacitor Layout

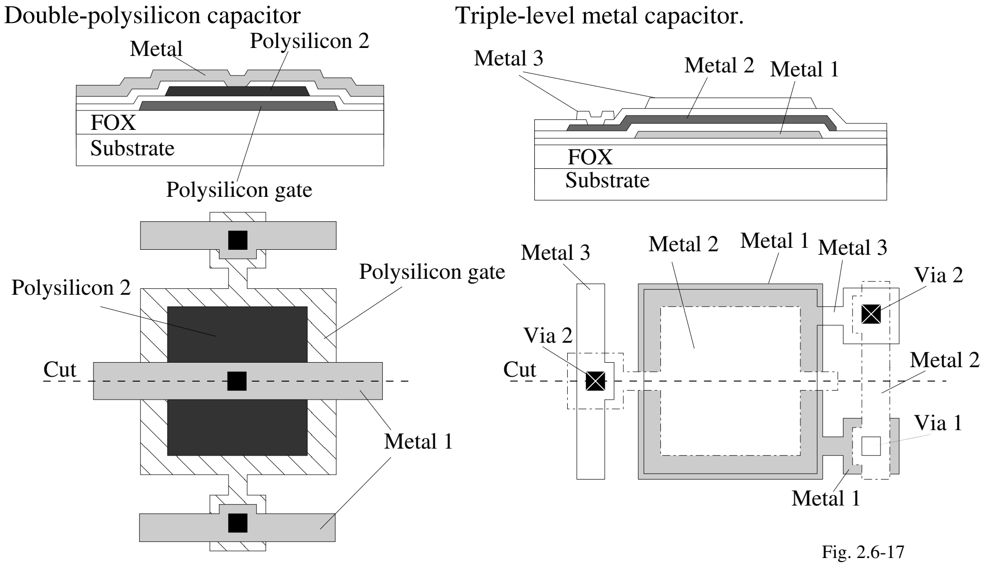


Fig. 2.6-17

Design Rules

Design rules are geometrical constraints which guarantee the proper operation of a circuit implemented by a given CMOS process.

These rules are necessary to avoid problems such as device misalignment, metal fracturing, lack of continuity, etc.

Design rules are expressed in terms of minimum dimensions such as minimum values of:

- Widths
- Separations
- Extensions
- Overlaps

- Design rules typically use a minimum feature dimension called “lambda”. Lambda is usually equal to the minimum channel length.
- Minimum resolution of the design rules is typically half lambda.
- In most processes, lambda can be scaled or reduced as the process matures.

SECTION 2.7 - BIPOLAR TRANSISTOR (OPTIONAL)

Major Processing Steps for a Junction Isolated BJT Technology

Start with a p substrate.

1. Implantation of the buried n^+ layer
2. Growth of the epitaxial layer
3. p^+ isolation diffusion
4. Base p-type diffusion
5. Emitter n^+ diffusion
6. p^+ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

Implantation of the Buried Layer (Mask Step 1)

Objective of the buried layer is to reduce the collector resistance.

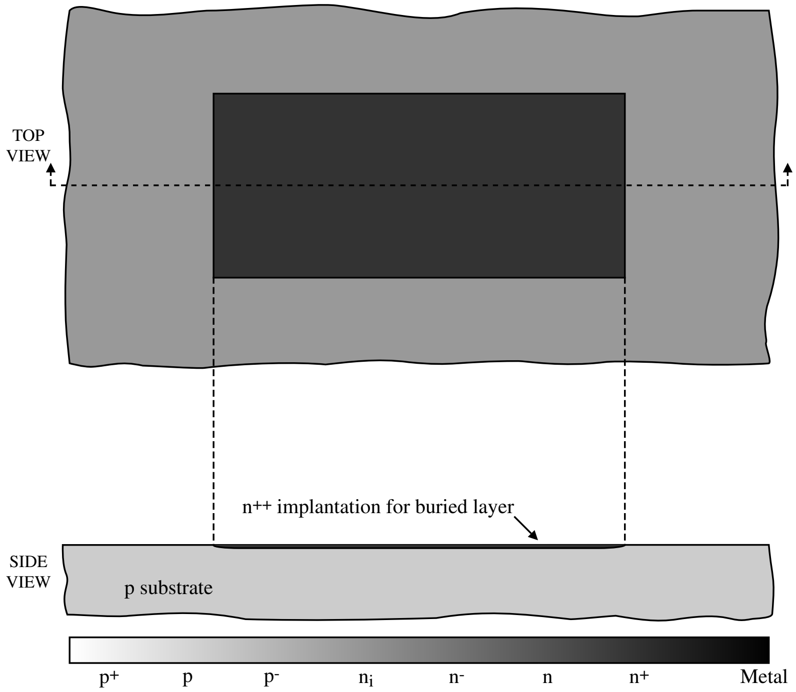


Fig.2.7-1

Epitaxial Layer (No Mask Required)

The objective is to provide the proper *n*-type doping in which to build the *npn* BJT.

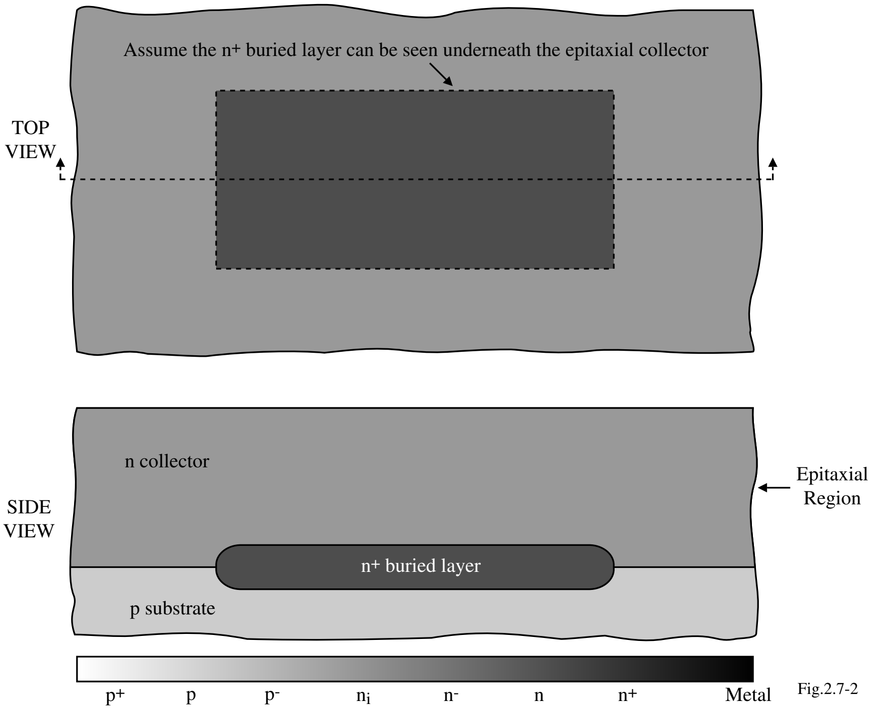


Fig.2.7-2

p^+ isolation diffusion (Mask Step 2)

The objective of this step is to surround (isolate) the *npn* BJT by a p^+ diffusion. These regions also permit contact to the substrate from the surface.

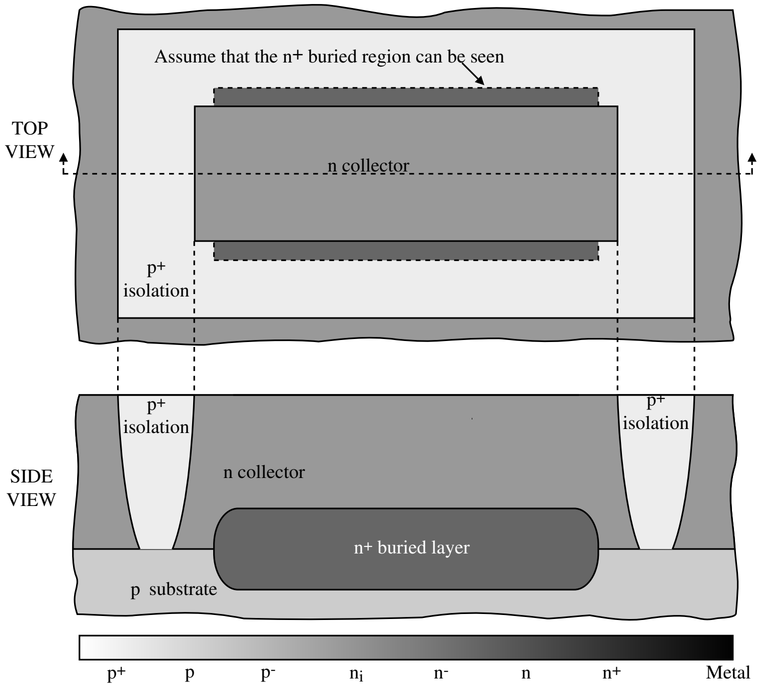


Fig.2.7-3

Base *p*-type diffusion (Mask Step 3)

The step provides the *p*-type base for the *npn* BJT.

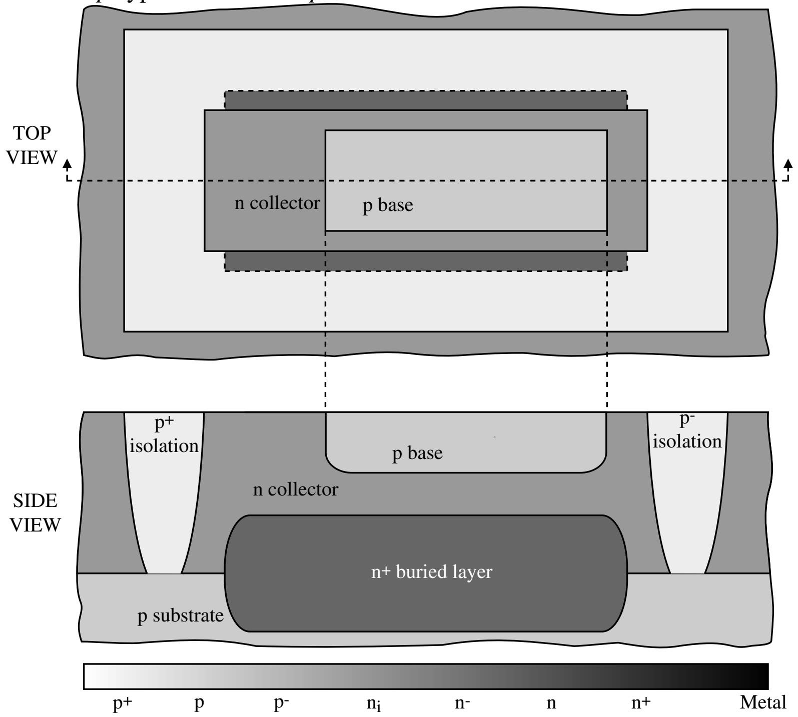


Fig.2.7-4

Emitter n^+ diffusion (Mask Step 4)

This step implements the n^+ emitter of the *npn* BJT and the ohmic contact to the collector.

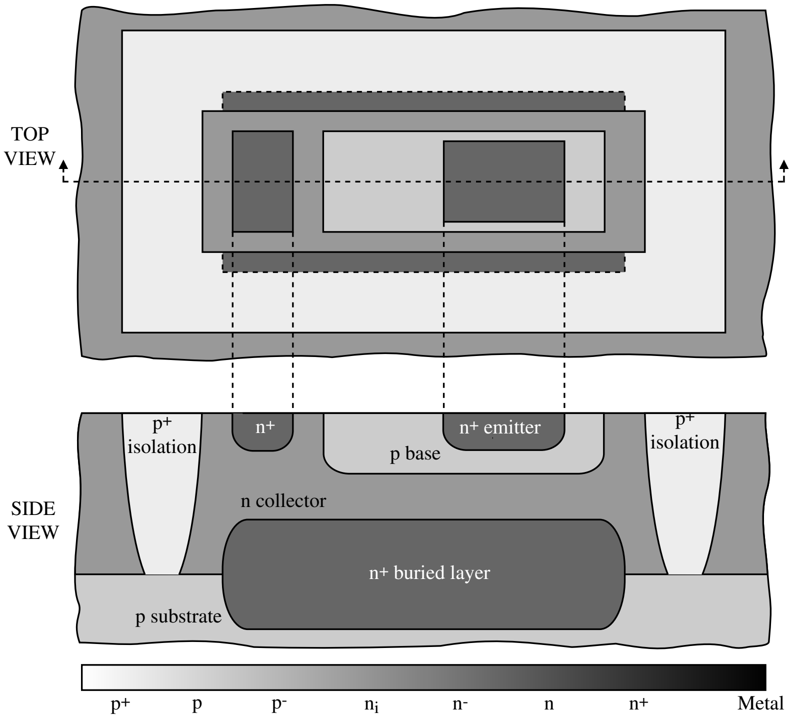


Fig.2.7-5

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p^+ ohmic contact (Mask Step 5)

This step permits ohmic contact to the base region if it is not doped sufficiently high.

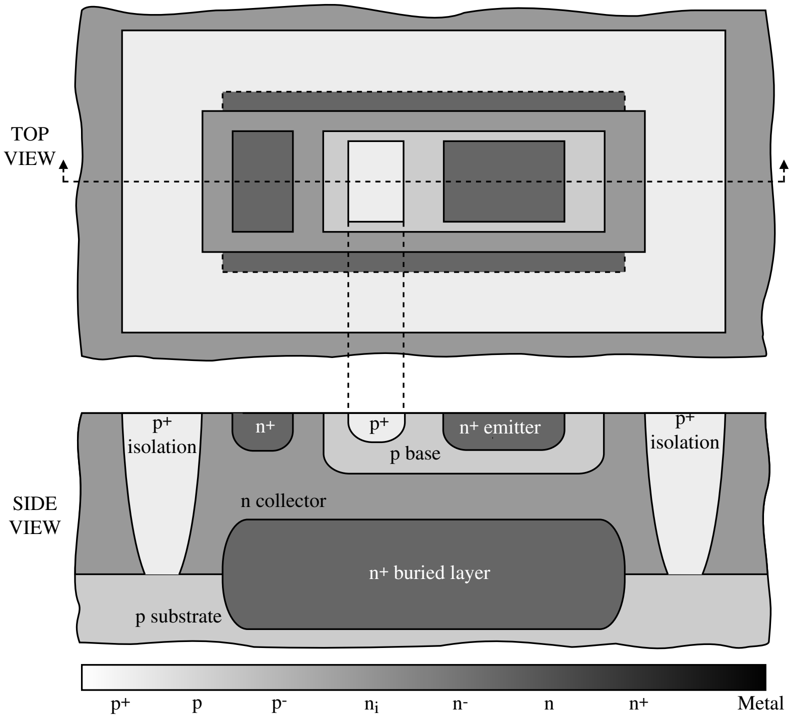

Fig.2.7-6

Contact etching (Mask Step 6)

This step opens up the areas in the dielectric area which metal will contact.

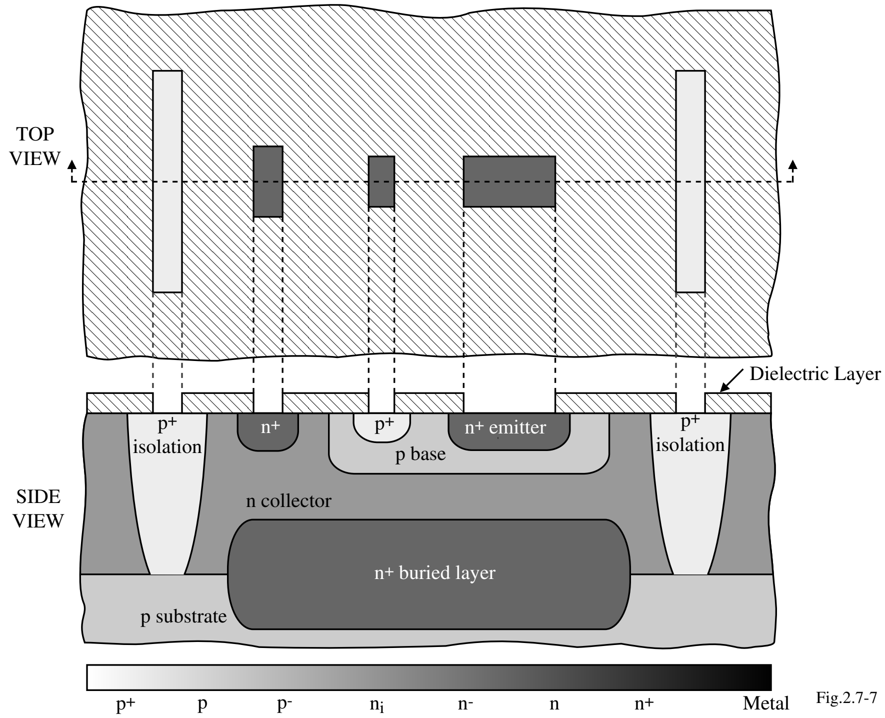

Fig.2.7-7

Metal deposition and etching (Mask Step 7)

In this step, the metal is deposited over the entire wafer and removed where it is not wanted.

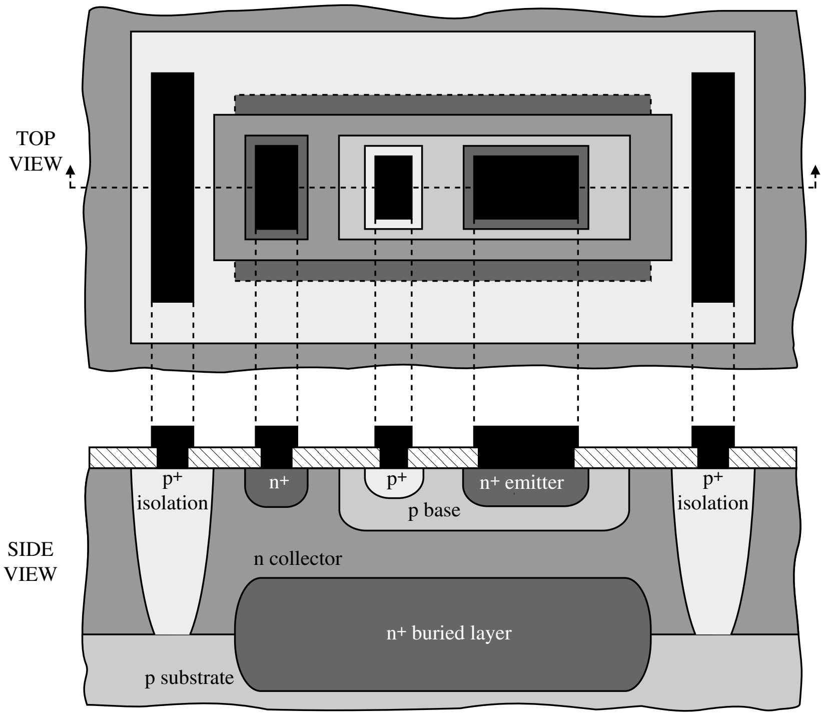

Fig.2.7-8

Passivation (Mask Step 8)

Covering the entire wafer with glass and opening the area over bond pads (which requires another mask).

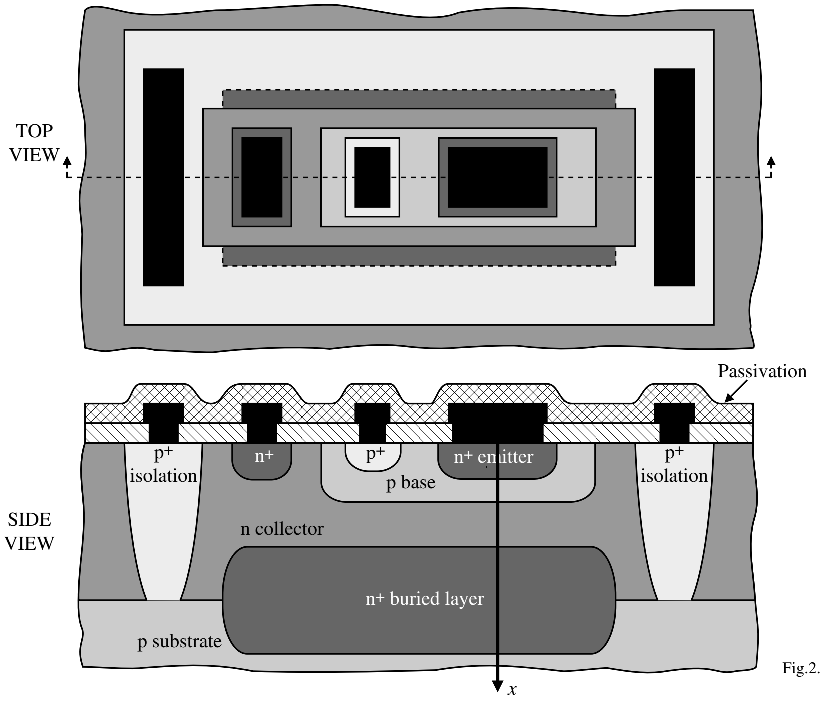

Fig.2.7-9

Typical Impurity Concentration Profile for the *npn* BJT

Taken along the line from the surface indicated in the last slide.

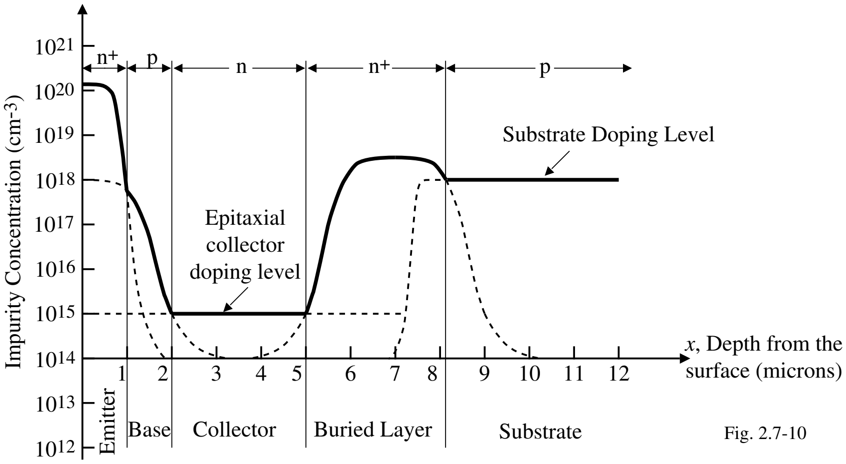

Fig. 2.7-10

Substrate *pnp* BJT

Collector is always connected to the substrate potential which is the most negative DC potential.

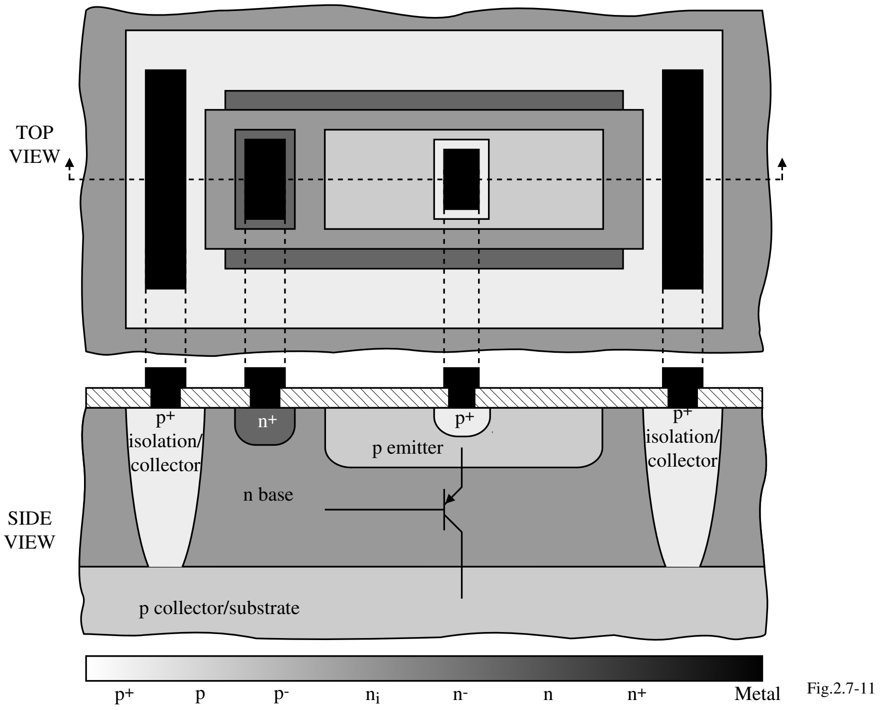

Fig.2.7-11

Lateral *pnp* BJT

Collector is not constrained to a fixed dc potential.

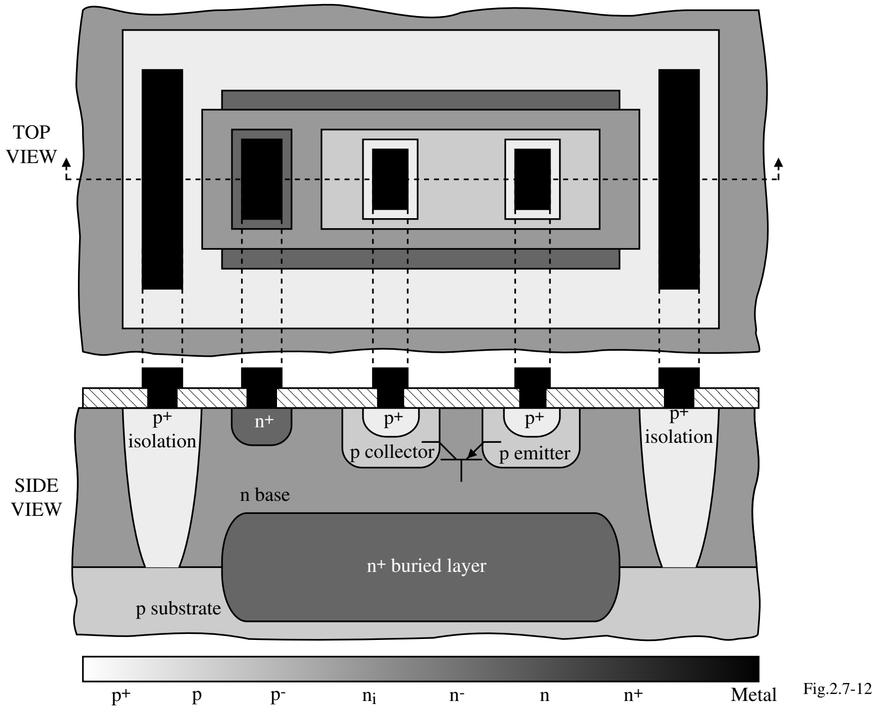

Fig.2.7-12

Types of Modifications to the Standard *npn* Technology

1.) Dielectric isolation - Isolation of the transistor from the substrate using an oxide layer.

2.) Double diffusion - A second, deeper n$^+$ emitter diffusion is used to create JFETs.

3.) Ion implanted JFETs - Use of an ion implantation to create the upper gate of a p-channel JFET

4.) Superbeta transistors - Use of a very thin base width to achieve higher values of β_F.

5.) Double diffused *pnp* BJT - Double diffusion is used to build a vertical *pnp* transistor whose performance more closely approaches that of the *npn* BJT.

SECTION 2.8 - BiCMOS TECHNOLOGY (OPTIONAL)

Typical BiCMOS Technology

The following pages describe a 0.5μm BiCMOS process typical of todays deep submicron technologies.

Masking Sequence:

1. Buried n$^+$ layer
2. Buried p$^+$ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide
10. Base implant
11. Capacitor implant
12. Hi resistance Poly
13. Poly 2
14. Emitter implant
15. Poly 1
16. NMOS lightly doped drain
17. PMOS lightly doped drain
18. n$^+$ source/drain
19. p$^+$ source/drain
20. Silicide protection
21. Contacts
22. Metal 1
23. Via 1
24. Metal 2
25. Via 2
26. Metal 3
27. Nitride passivation

Notation:

BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated by the reaction of oxygen and nitride, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate (actually tetraethyl orthosilicate). A chemical compound used to deposit conformal oxide films.

Photoresist Sequence for Deep Submicron Processes

1.) Coat
2.) Soft bake
3.) Expose
4.) Post exposure bake (avoid standing waves)
   - Avoids standing waves
   - Gives increased contrast
   - Improves adhesion

5.) Develop
6.) Hardbake
7.) DUV flood exposure (etch or implant) - Optional

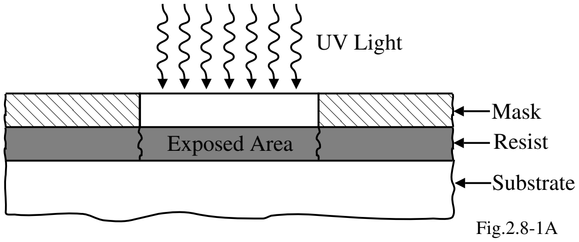

Fig.2.8-1A

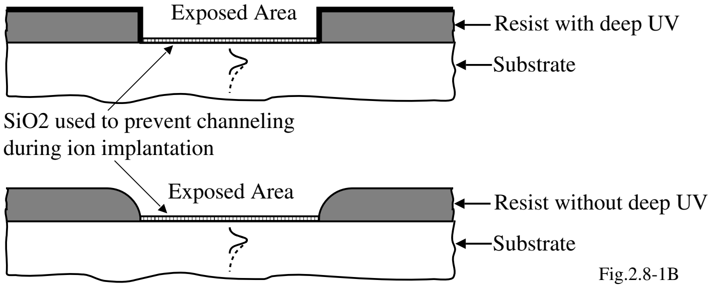

Fig.2.8-1B

Generic Photoresist Processing Sequence

1.) Wafer is coated with photoresist.
2.) Photoresist is exposed through a photomask or reticle
3.) Exposed photresist is developed away
4.) Wafer/film unprotected by photoresist is etched and/or ion implanted
5.) Remaining unexposed photresist is stripped off of the wafer.

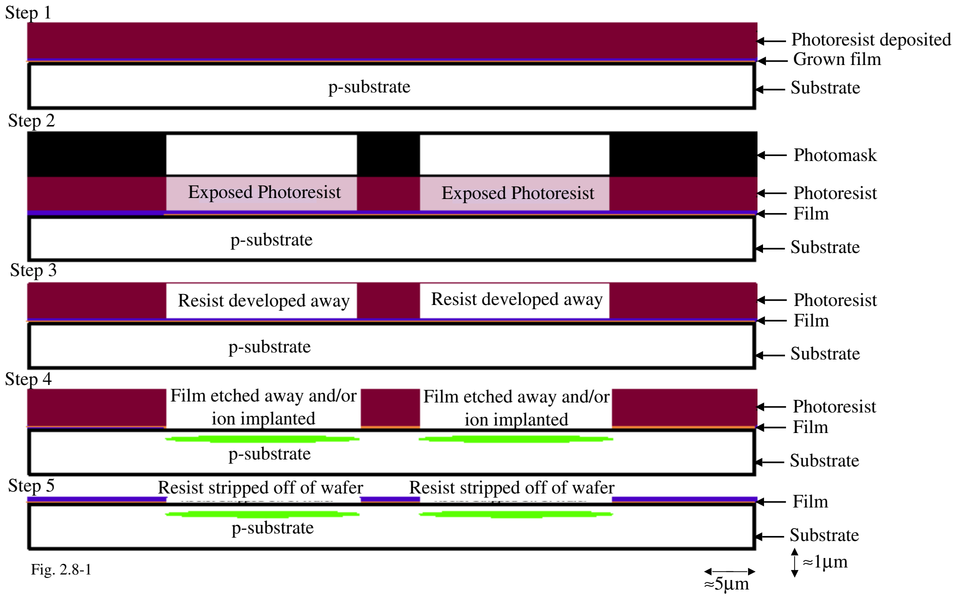

Fig. 2.8-1

n^+ Buried Layer Mask

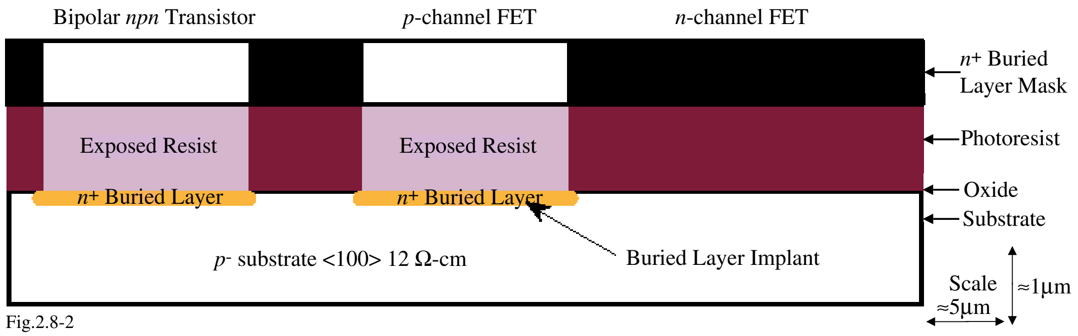

Fig.2.8-2

Process Step	Description	Reason
Starting Material	*p*-type, <100>, 12Ω-cm	*p*-type for isolating the collector of the *npn* transistor. <100> wafer orientation, specifies the crystal orientation with the least amount of Si atoms at the surface, hence the fewest dangling bonds, interface states, etc., which adversely effects the MOS performance and low current *npn* beta. Non-epi wafers are used for processes initially with the epitaxial silicon (epi) to be added later.
Laser Scribe	Laser lettering	Labels each wafer as to the wafer number and lot number
Pre-implant oxidation	Thermal oxide	Minimizes the buried layer implant channeling
n^+ Buried Layer Mask	**Shape=Dark**	**Defines the n^+ buried layer region by clearing it of photoresist**
Buried layer implant	Arsenic (AS-75)	Implants arsenic to create the n^+ buried layer

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p^+ Buried Layer

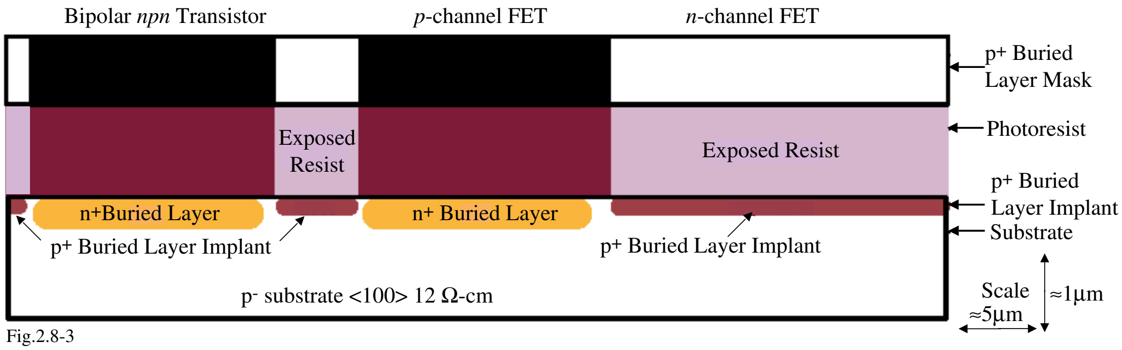


Fig.2.8-3

Process Step	Description	Reason
n^+ Resist Strip	Plasma Strip	Removes the photoresist used to mask the non-buried n^+ areas from ion implantation
n^+ Buried Layer Anneal and Oxidation	Thermal oxide	Anneals damage to the silicon from the $n+$ buried layer implant and grows oxide
p^+ Buried Layer Mask	**Shape=Clear**	**Defines the p^+ buried layer/ isolation region by clearing it of photoresist**
Buried layer implant	Boron (B-11)	Implants boron to create the p^+ buried layer

Epitaxial Growth

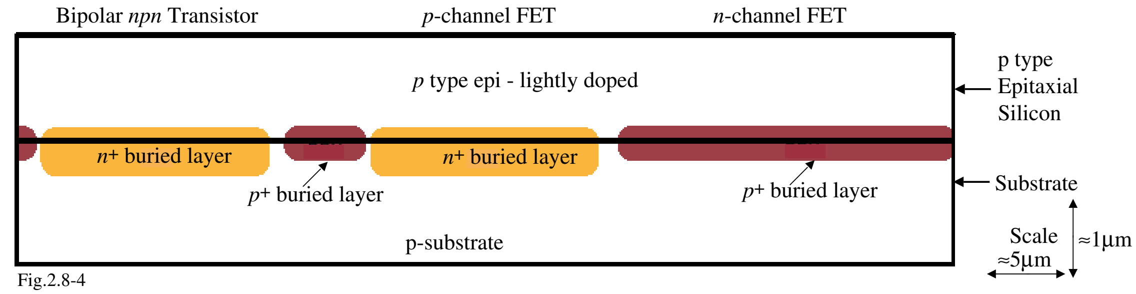


Fig.2.8-4

Process Step	Description	Reason
p^+ Resist Strip	Plasma Strip	Removes the photoresist used to mask the non-buried p^+ areas from ion implantation
p^+ Buried Layer Anneal and Oxidation	Thermal oxide - Furnace	Anneals damage to the silicon from the *p*+ buried layer implant
Epitaxial Growth	CVD Deposition	Grows additional <100> silicon on top of the existing silicon and implants. This is the layer which will be used for fabricating the active devices. The lightly doped *p*-type epi will not interfere with the twin well and collector tub doping which will come later.

Collector Tub

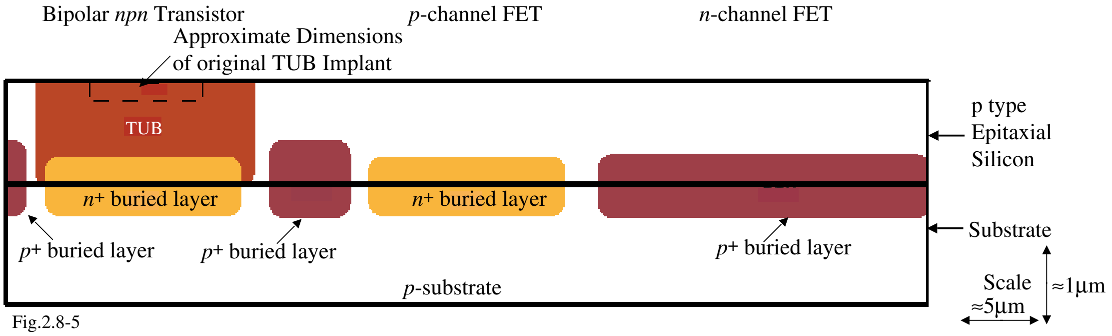


Fig.2.8-5

Process Step	Description	Reason
Tub Oxidation	Thermal Oxidation	Minimizes the TUB implant channeling
TUB Mask	**Shape = Dark**	**Defines the *npn* collector tub region**
TUB Implant	Phosphorus (P-31)	Implants phosphorus into the *npn* collector tub region.
Resist Strip	Plasma-Strip	Premoves the photoresist used to mask the non-tub regions from implant.
TUB Anneal and Drive	Thermal-Furnace	Anneals silicon damage and drives the phosphorus deep into the silicon to form the tub.
TUB Oxide Etch	Wet Etch	Removes oxide prior to growing pad oxide.

Active Area Definition

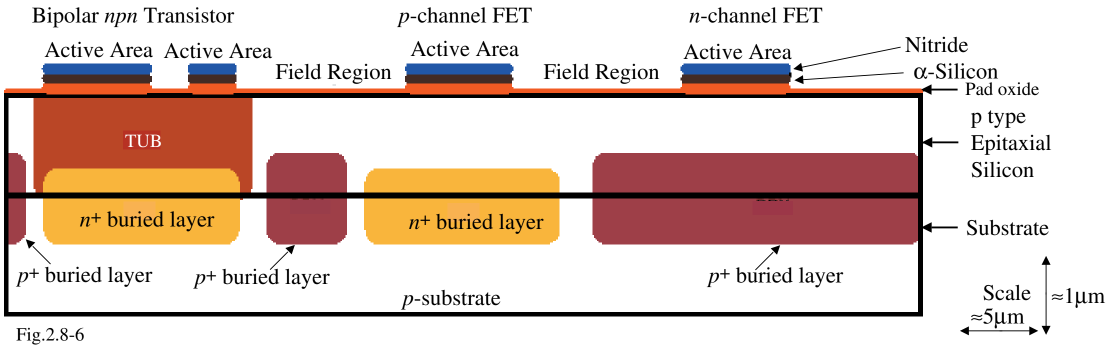


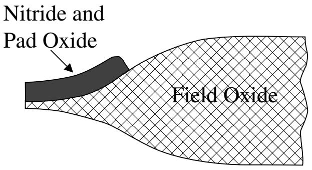
Fig.2.8-6

Process Step	Description	Reason
Pad Oxidation*	Thermal Oxidation	Stress relief for nitride (a very high stress film) to eliminate stress induced dislocations in the silicon. Oxidation consumes ≈46% of its thickness in the silicon. Therefore for a thickness of 175Å there is 81Å down and 94Å up.
α-Silicon Deposition*	LPCVD Silicon	α-Silicon is polysilicon deposited at low temperatures and is still amorphous. It is used for additional stress relief for the nitride and to minimize the bird's beak encroachment into the active regions
Nitride Deposition*	LPCVD	Oxidation barrier for subsequent field oxidation
Active Area Mask	**Shape = Clear**	**Defines the active areas (where active devices are formed) and the field regions. Active areas remain covered with the resist.**
Nitride Etch	Dry Etch	Removes the nitride, α-Silicon and some/all of the oxide, exposing the field regions
Resist Strip	Plasma Strip	Removes the photoresist used to mask the active areas from the etching

* These steps constitute locally oxidized silicon isolation known as LOCOS which is used to prevent field oxide from growing in active regions.

Bird's Beak Formation - Information

Bird's Beak under normal conditions



Bird's Beak with the nitride too thick

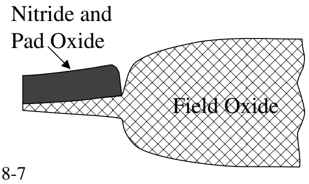


Fig. 2.8-7

Collector Sink and *n*-Well Region Definitions

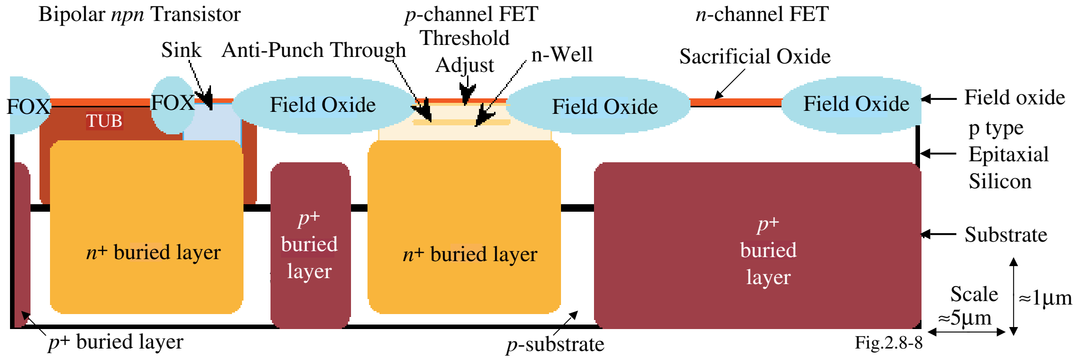


Fig.2.8-8

Process Step	Description	Reason
Field Oxidation	Thermal Oxidation	Isolates silicon form conductor layers and the related effects
Nitride & α-Silicon Etch	Wet/Dry Etch	Removes remaining nitride, α-Silicon, and oxide
Sacrificial Oxidation	Thermal Oxidation	Cleans the Si surface prior to gate oxidation, and removes Kooi nitride
Collector Sinker Mask	**Shape = Dark**	**Defines the collector sinkers to connect the *n*+ buried layer to the surface**
Sink Implant	Phosphorus (P-31)	Implants collector sinkers
Resist Strip	Plasma Strip	Removes the photoresist used to mask non-Sink areas from the implant
Sink Anneal	Thermal-Furnace	Anneals damage to silicon and begins to drive-in the Sink
***n*-Well Mask**	**Shape = Dark**	**Defines the *n*-well regions by clearing them of photoresist**
n-Well Implant	Phosphorus (P-31)	Implants the *n*-Well region for the *p*-channel FETs
n-well Anti-Punch Through Implant	Phosphorus (P-31)	Implants Anti-Punch Through region at the base of the source/drains. Dopes the region under the well higher.
n-Well Threshold Implant	Phosphorus (P-31)	Adjusts the *p*-channel transistor threshold voltage
Resist Strip	Plasma Strip	Removes the photoresist used to mask non-*n*-Well areas from the implant
n-well Anneal	Thermal-Furnace	Anneals damage to silicon and drives-in the *n*-Well and collector sink

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Definition of the *p*-Well and Emitter Window Regions

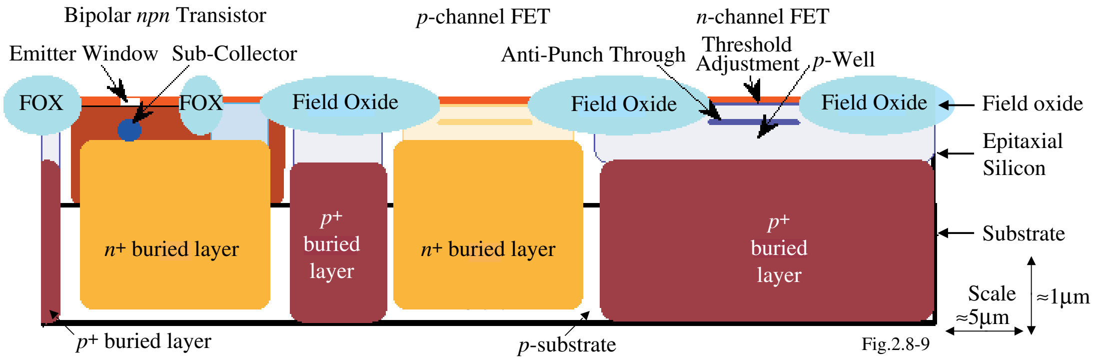

Fig.2.8-9

Process Step	Description	Reason
***p*-Well Mask**	**Shape = Clear**	**Defines the *p*-Well regions by clearing them of photoresist**
p-Well Implant	Boron (B-11)	Implants the *p*-Well region for *n*-channel FETs
p-Well Anti-Punch Through Implant	Boron (B-11)	Implants the Anti-Punch Through region at the base of the source/drains
p-Well Threshold Implant	Boron (B-11)	Adjusts the *n*-channel transistor threshold voltage
Resist Strip	Plasma Strip	Removes resist used to mask non-*p*-Well areas from implant
Emitter Window Mask	**Shape = Dark**	**Defines the Emitter Window regions by clearing them of resist**
Sub-Collector Implant	Phosphorus (P-31)	Implants the sub-collector to reduce the collector resistance and defines the depth of the base into the collector of the *npn* transistor. (Saves the sacrificial oxide over the BJT)
Oxide Etch	Dry Etch	Defines the location of the *npn* emitter by opening the oxide
Resist Strip	Plasma Strip	Removes resist used to mask non-emitter areas from implant and etch
Oxide Etch and Clean	Wet etch/clean	Cleaning step which removes any remaining oxide or polymer in the emitter window

Definition of Active Area where Base Oxide will Remain after Etch

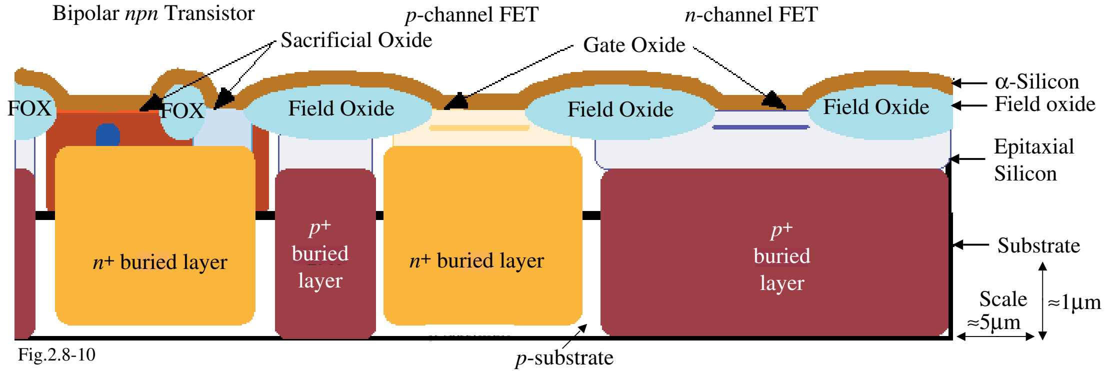

Fig.2.8-10

Process Step	Description	Reason
Base Oxide Mask	**Shape = Clear**	**Defines the FET regions by clearing them of photoresist so the base oxide can be etched, a gate oxide can be grown and the Base oxide over the *npn* transistors protected.**
Oxide Etch	Wet Etch	Removes the sacrificial oxide in the exposed CMOS regions
Resist Strip	Plasma Strip	Removes the photoresist used to mask the *npn* base/emitter regions.
Gate Oxidation	Thermal Oxidation	Grows gate oxide insulator between oxide and Poly1 gate and anneals the damage from the emitter silicon surface.
α-Silicon Deposition	LPCVD Silicon	Deposits the first layer of gate Poly1 to protect the gate oxide.

Implantation of the Base and Doping of the Poly Emitter

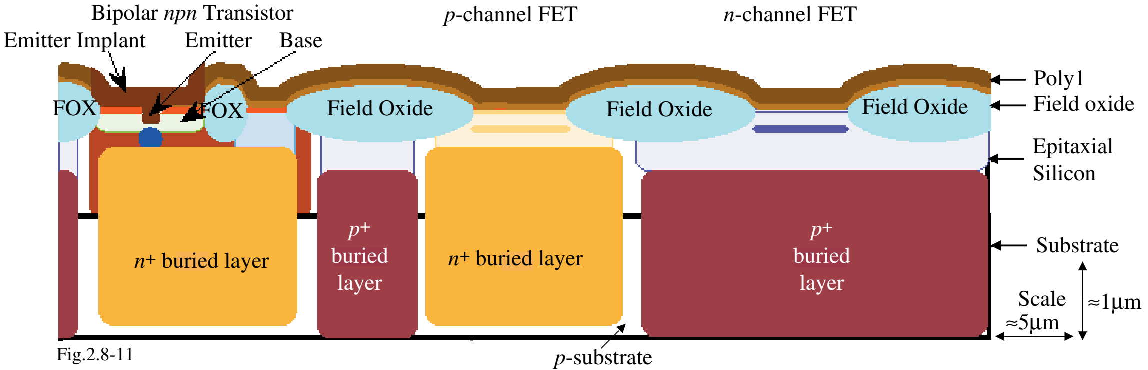

Fig.2.8-11

Process Step	Description	Reason
Base Implant Mask	**Shape = Dark**	**Defines Emitter Window regions by clearing them of photoresist**
α-Silicon Etch	Dry/Wet Etch	Removes the α-Silicon over the emitter/base of the *npn* transistors
Base Implant	Boron (B-11)	Implants the intrinsic base of the *npn*
Resist Strip	Plasma Strip	Removes resist used to mask non-*p*-Well areas from implant
Oxide Etch	Wet Etch	Removes oxide in the emitter window
Poly1 Deposition	LPCVD	Thickens the α-Silicon for better conduction and contacts silicon in the emitter window to enable formation of the *npn* emitter
Blanket Implant	Arsenic (As-75)	Dopes the poly just sufficiently to make it conductive and prevent any charging problems
Emitter Implant Mask	**Shape = Dark**	**Defines the region over the *npn* transistors for emitter implant**
Emitter Implant	Arsenic (As-75)	Implants the Poly1 over the emitter window
Resist Strip	Plasma Strip	Removes resist masking poly protected from the implant
Poly Emitter Anneal	Thermal-Furnance	Diffuses the implant from the Poly1 into the silicon to form the emitter

Capacitor Bottom Plate and High Resistance Poly Implants

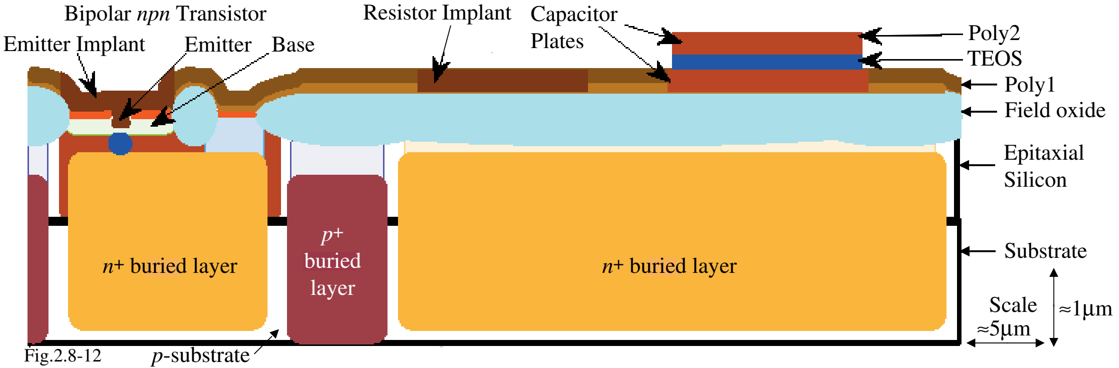

Fig.2.8-12

Process Step	Description	Reason
Capacitor Implant Mask	**Shape = Dark**	**Defines the bottom capacitor plates by clearing them of resist**
Capacitor Implant	Phosphorus (P-31)	Implants the bottom plate of the capacitor making it conductive
Resist Strip	Plasma-Strip	Removes resist masking non-capacitor areas from implant
Anneal	Furnace	Makes the dopant electrically active in the polysilicon
Hi Resistance Poly Mask	**Shape = Dark**	**Defines the high value resistors by clearing them of resist**
Resistor Implant	Boron (B-11)	Implants the high value resistor to ≈ 1000Ω/square
Resist Strip	Plasma Strip	Removes resist masking the non-hi resistance poly areas from the implant
TEOS Deposition/Densification	LPCVD Oxide	Deposits the capacitor dielectric
α-Silicon Deposition	LPCVD	Deposits the capacitor top plate
Capacitor Implant	Boron (B-11)	Implants capacitor top plate making it electrically conductive
Anneal	Furnace	Makes the polysilicon electrical active in the polysilicon
Poly2 Mask	**Shape = Clear**	**Defines the capacitor top plate by covering them with resist**
Poly2 Etch	Dry Etch	Removes the Poly2 where not protected by photoresist
Resist Strip	Plasma Strip	Removes the photoresist masking top capacitor plate from the etch

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Poly1, *n*-Channel LD Source/Drains and *p*-Channel LD Source/Drains Definitions

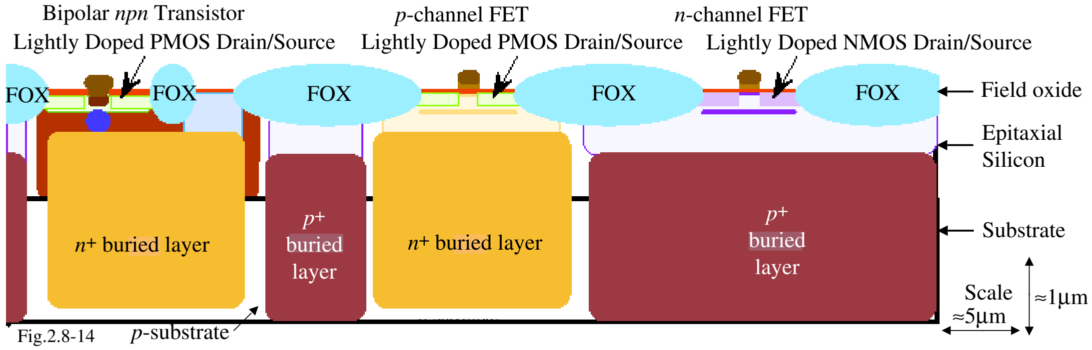

Fig.2.8-14

Process Step	Description	Reason
Poly1 Mask	**Shape = Clear**	**Defines the Poly1 gates and local interconnects**
Poly1 Etch	Plasma-Strip	Removes the Poly1 where not protected by photoresist
Resist Strip	Plasma-Strip	Removes the protective photoresist
Poly oxidation	Thermal Oxidation	Anneals the surface states of the poly grain boundaries, oxidizes charge states at the edges of Poly1 gates, anneals traps in silicon surface reducing the S/D leakage
NMOS Drain/Source Mask	**Shape = Clear**	**Defines the *n*-channel D/S by removing the resist covering them**
NMOS Lightly Doped Drain/ Source Implant	Phosphorus (P-31)	Implants the *n*-channel lightly doped source and drain regions
Resist Strip	Plasma Strip	Removes the resist masking the non-*n*-channel FETs and other regions
PMOS Drain/Source Mask	**Shape = Dark**	**Defines the *p*-channel D/S by removing the resist covering them**
PMOS Lightly Doped Drain/ Source Implant	Boron (B-11)	Lightly doped *p* implant in the *p*-channel drain/source regions and the base region
Resist Strip	Plasma-Strip	Removes the resist masking the non-*p*-channel FETs and other regions

Spacer Oxide Formation - Information

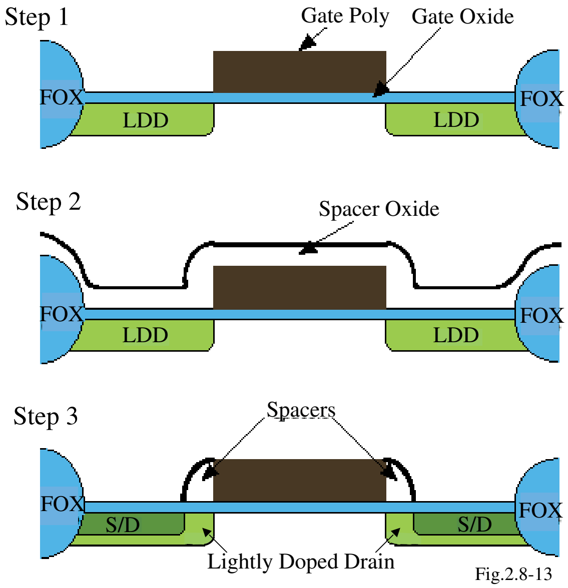

Fig.2.8-13

Step 1 - FET receives a light LDD implant, which is defined by poly gate and field oxide.

Step 2 - FET is conformally coated with spacer oxide which is much thicker at edge of poly gate.

Step 3 - Spacer oxide is etched leaving only the thickest part intact along the edge of the poly gate and the FET receives a heavy source/drain implant.

Heavily Doped Implants for Source/Drains of the *n*-Channel and *p*-Channel FETs

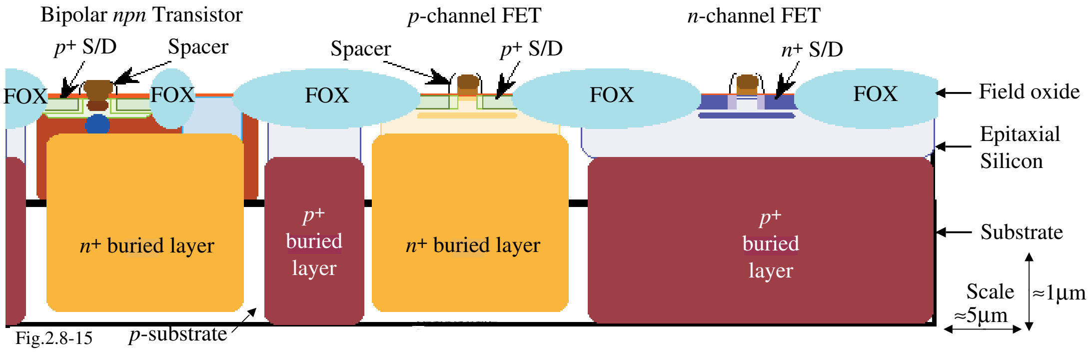

Fig.2.8-15

Process Step	Description	Reason
TEOS Deposition	LPVCD Oxide	Deposits oxide to create sidewall spacer on FET gates
Spacer Etch	Dry Etch	Removes the TEOS except along the edges of the Poly1 lines
Source/Drain Oxidation	Thermal Oxidation	Minimizes the S/D implant channeling
n^+ Source/Drain Mask	**Shape = Clear**	**Defines the *n*-channel S/D's by removing the resist covering them**
n^+ Source/Drain Implant	Arsenic (As-75)	n^+ implant into the *n*-channel source and drain regions
Resist Strip	Plasma Strip	Removes the resist masking the non-*n*-channel FETs and other regions
Source/Drain Anneal	Furnace	Makes the n^+ S/D and LDD's implants electrically active in the silicon
p^+ Source/Drain Mask	**Shape = Dark**	**Defines the *p*-channel D/S's by removing the resist covering them**
p^+ Source/Drain Implant	Boron (B-11)	p^+ implant into the *p*-channel source and drain and extrinsic base regions
Resist Strip	Plasma-Strip	Removes the resist masking the non-*p*-channel FETs and other regions

Preparation for Silicide Application

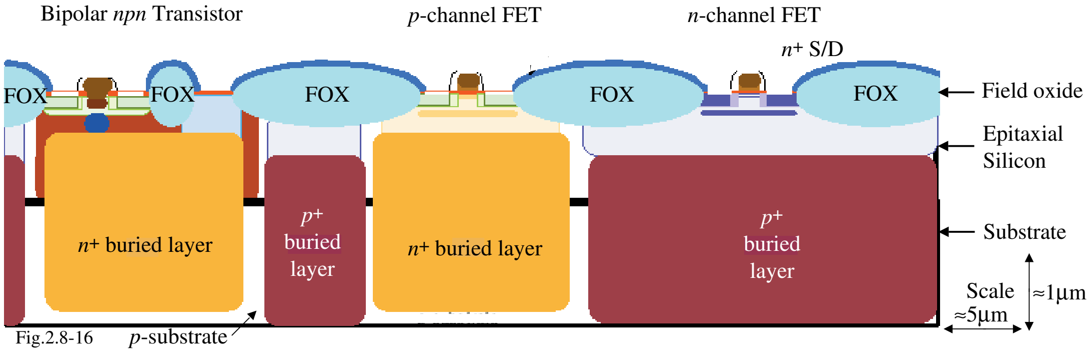

Fig.2.8-16

Process Step	Description	Reason
Silicon TEOS Deposition	LPVCD	Deposits oxide film to protect poly and silicon from silicidation
Nitride Deposition	LPVCD	Deposits nitride film to protect poly and silicon from silicidation
Resist Coat	Photoresist	Protects front side of the wafer from etching
Backside etch	Dry Etch	Removes nitrides, oxides, etc. from the back of the wafer
Silicide Protection Mask	**Shape = Clear**	**Opens up the photoresist over areas to be silicided**
Nitride Etch	Dry Etch	Removes the nitride and oxide from poly and silicon
Resist Strip	Plasma-Strip	Removes resist masking the remaining nitride
Junction Anneal	Furnace	Makes the p^+ source/drain implants electrically active in the silicon

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Application of the Silicide

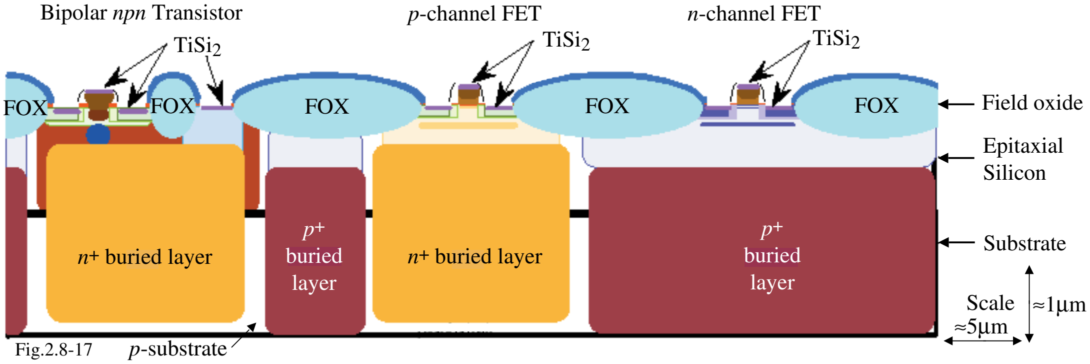

Fig.2.8-17

Process Step	Description	Reason
Oxide Etch	Wet Etch	Removes native oxide from poly and silicon
TiTiN Deposition	Sputtering	Deposits Ti film to form the silicide followed by TiN to act as a protective layer to prevent excess Si diffusion to the surface.
Anneal	Rapid Thermal Processor	Allows the Ti and Si to mutually interdiffuse and form TiSi$_2$ in the contacts and in Schottky structures
TiN Etch	Dry Etch	Removes TiN and unreacted Ti from the surface

Contacts

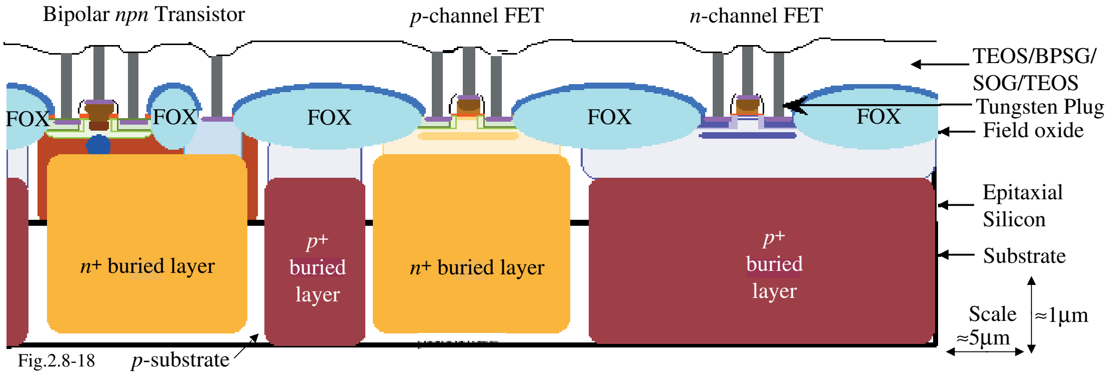

Fig.2.8-18

Process Step	Description	Reason
TEOS Deposition	LPCVD Oxide	Provides a good conformal coating, adhesion, and separation between $TiSi_2$ & BPSG
BPSG Deposition	LPCVD Oxide	Boron and Phosphorus make this glass flow and planarize as well as insulate silicon/metal1. The phosphorus also traps moisture and mobile ions.
Spin-On Glass (SOG)	Spin	Deposited as a viscous liquid, like resist, it provides a very planar dielectric.
Etchback	Etch	Flattens/planarizes the SOG to improve subsequent metal step-coverage.
TEOS Deposition	LPCVD Oxide	Second coating provides a good conformal coating, adhesion, and separation between BPSG/SOG and metal1.
Contact Mask	**Shape = Dark**	**Opens up the photoresist over contacts**
Contact Etch	Dry Etch	Removes the oxide over contacts to poly and silicon
Resist Strip	Plasma Strip	Removes resist masking the remaining oxide
TiN Deposition	Sputtering	Acts as an adhesive layer for the tungsten plug
Tungsten Deposition	Sputtering	Deposits tungsten in the contact holes and on the wafer surface
Tungsten Etchback	Dry Etch	Removes tungsten from the wafer surface

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Tungsten Contact and Via Fill - Information

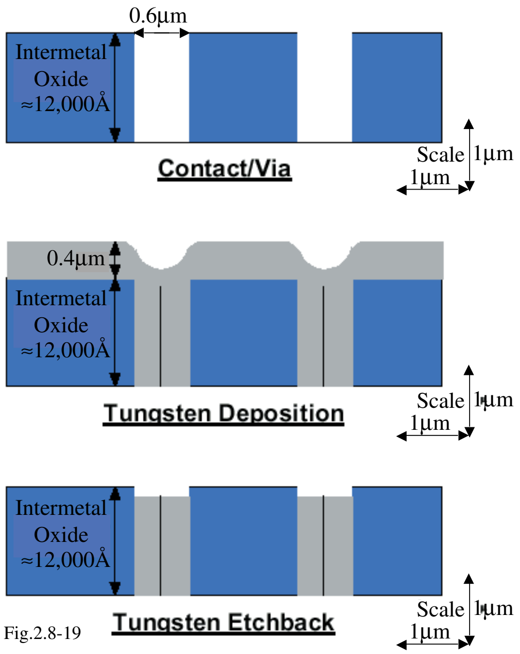
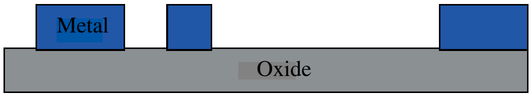
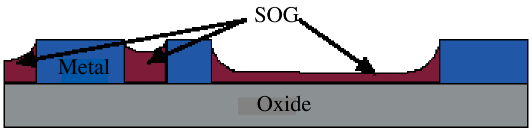


Fig.2.8-19

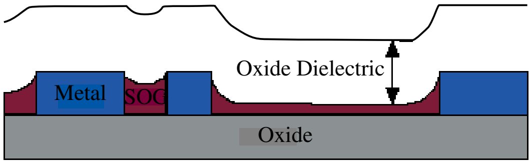
Spin On Glass Planarization - Information



Prior to Spin On Glass (SOG)



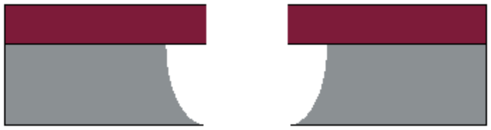
After Spin On Glass (SOG)



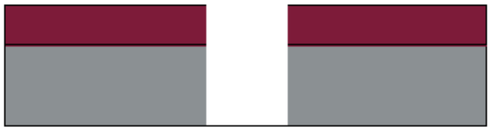
After Dielectric Depositon

Fig.2.8-21

Etch Types and Results - Information



Isotropic Etch (Wet/Dry)



Anisotropic Etch (Dry Only)

Anisotropic/Isotropic Etch (Wet & Dry)

Fig.2.8-22

Wet etch provides good step coverage while dry etch provides good feature size. The dry/wet combinations provide both.

SEM of the Tungsten Contact

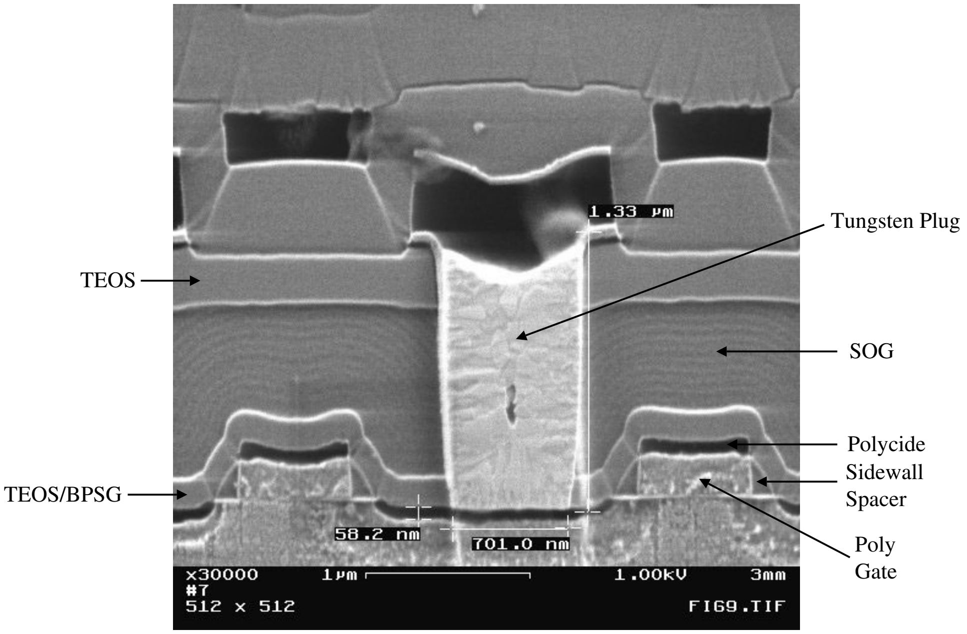


Fig. 2.8-20

Metal1

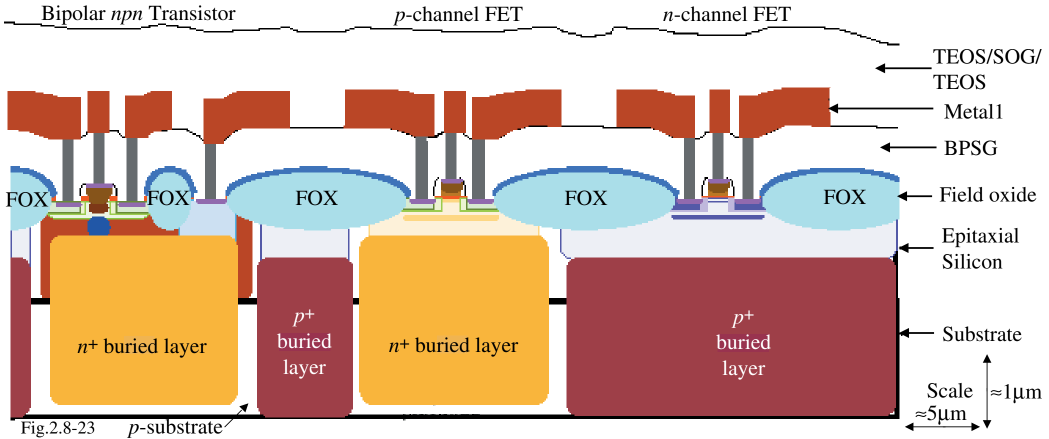


Fig.2.8-23

Process Step	Description	Reason
TiN Deposition/Nitridation	Reactive Sputtering	Acts as adhesion/barrier layer between aluminum and tungsten
Aluminum Deposition	Sputtering	Deposits conductive aluminum layer on the wafer surface
TiN AntiReflection Coating	Sputtering -ARC	Aids photoresist processing by eliminating standing waves
Metal1 Mask	**Shape = Clear**	**Defines Metal1 lines which remain protected from etching**
Metal1 Etch	Dry Etch	Removes unprotected metal1 leaving conducting lines
Resist Strip	Plasma Strip	Removes resist masking the protected metal conducting lines
TEOS Deposition	LPCVD Oxide	Provides a good conformal coating, adhesion, & separation between Metal1 & SOG
Spin-On Glass (SOG)	Spin	Deposited as a viscous liquid, like resist, to provide a very planar dielectric
Anneal and Etchback	Etch	Flattens/planarizes high points and corners in the SOG to improve the subsequent metal step-coverage
TEOS Deposition	LPCVD Oxide	Second coating provides a good conformal coating, adhesion, and separation between SOG and metal2

Metal1-Metal2 Vias and Metal2

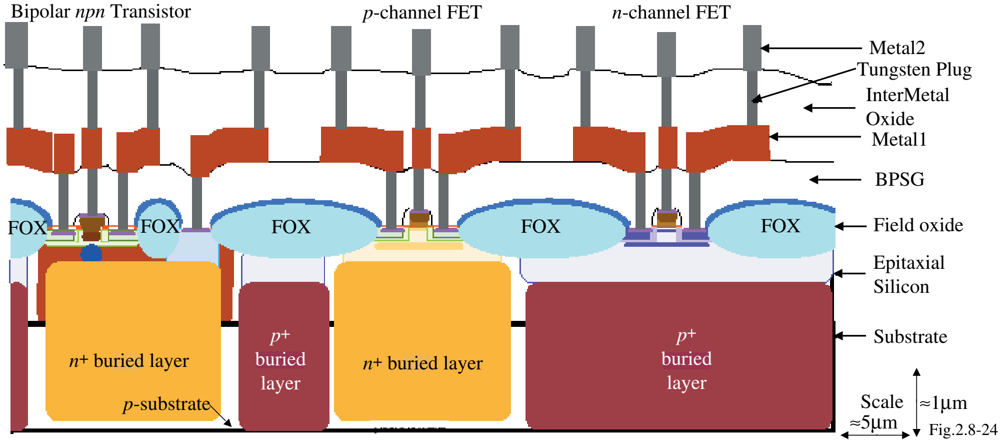


Fig.2.8-24

Process Step	Description	Reason
Via1 Mask	**Shape = Dark**	**Defines vias by opening the photoresist over the via locations**
Via1 Etch	Dry Etch	Removes oxide in vias leaving openings in oxide to metal1
Resist Strip	Plasma-Strip	Removes resist masking the protected metal lines
TiN Deposition	Sputtering	Acts as an adhesive layer for the tungsten plug
Tungsten Deposition	Sputtering	Deposits tungsten in the via holes and on the wafer surface
Tungsten Etchback	Dry Etch	Removes tungsten from the wafer surface
TiN Deposition/Nitridation	Reactive Sputtering	Acts as an adhesive/barrier layer for the aluminum and tungsten
Aluminum Deposition (M2)	Sputtering	Deposits conductive aluminum layer on the wafer surface
TiN AntiReflection Coating	Sputtering - ARC	Aids photoresist processing by eliminating standing waves
Metal2 Mask	**Shape = Clear**	**Defines Metal2 lines which remain protected from etching**
Metal2 Etch	Dry Etch	Removes unprotected metal2 leaving conducting lines
Resist Strip	Plasma-Strip	Removes resist masking the protected metal lines

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SEM of the Metal1-Metal2 Via

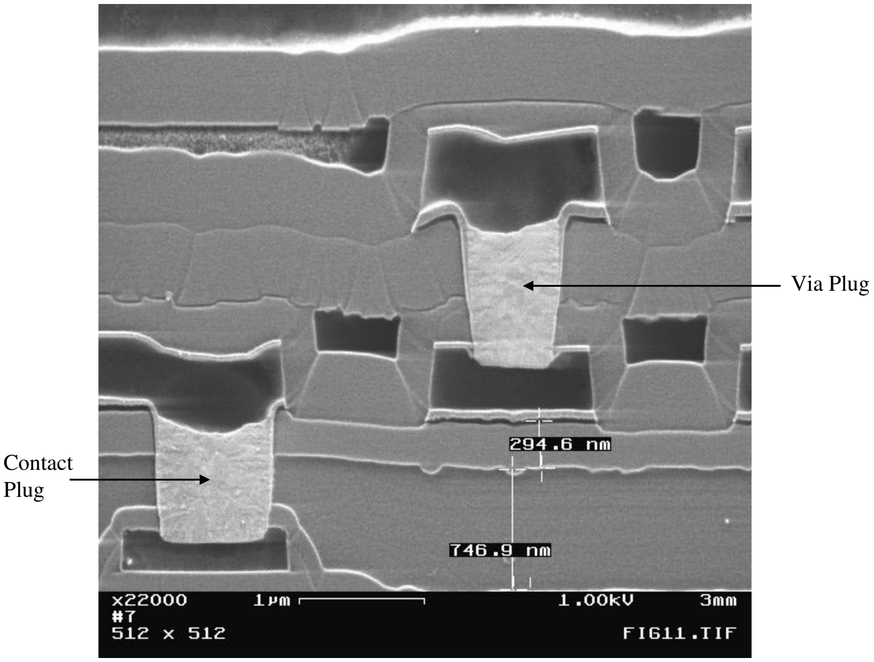


Fig.2.8-25

Metal2-Metal3 Vias

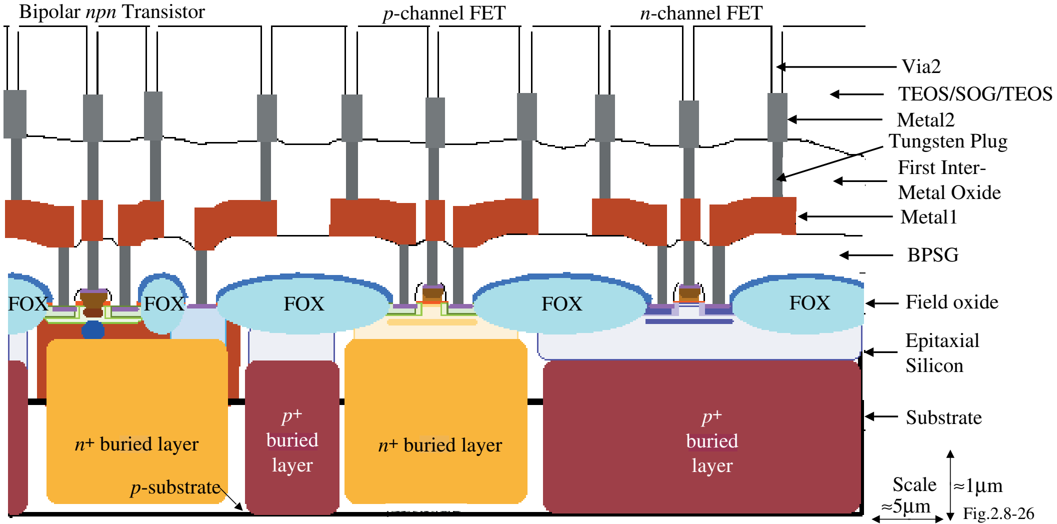


Fig.2.8-26

Process Step	Description	Reason
TEOS Deposition	LPCVD Oxide	Provides a good conformal coating, adhesion, and separation between Metal2 and SOG
Spin-On Glass (SOG)	Spin	Deposited as a viscous liquid, like resist, it provides a very planar dielectric
Anneal and Etchback	Etch	Flattens/planarizes high points and corners in the SOG to improve subsequent metal step-coverage
TEOS Deposition	LPCVD Oxide	Second coating provides a good conformal coating, adhesion and separation between SOG and metal3
Via2 Mask	**Shape = Dark**	**Defines vias by opening the resist over the via locations**
Via2 Etch	Dry Etch	Removes oxide in vias leaving openings in oxide to metal2
Resist Strip	Plasma-Strip	Removes resist masking the protected metal lines

---

Metal3

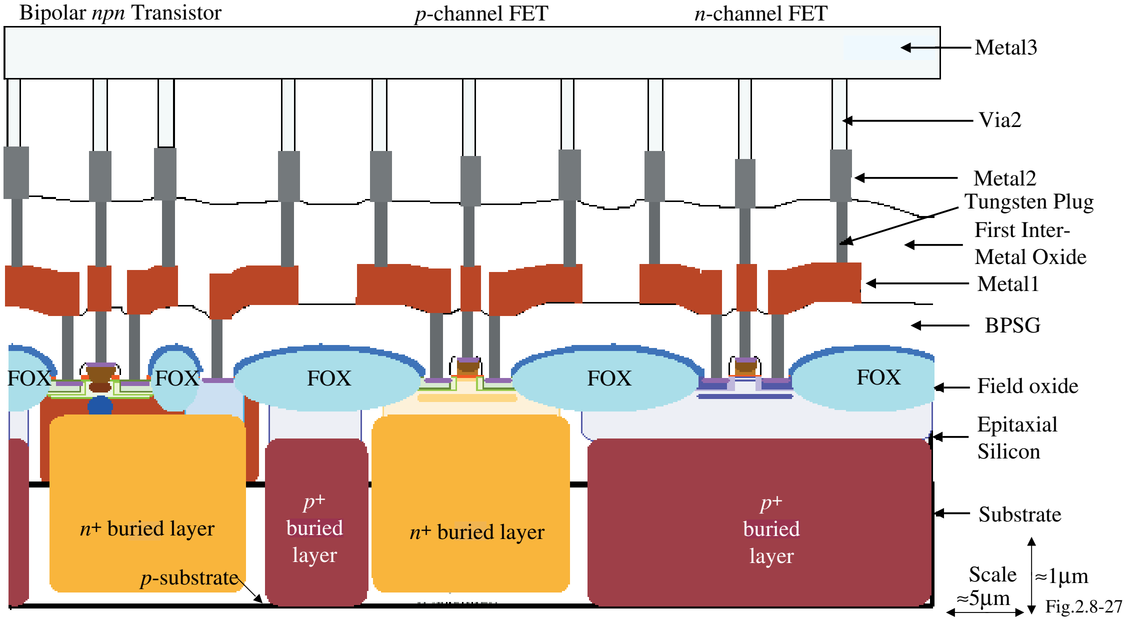


Fig.2.8-27

Process Step	Description	Reason
TiN Deposition/Nitridation	Reactive Sputtering	Acts as an adhesive layer for the aluminum metallization
Aluminum Deposition (M3)	Sputtering	Deposits conductive aluminum layer on the wafer surface
TiN ARC	Sputtering	Aids photoresist processing by eliminating standing waves

Metal3 and Bond Pad Openings

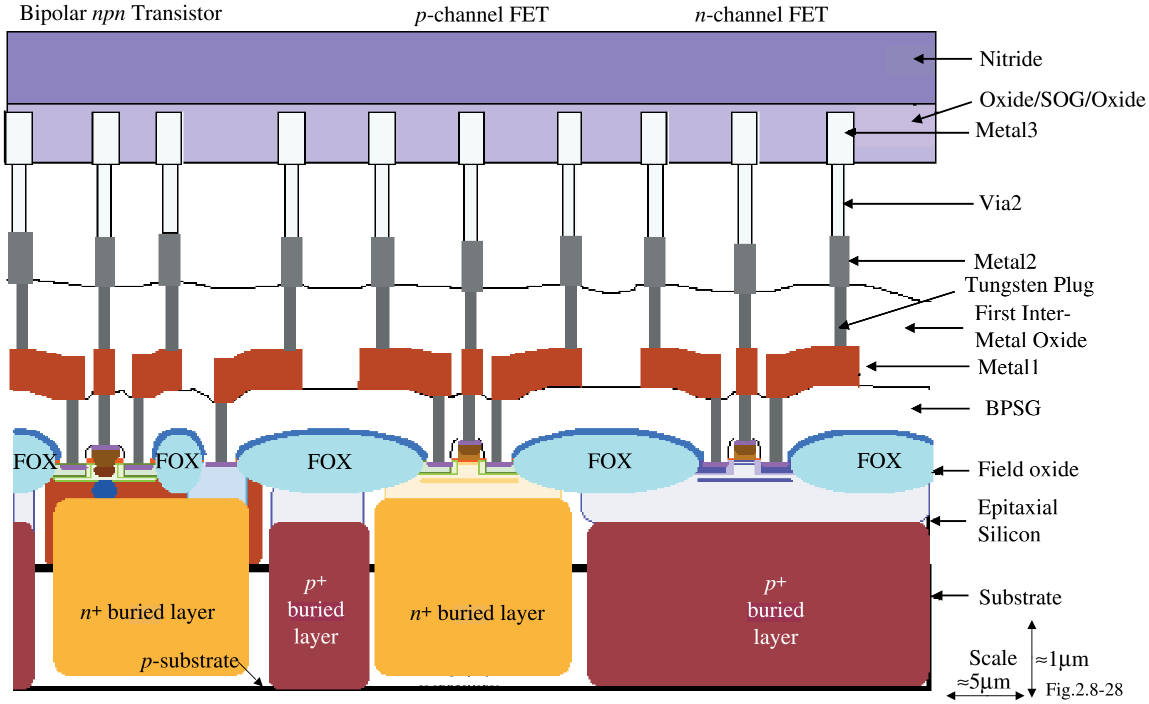


Fig.2.8-28

Metal3 and Bond Pad Openings - Continued

Process Step	Description	Reason
Metal3 Mask	**Shape = Clear**	**Defines Metal3 lines which remain protected from etching**
Metal3 Etch	Dry Etch	Removes Metal3 leaving conducting lines
Resist Strip	Plasma-Strip	Removes resist masking the protected metal lines
Oxide/SOG/Oxide Deposition	LPCVD/Spin/LPCVD	Stress relief between nitride and Metal3
Nitride Deposition	LPCVD	Barrier film protecting circuitry from moisture, hydrogen, etc.
Nitride Passivation Mask	**Shape = Dark**	**Defines the bond pads by opening resist over the pad locations**
Pad Etch	Dry Etch	Removes passivation over the bond pads for electrical contact
Resist Strip	Plasma-Strip	Removes resist masking the passivation

SEM of All Metal Levels and Vias

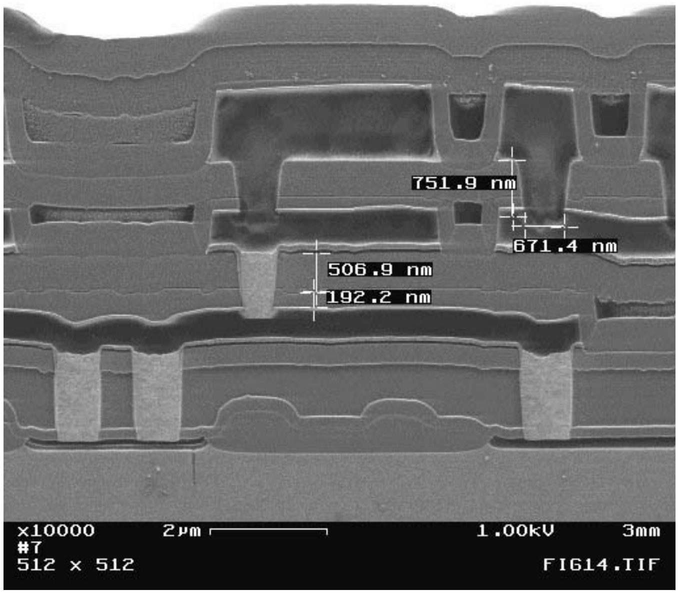


Fig.2.8-29

FURTHER CONSIDERATIONS ON PROCESSING

Dry Etching

Dry etching uses gases in a plasma state as the etch medium. A plasma etcher requires a chemical etchant and an energy sources as shown below.

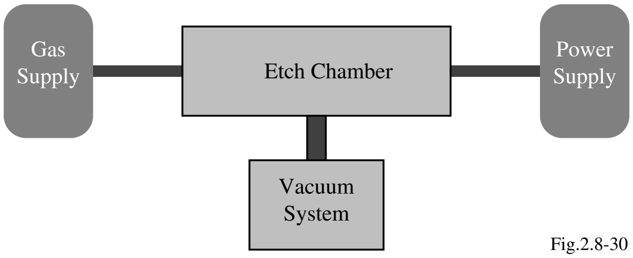

Gas Supply
Etch Chamber
Power Supply
Vacuum System

Fig.2.8-30

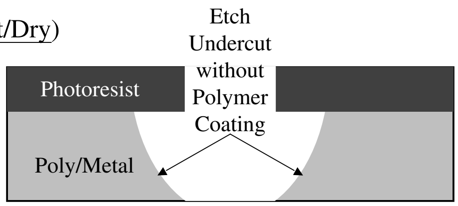
Operation:

- Load wafers in chamber
- Establish vacuum
- Fill chamber with reactive gases (reactant)
- Power supply creates a radio frequency field through electrodes in the chamber
- RF field energizes the gas mixture to a plasma state
- The energized reactive gases attack the material to be etched converting it into volatile components that are removed from the chamber by the vacuum system.

Anisotropic Dry Etching

Etch types:

Isotropic Etch (Wet/Dry)



Anisotropic Etch (Dry Only)

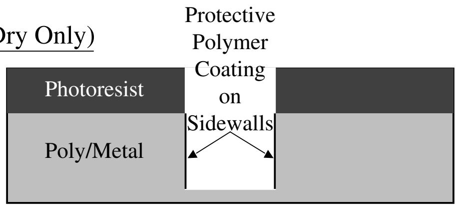


Fig.2.8-31

Operation of Anisotropic Etching:

- Starts with a vertically directed ionized etchant
- This etchant will also etch the protective photoresist layer which forms polymer residues in the vapor which redeposit on the sides of the material being etched.
- The redeposited polymer acts as a protective layer and prevents the etch from undercutting the photoresist.
- The success of this method requires that the photoresist and poly/metal etch rates are balanced and optimized over a broad range of pattern densities.

Problems with Anisotropic Dry Etching

1.) Insufficient redeposited polymer on the sidewalls.

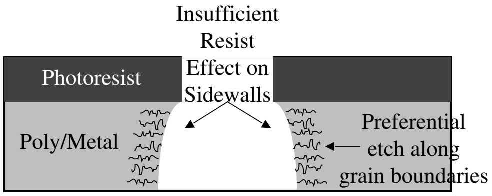


Fig.2.8-32

2.) Etch loading.

Etch loading is the influence of the amount of material to be etched on the etch rate. The smaller the amount of material to be etched, the faster the etch rate.

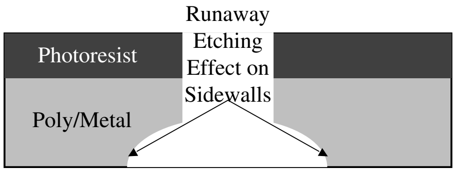


Fig.2.8-33

HALO/Pocket Implant

The purpose of this implant is to place an oppositely doped region, forming an abrupt junction, at the bottom of the S/D and channel edge of the lightly doped drain (LDD). The implant is performed at a high angle, generally between 45° to 60° while the wafer is rotated in order to implant under the gate, usually using the same mask as the LDD.

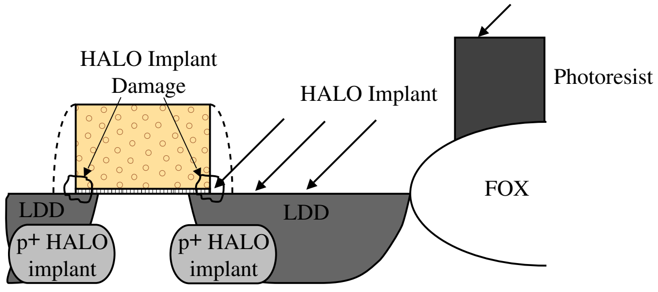


Fig.2.8-34

Comments:

- The heavier doping at the channel edge reduces the short channel effects (decreases λ)
- The heavier doping at the channel edge also reduces the drain induced barrier lowering (decreases λ)
- The HALO implant can damage the gate dielectric at the very edge of the FET's resulting in gate oxide leakage, hot carrier injection, increased interface traps and increased oxide trapped charge.
- Increases S/D capacitance only in a very localized region

SUMMARY

- This section has illustrated the major process steps for a 0.5micron BiCMOS technology.
- The performance of the active devices are:

  npn bipolar junction transistor:

  $f_T = 12\text{GHz}$, $\beta_F = 100\text{-}140$ $BV_{CEO} = 7\text{V}$

  n-channel FET:

  $K' = 127\mu\text{A/V}^2$ $V_T = 0.64\text{V}$ $\lambda_N \approx 0.060$

  p-channel FET:

  $K' = 34\mu\text{A/V}^2$ $V_T = -0.63\text{V}$ $\lambda_P \approx 0.072$

- Although today's state of the art is 0.35µm or 0.25µm BiCMOS, the processing steps illustrated above approximate that which is done in smaller technology.

SECTION 2.9 - SUMMARY

- Basic fabrication processes include:
    - Oxide growth
    - Thermal diffusion
    - Ion Implantation
    - Deposition
    - Etching
- PN junctions are used to electrically isolate regions in CMOS
- A simple CMOS technology requires about 8 masks
- Bipolar technology provides a good vertical NPN and reasonable lateral and substrate PNPs
- BiCMOS combines the best of both BJT and CMOS technologies
- Passive component compatible with CMOS technology include:
    - Capacitors - MOS, poly-poly, metal-metal, etc.
    - Resistors - Diffused, implanted, well, etc.
    - Inductors - Planar good only at very high frequencies
- CMOS technology has a reasonably good lateral BJT
- Other considerations in CMOS technology include:
    - Latch-up
    - ESD protection
    - Temperature influence
    - Noise influence
- Design rules are used to preserve the integrity of the technology