

## LECTURE 400 – OVERSAMPLING ADCS – PART II

### LECTURE ORGANIZATION

#### Outline

- Implementation of  $\Delta\Sigma$  modulators
- Decimation and filtering
- Bandpass  $\Delta\Sigma$  modulators
- Digital-analog oversampling converters
- Summary

***CMOS Analog Circuit Design, 2<sup>nd</sup> Edition Reference***

Pages 705-715

### IMPLEMENTATION OF $\Delta\Sigma$ MODULATORS

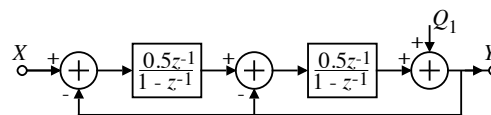
#### $\Delta\Sigma$ Modulators – The Analog Part of the Oversampling ADC

Most of today's delta-sigma modulators use fully differential switched capacitor circuits.

Advantages are:

- Doubles the signal swing and increases the dynamic range by 6dB
- Common-mode signals that may couple to the signal through the supply lines and substrate are canceled
- Charge injected by the switches are canceled to a first-order

Example:



First integrator dissipates the most power and requires the most accuracy.

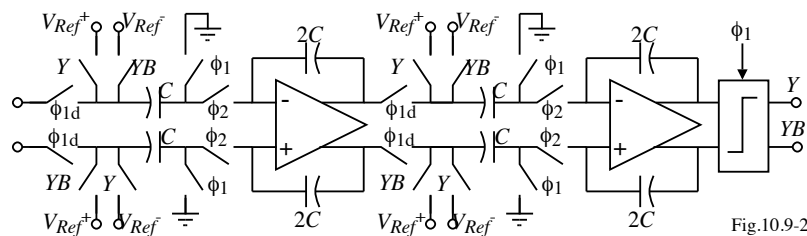


Fig.10.9-24

## 1.5V, 1mW, 98db $\Delta\Sigma$ Analog-Digital Converter<sup>†</sup>

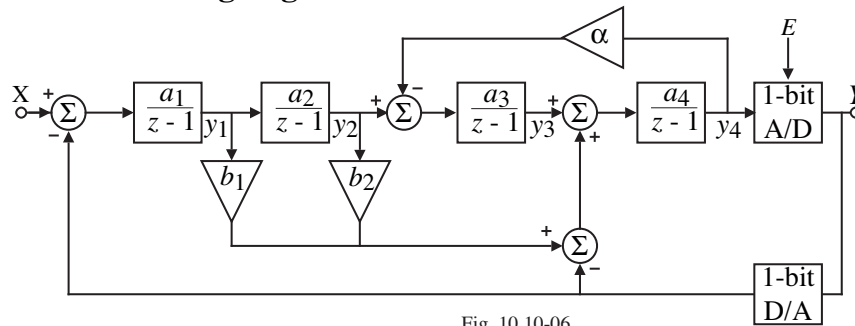


Fig. 10.10-06

where  $a_1 = 1/3$ ,  $a_2 = 3/25$ ,  $a_3 = 1/10$ ,  $a_4 = 1/10$ ,  $b_1 = 6/5$ ,  $b_2 = 1$  and  $\alpha = 1/6$

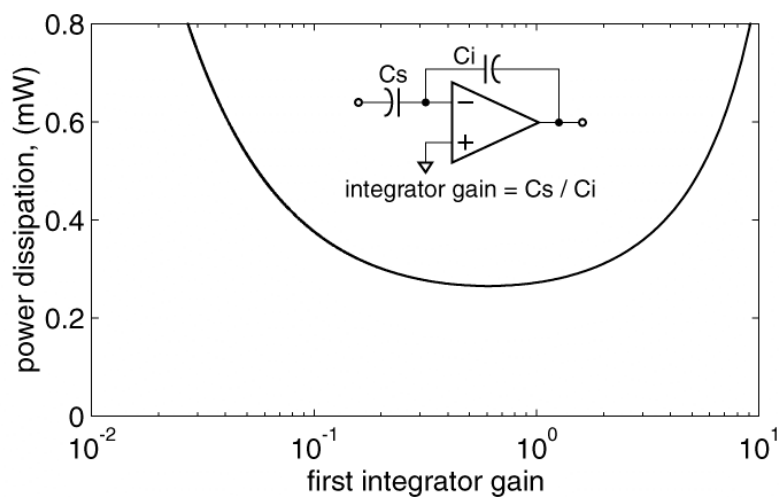
Advantages:

- The modulator combines the advantages of both DFB and DFF type modulators: Only four op amps are required. The 1st integrator's output swing is between  $\pm V_{REF}$  for large input signal amplitudes ( $0.6V_{REF}$ ), even if the integrator gain is large (0.5).
- A local resonator is formed by the feedback around the last two integrators to further suppress the quantization noise.
- The modulator is fully pipelined for fast settling.

<sup>†</sup> A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio  $\Delta\Sigma$  Modulator with 98dB Dynamic Range," *Proc. of 1999 Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 50-51.  
CMOS Analog Circuit Design

## 1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

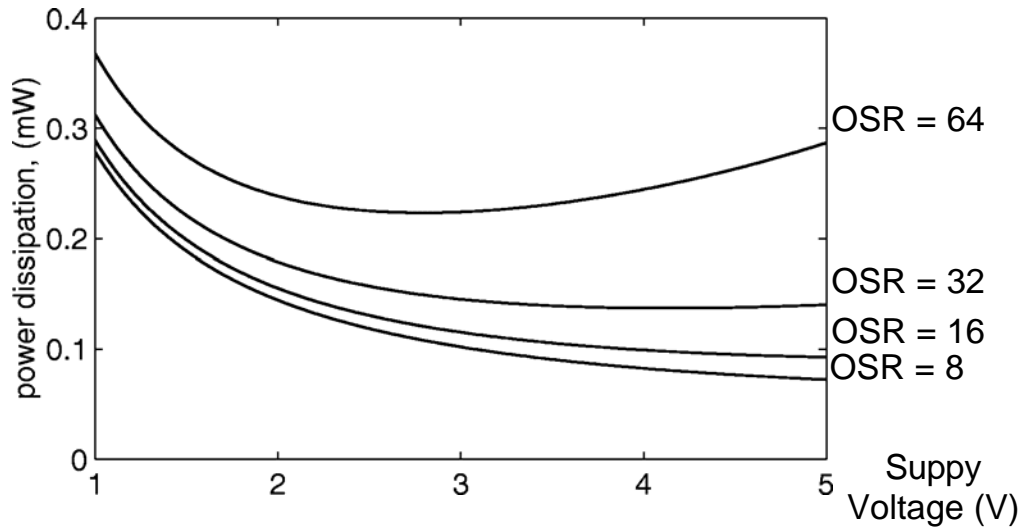
Integrator power dissipation vs. integrator gain



$DR = 98$  dB  
 $BW = 20$  kHz  
 $C_S = 5$  pF  
 $0.5 \mu\text{m}$  CMOS

### 1.5V, 1mW, 98db ΔΣ Analog-Digital Converter - Continued

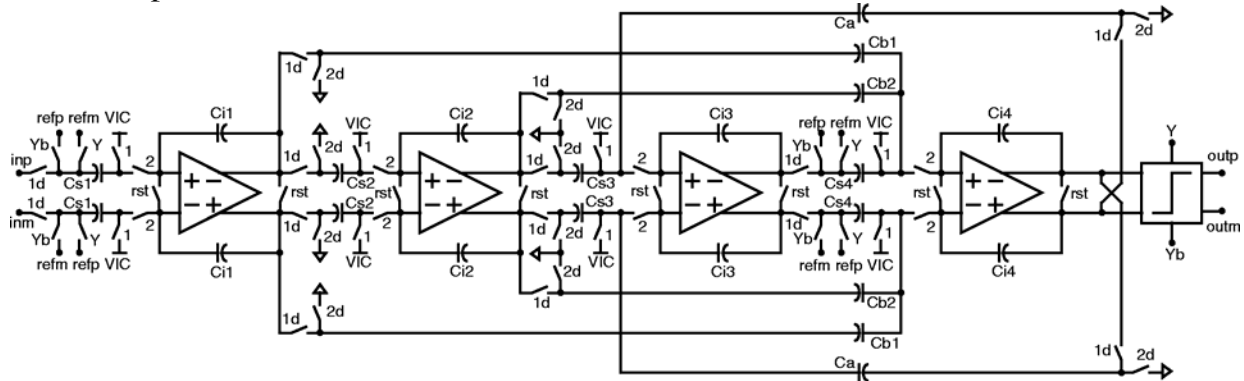
Modulator power dissipation vs. oversampling ratio



$DR = 98 \text{ dB}$   
 $BW = 20 \text{ kHz}$   
 Integrator gain = 1/3  
 0.5μm CMOS

### 1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Circuit Implementation:



Capacitor Values				
Capacitor	Integrator 1	Integrator 2	Integrator 3	Integrator 4
$C_s$	5.00pF	0.15pF	0.30pF	0.10pF
$C_i$	15.00pF	1.25pF	3.00pF	1.00pF
$C_a$	-	-	0.05pF	-
$C_{b1}$	-	-	-	0.12pF
$C_{b2}$	-	-	-	0.10pF

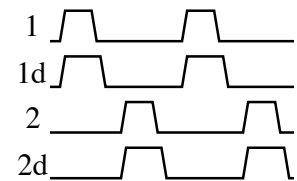
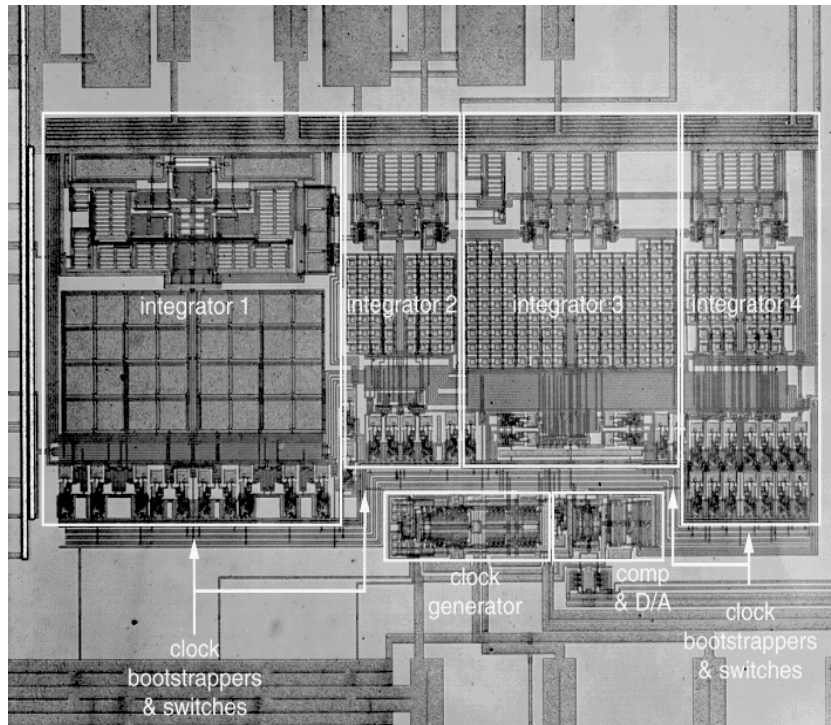


Fig.10.9-25

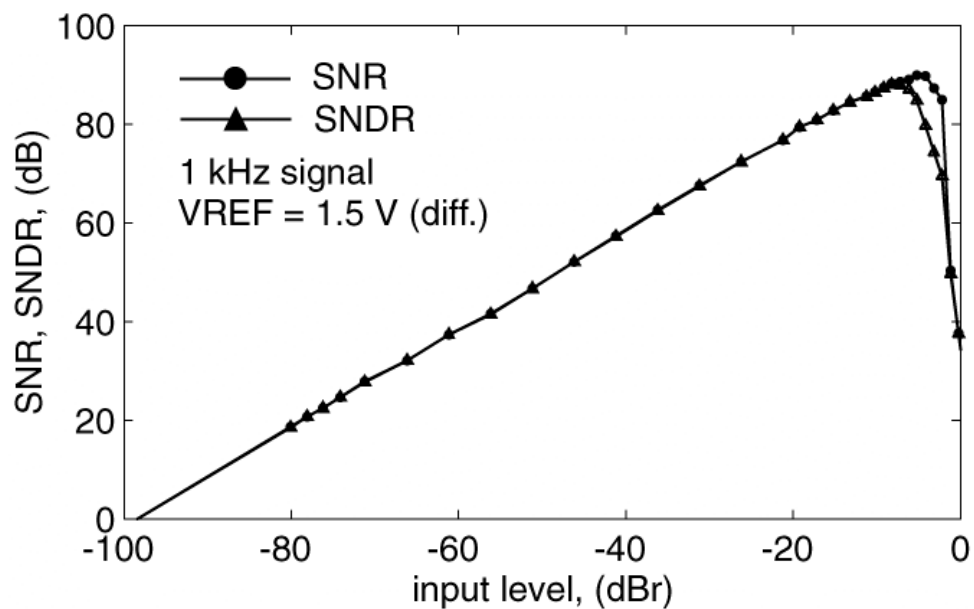
## 1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Microphotograph of the  $\Delta\Sigma$  modulator.



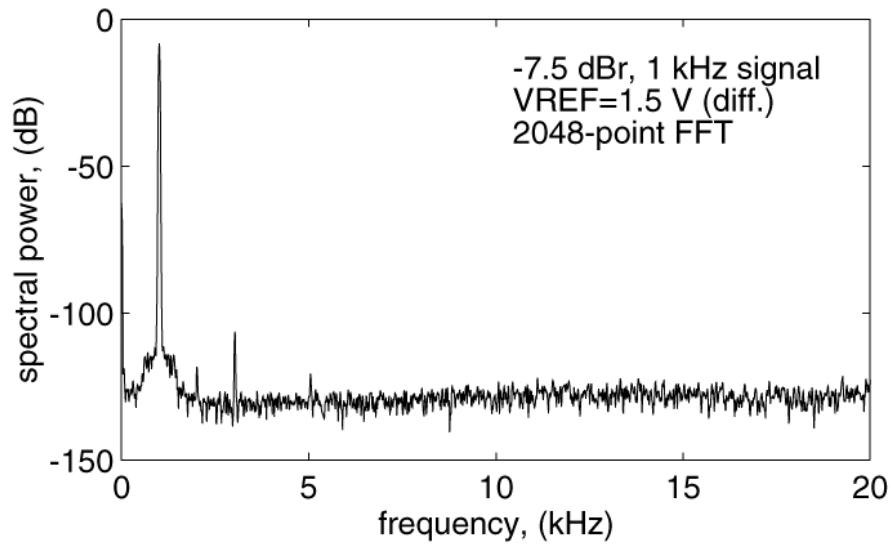
## 1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured SNR and SNDR versus input level of the modulator.

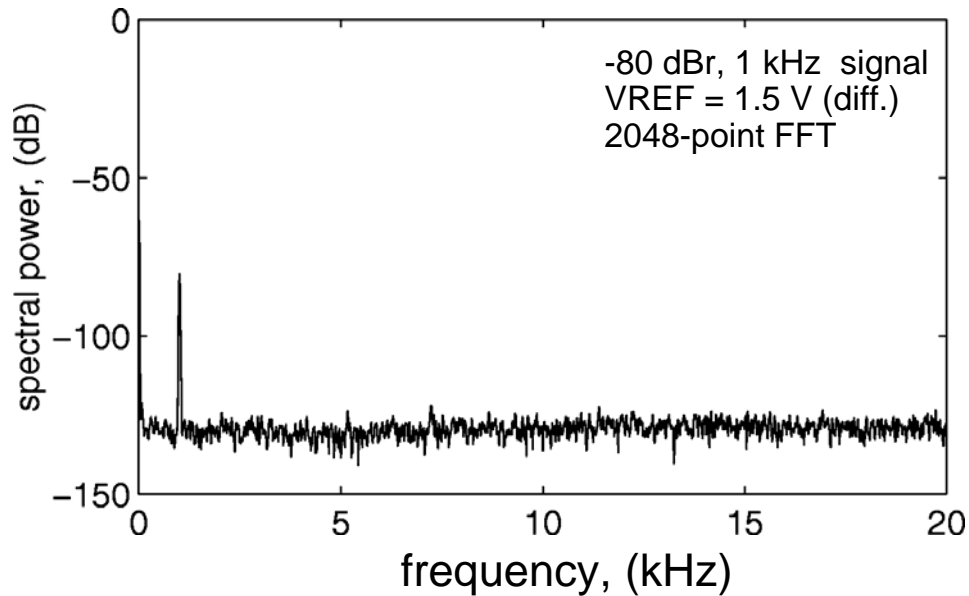


**1.5V, 1mW, 98dB  $\Delta\Sigma$  Analog-Digital Converter - Continued**

Measured baseband spectrum for a -7.5dBr 1kHz input.

**1.5V, 1mW, 98dB  $\Delta\Sigma$  Analog-Digital Converter - Continued**

Measured baseband spectrum for a -80dBr 1kHz input.



## 1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

### Measured 4th-Order $\Delta\Sigma$ Modulator Characteristics:

Table 5.4

Measured fourth-order delta-sigma modulator characteristics	
Technology : 0.5 $\mu\text{m}$ triple-metal single-poly n-well CMOS process	
Supply voltage	1.5 V
Die area	1.02 mm x 0.52 mm
Supply current	660 $\mu\text{A}$
analog part	630 $\mu\text{A}$
digital part	30 $\mu\text{A}$
Reference voltage	0.75V
Clock frequency	2.8224MHz
Oversampling ratio	64
Signal bandwidth	20kHz
Peak SNR	89 dB
Peak SNDR	87 dB
Peak S/D	101dB
HD <sub>3</sub> @ -5dBv 2kHz input	-105dBv
DR	98 dB

## DECIMATION AND FILTERING

### Delta-Sigma ADC Block Diagram

The decimator and filter are implemented digitally and consume most of the area and the power.

Function of the decimator and filter are;

- 1.) To attenuate the quantization noise above the baseband
- 2.) Bandlimit the input signal
- 3.) Suppress out-of-band spurious signals and circuit noise

Most of the  $\Delta\Sigma$  ADC applications demand decimation filters with linear phase characteristics leading to the use of finite impulse response (FIR) filters.

FIR filters:

For a specified ripple and attenuation,

$$\text{Number of filter coefficients} \propto \frac{f_s}{f_t}$$

where  $f_s$  is the input rate to the filter (clock frequency of the quantizer) and  $f_t$  is the transition bandwidth.

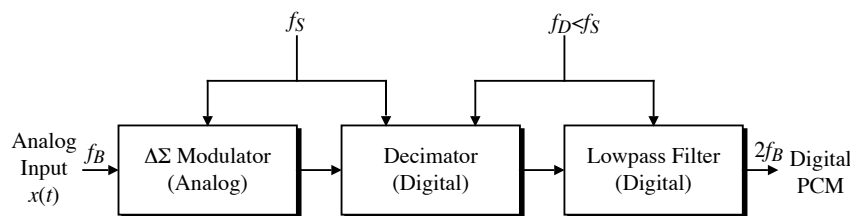


Fig.10.9-07

## A Multi-Stage Decimation Filter

To reduce the number of stages, the decimation filters are implemented in several stages. Typical multi-stage decimation filter:

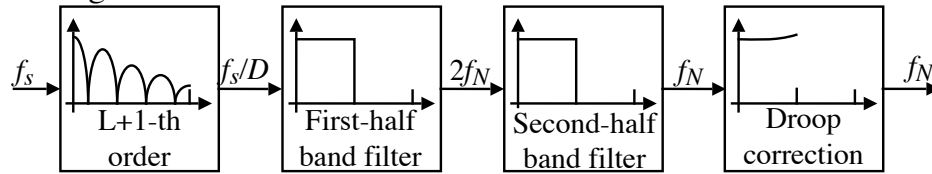


Fig.10.9-26

- 1.) For  $\Delta\Sigma$  modulators with  $(1-z^{-1})^L$  noise shaping comb filters are very efficient.
  - Comb filters are suitable for reducing the sampling rate to four times the Nyquist rate.
  - Designed to suppress the quantization noise that would otherwise alias into the signal band upon sampling at an intermediate rate of  $f_{s1}$ .
- 2.) The remaining filtering is performed in stages by FIR or IIR filters.
  - Suppresses out-of-band components of the signal
- 3.) Droop correction - may be required depending upon the ADC specifications

## Comb Filters

A comb filter that computes a running average of the last  $D$  input samples is given as

$$y[n] = \frac{1}{D} \sum_{i=0}^{D-1} x[n-i]$$

where  $D$  is the decimation factor given as

$$D = \frac{f_s}{f_{s1}}$$

The corresponding  $z$ -domain expression is,

$$H_D(z) = \sum_{i=1}^D z^{-i} = \frac{1}{D} \frac{1 - z^{-D}}{1 - z^{-1}}$$

The frequency response is obtained by evaluating  $H_D(z)$  for  $z = e^{j2\pi f T_s}$ ,

$$H_D(f) = \frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} e^{-j2\pi f T_s / D}$$

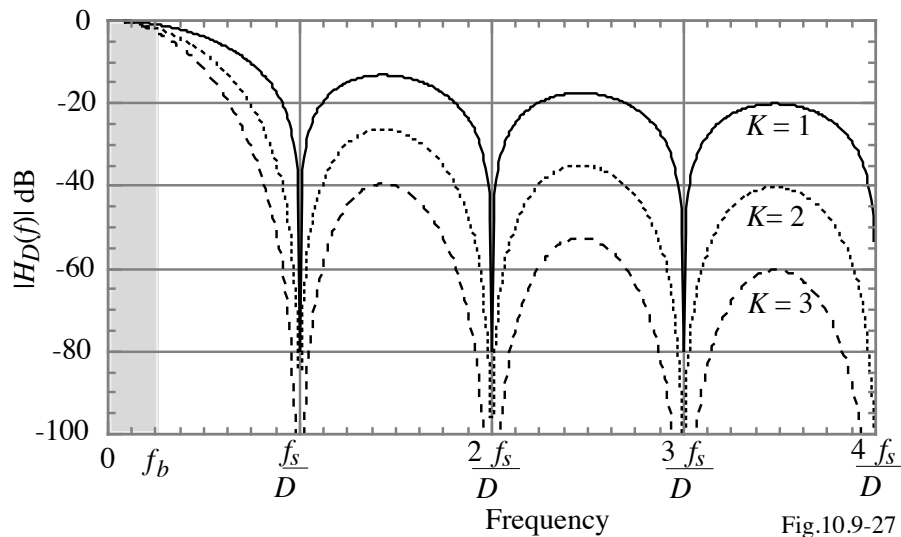
where  $T_s$  is the input sampling period ( $=1/f_s$ ). Note that the phase response is linear.

For an  $L$ -th order modulator with a noise shaping function of  $(1-z^{-1})^L$ , the required number of comb filter stages is  $L+1$ . The magnitude of such a filter is,

$$|H_D(f)| = \left( \frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} \right) K$$

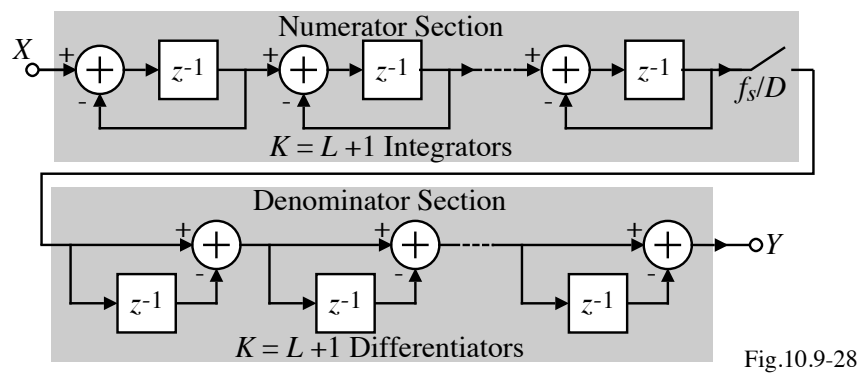
## Magnitude Response of a Cascaded Comb Filter

$K = 1, 2$  and  $3$



## Implementation of a Cascaded Comb Filter

Implementation:



Comments:

- 1.) The  $L+1$  integrators operating at the sampling frequency,  $f_s$ , realize the denominator of  $H_D(z)$ .
- 2.) The  $L+1$  differentiators operating at the output rate of  $f_{s1} (= f_s/D)$  realize the numerator of  $H_D(z)$ .
- 3.) Placing the integrator delays in the feedforward path reduces the critical path from  $L+1$  adder delays to a single adder delay.

## Implementation of Digital Filters<sup>†</sup>

Digital filter structures:

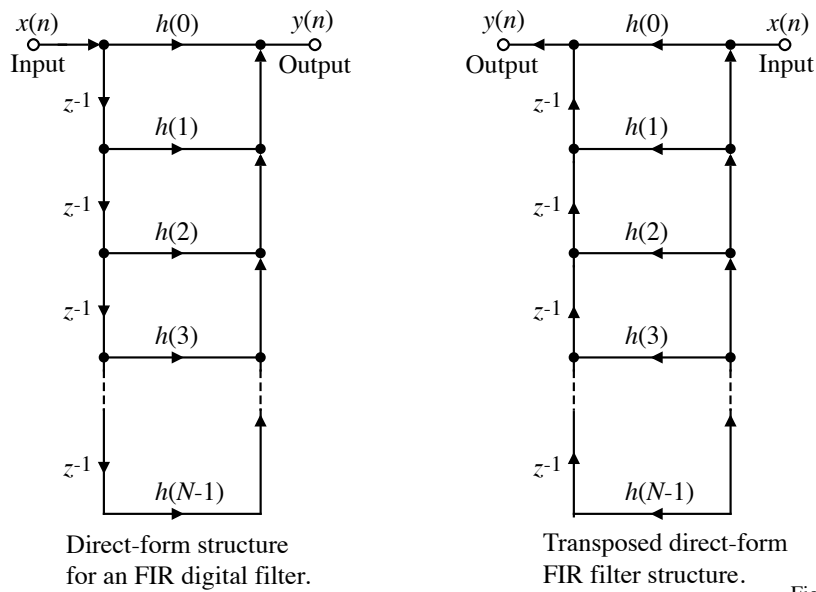
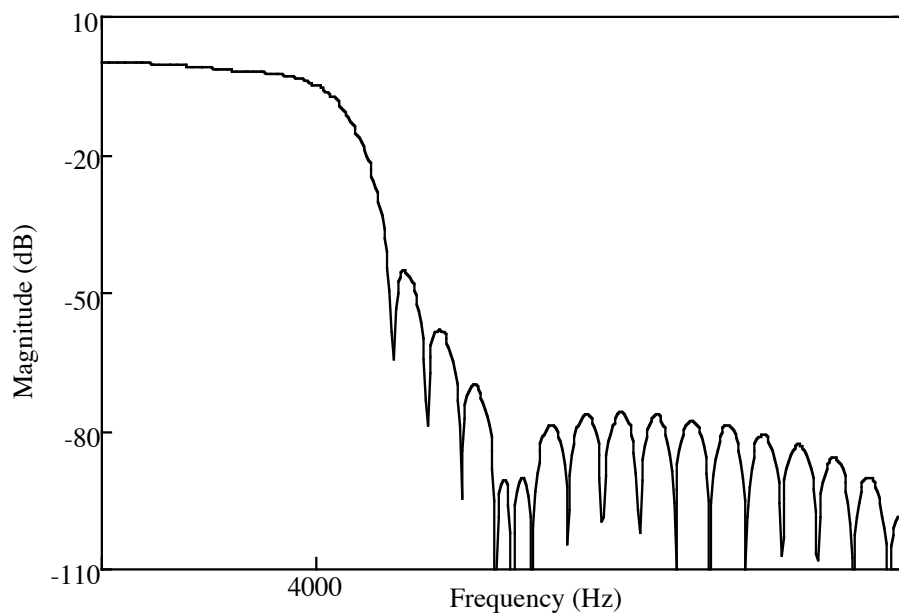


Fig.10.9-29

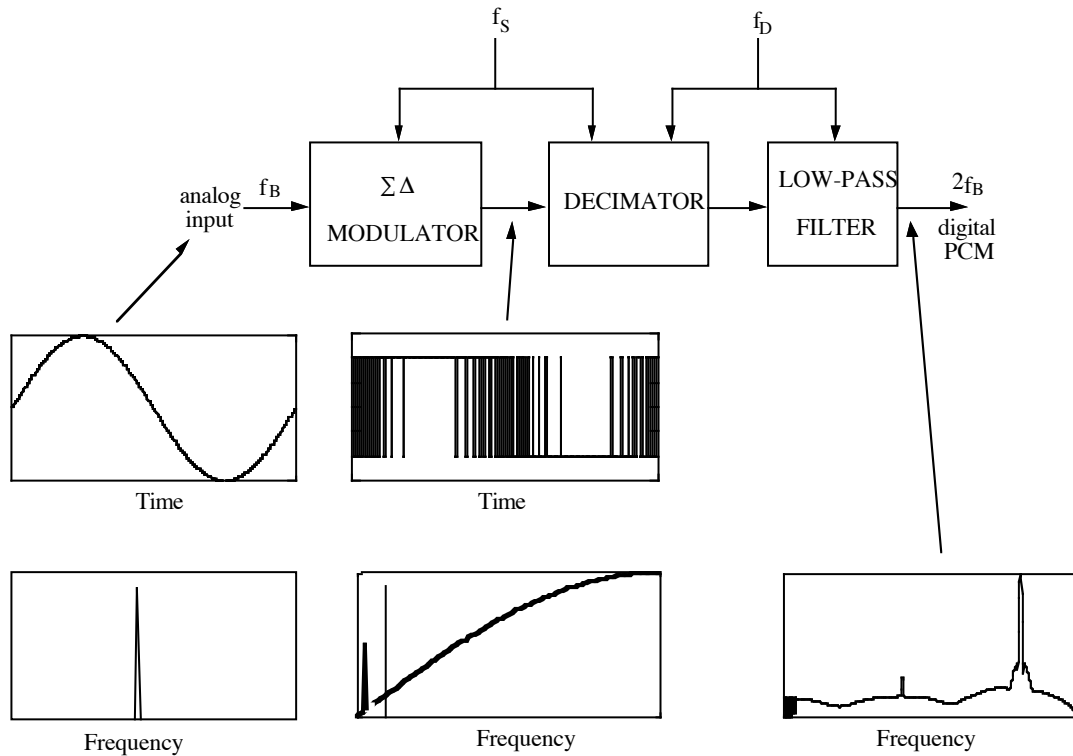
<sup>†</sup> S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters-Theory, Design, and Simulation*, IEEE Press, NY, Chapter 13, 1997.  
 CMOS Analog Circuit Design © P.E. Allen - 2010

## Digital Lowpass Filter

Example of a typical digital filter used in removal of the quantization noise at higher frequencies



### Illustration of the Delta-Sigma ADC in Time and Frequency Domain



### BANDPASS DELTA-SIGMA MODULATORS

#### Bandpass ΔΣ Modulators

Block diagram of a bandpass modulator:

Components:

- Resonator - a bandpass filter of order  $2N, N= 1, 2, \dots$
- Coarse quantizer (1 bit or multi-bit)

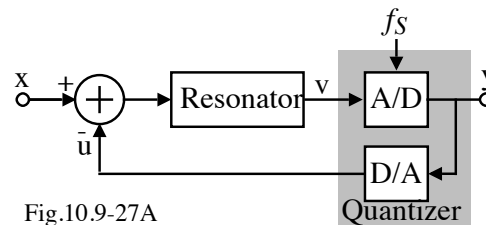


Fig.10.9-27A

The noise-shaping of the bandpass oversampled ADC has the following interesting characteristics:

$$\text{Center frequency} = f_s \cdot (2N-1)/4$$

$$\text{Bandwidth} = \text{BW} = f_s / M$$

Illustration of the Frequency Spectrum ( $N=1$ ):

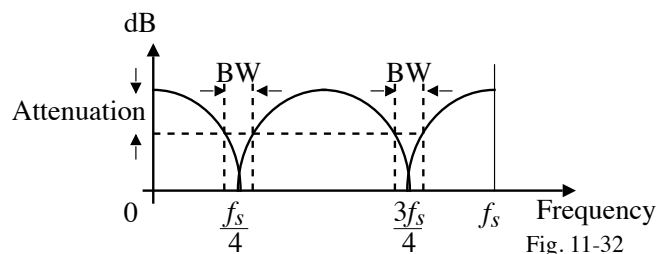


Fig. 11-32

Application of the bandpass ΔΣ ADC is for systems with narrowband signals (IF frequencies)

### A First-Order $\Delta\Sigma$ Bandpass Modulator

Bandpass Resonator:

$$V(z) = z^{-1} [X(z) - z^{-1}V(z)] = z^{-1}X(z) - z^{-2}V(z)$$

$$V(z) (1+z^{-2}) = z^{-1}X(z) \rightarrow \frac{V(z)}{X(z)} = \frac{z^{-1}}{1+z^{-2}}$$

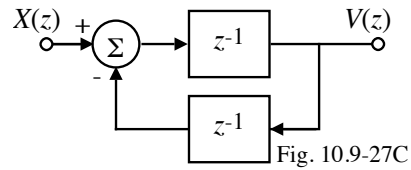


Fig. 10.9-27C

Modulator:

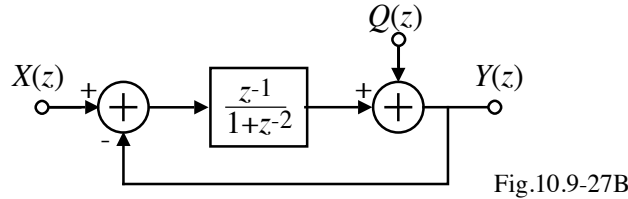


Fig.10.9-27B

$$Y(z) = Q(z) + [X(z) - Y(z)] \left( \frac{z^{-1}}{1+z^{-2}} \right) \rightarrow$$

$$Y(z) = \left( \frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right) Q(z) + \left( \frac{z^{-1}}{1+z^{-1}-z^{-2}} \right) X(z)$$

$$NTF_Q(z) = \left( \frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right)$$

The  $NTF_Q(z)$  has two zeros on the  $j\omega$  axis.

### Resonator Design

Resonators can be designed by applying a lowpass to bandpass transform as follows:

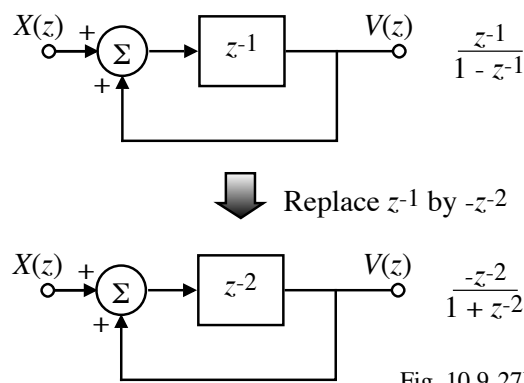


Fig. 10.9-27D

Result:

- Simple way to design the resonator
- Inherits the stability of a lowpass modulator
- Center frequency located at  $f_s/4$

## Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Block diagram:

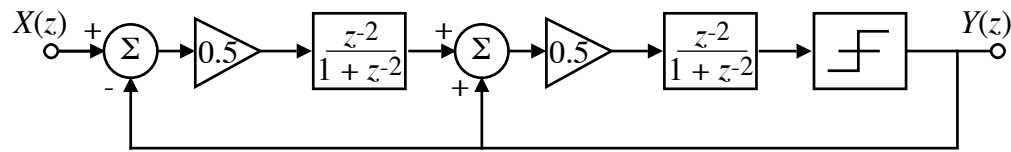


Fig. 10.9-27E

Comments:

- Designed by applying a lowpass to bandpass transform to a second-order lowpass  $\Delta\Sigma$  modulator
- The stability and SNR characteristics are the same as those of a second-order lowpass modulator
- The  $z$ -domain output is given as,
 
$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2Q(z)$$
- The zeros are located at  $z = \pm j$  which corresponds to notches at  $f_s/4$ .

## Resonator Circuit Implementation

Block diagram of  $z^{-2}/(1+z^{-2})$ :

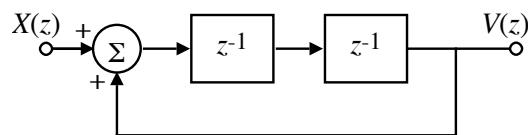


Fig. 10.9-27F

Fully differential switch-capacitor implementation:

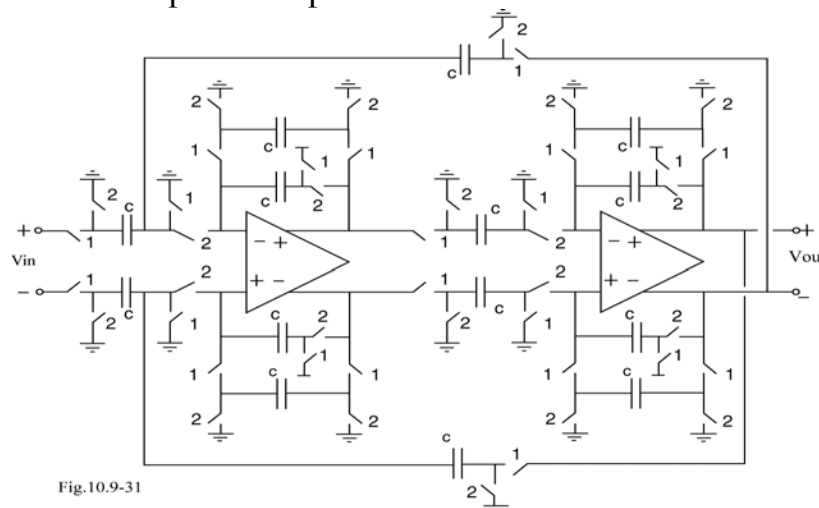
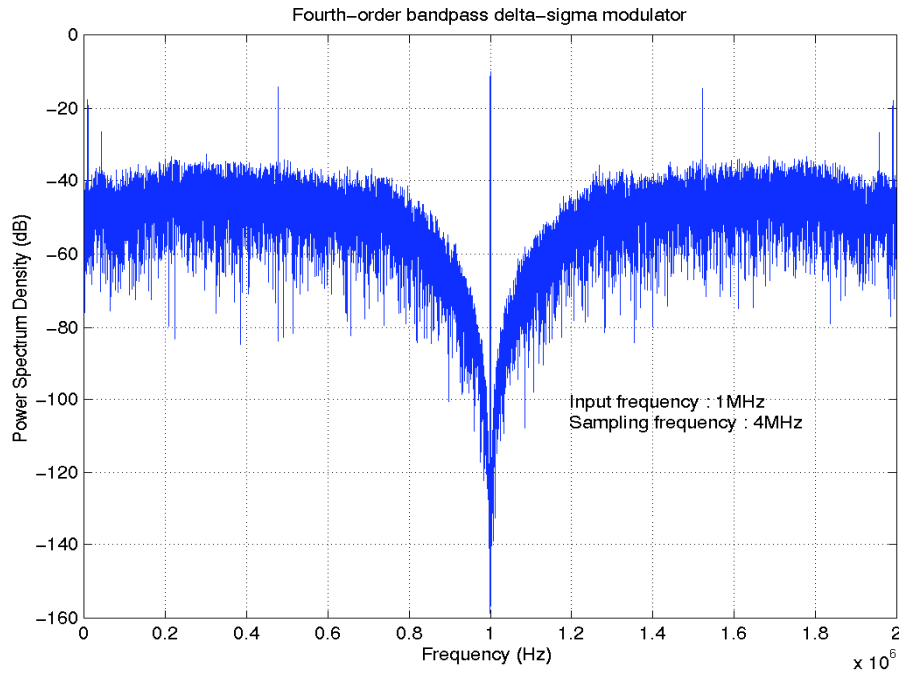


Fig. 10.9-31

## Power Spectral Density of the Previous Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Simulated result:



## DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTERS

### Principles

The principles of oversampling and noise shaping are also widely used in the implementation of  $\Delta\Sigma$  DACs.

Simplified block diagram of a delta-sigma DAC:

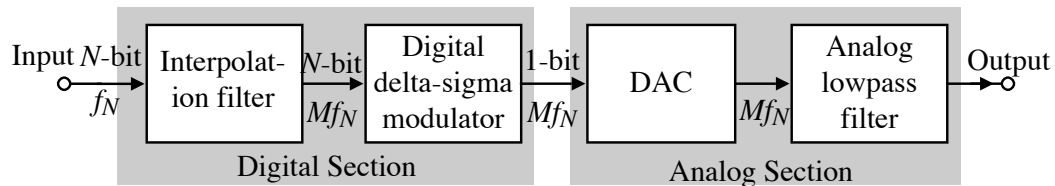


Fig10.9-29

Operation:

- 1.) A digital signal with  $N$ -bits with a data rate of  $f_N$  is sampled at a higher rate of  $Mf_N$  by means of an interpolator.
- 2.) Interpolation is achieved by inserting “0”s between each input word with a rate of  $Mf_N$  and then filtering with a lowpass filter.
- 3.) The MSB of the digital filter is applied to a DAC which is applied to an analog lowpass filter to achieve the analog output.

## Block Diagram of a $\Delta\Sigma$ DAC

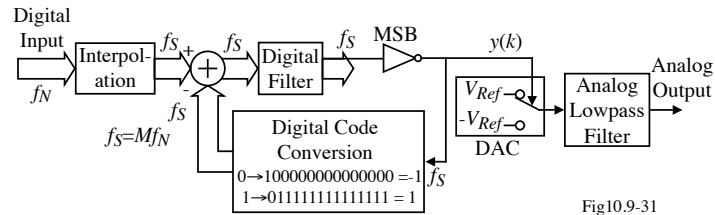


Fig10.9-31

Operation:

- 1.) Interpolate a digital word at the conversion rate of the converter ( $f_N$ ) up to the sample frequency,  $f_s$ .
- 2.) The word length is then reduced to one bit with a digital sigma-delta modulator.
- 3.) The one bit PDM signal is converted to an analog signal by switching between two reference voltages.
- 4.) The high-frequency quantization noise is removed with an analog lowpass filter yielding the required analog output signal.

Sources of error:

- Device mismatch (causes harmonic distortion rather than DNL or INL)
- Component noise
- Device nonlinearities
- Clock jitter sensitivity
- Inband quantization error from the  $\Delta$ - $\Sigma$  modulator

## Frequency Viewpoint of the $\Delta\Sigma$ DAC

Frequency spectra at different points of the delta-sigma ADC:

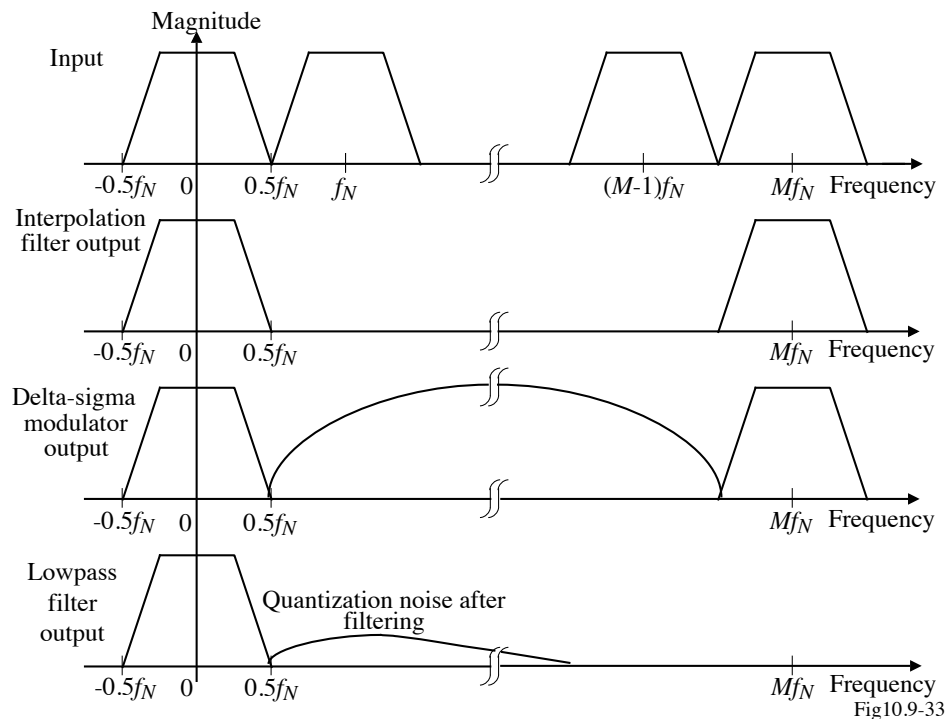
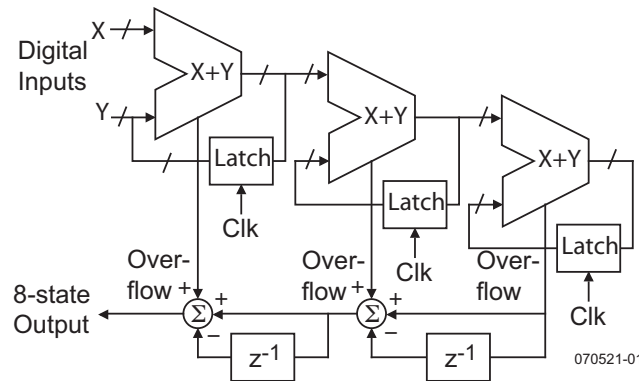


Fig10.9-33

### A Third-Order, $\Delta\Sigma$ Modulator for a DAC

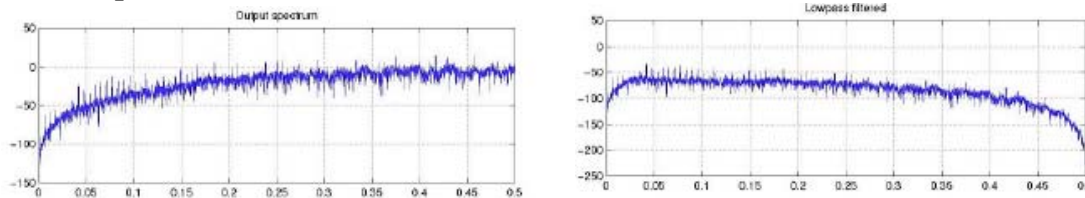
A digital equivalent of the third-order MASH  $\Delta\Sigma$  modulator is shown below.



The  $m$ -bit accumulators consist of an  $m$ -bit adder and  $m$ -bit latches.

The 8-state digital output is converted to an analog through means of an analog filter.

Spectral outputs:



### 1-Bit DAC for the $\Delta\Sigma$ Digital-to-Analog Converter - The Analog Part

The MSB output from the digital filter is used to drive a 1-bit DAC.

Possible architectures:

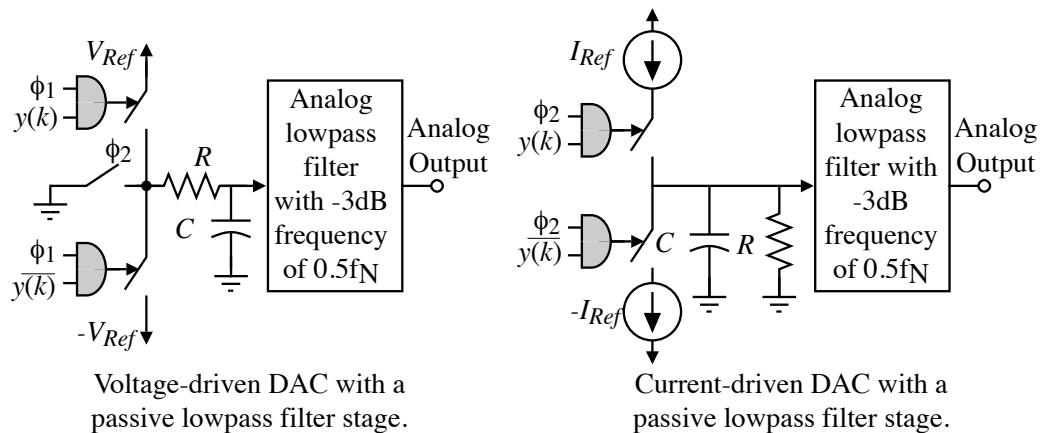


Fig10.9-32

A multi-bit output would consist of more parallel, controlled current sources and sinks.

## Switched-Capacitor DAC and Filter

Typically, the DAC and the first stage of the lowpass filter are implemented using switched-capacitor techniques.

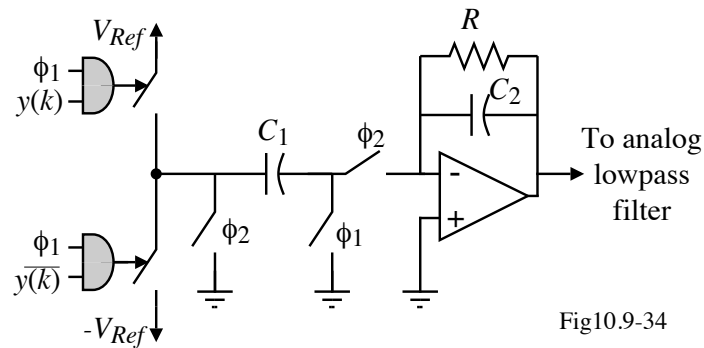


Fig10.9-34

It is necessary to follow the switched-capacitor filter by a continuous time lowpass filter to provide the necessary attenuation of the quantization noise.

## SUMMARY

### Comparison of the Various Types of ADCs

A/D Converter Type	Maximum Practical Number of Bits ( $\pm 1$ )	Speed (Expressed in terms of $T$ a clock period)	Area Dependence on the number of bits, $N$ , or other ADC parameters
Dual Slope	12-14 bits	$2(2NT)$	Independent
Successive Approximation with self-correction	12-15 bits	$NT$	$\propto N$
1-Bit Pipeline	10 bits	$T$ (After $NT$ delay )	$\propto N$
Algorithmic	12 bits	$NT$	Independent
Flash	6 bits	$T$	$\propto 2^N$
Two-step, flash	10-12 bits	$2T$	$\propto 2^{N/2}$
Multiple-bit, M-pipe	12-14 bits	$MT$	$\propto 2^{N/M}$
$\Delta$ - $\Sigma$ Oversampled (1-bit, $L$ loops and $M$ = oversampling ratio = $f_{\text{clock}}/2f_b$ )	15-17 bits	$MT$	$\propto L$

### Comparison of Recent ADCs

Resolution versus conversion rate:

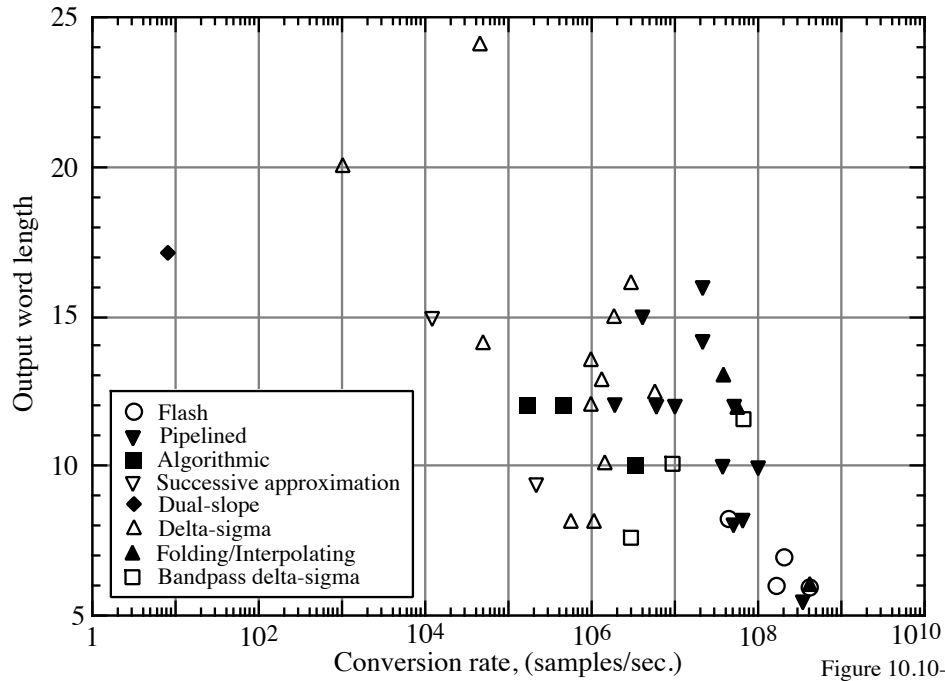


Figure 10.10-1

### Comparison of Recent ADCs - Continued

Power dissipation versus conversion rate:

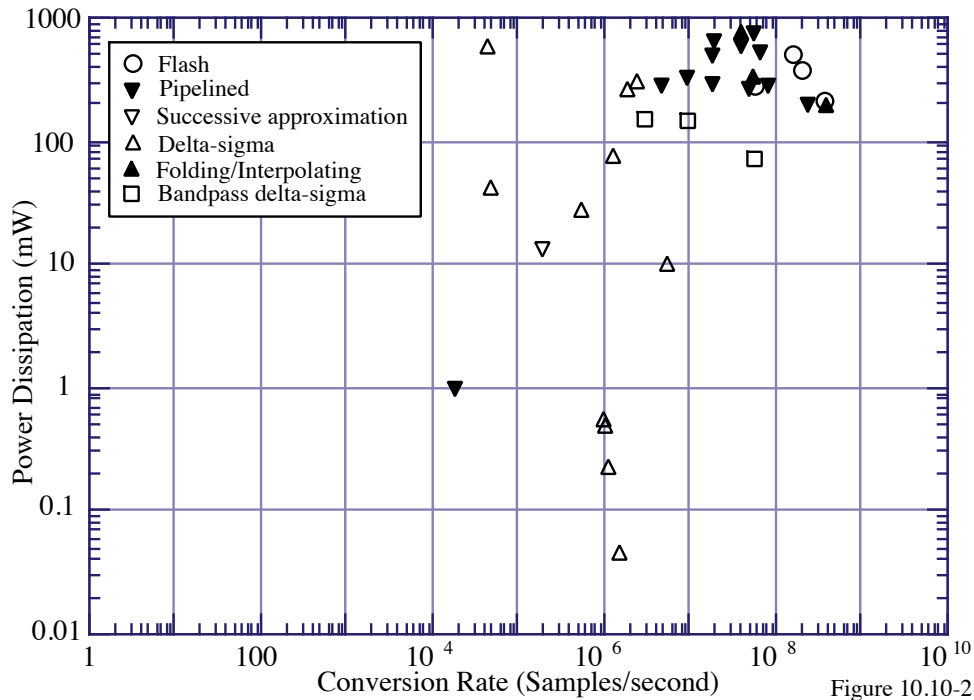


Figure 10.10-2

## References for Previous Figures

- [1] A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC. *Vorenkamp, P.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1876-1886
- [2] A 15-b, 5-Msample/s Low-Spurious CMOS ADC. *Kwak, S. -U.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1866-1875
- [3] Error Suppressing Encode Logic of FCDL in a 6-b Flash A/D Converter. *Ono, K.*, IEEE J-SC, vol. 32, no.9, Sep 97 1460-1464
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- [8] A DSP-Based Hearing Instrument IC. *Neuteboom, H.*, IEEE J-SC, vol. 32, no. 11, Nov 97 1790-1806
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- [11] Quadrature Bandpass  $\Delta\Sigma$  Modulation for Digital Radio. *Jantzi, S. A.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1935-1950
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## CONCLUDING THOUGHTS

- What is analog circuit design?

*The complex process of creating circuit solutions using analog circuit techniques.*

- What is the analog integrated circuit design process?

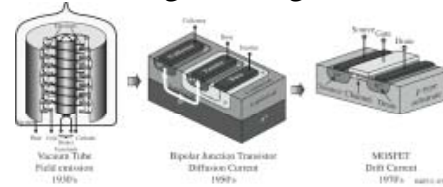
*The even more complex process of combining analog design with IC technology which includes electrical, physical and test design.*

- What are the key principles, concepts and techniques for analog IC design?

*Key principles – Fundamental laws*

*Key concepts – Important relationships and ideas*

*Key techniques – Tools that allow simplification or insight*



Technology changes but principles, concepts and techniques remain the same.

- How can the analog IC designer enhance creativity and solve new problems in today's industrial environment?

*Learn the key principles, concepts and techniques of analog circuit design*

*Learn from mistakes*

*Learn the technology*

*Always try to understand the concept and operation*

*of the circuit, never rely on a computer or someone else for this understanding*

