CHAPTER 7 – HIGH PERFORMANCE CMOS OP AMPS

INTRODUCTION

Chapter Outline
7.1 Buffered Op Amps
7.2 High-Speed/Frequency Op Amps
7.3 Differential Output Op Amps
7.4 Micropower Op Amp
7.5 Low-Noise Op Amps
7.6 Low Voltage Op Amps

Goal
To illustrate the degrees of freedom and choices of different circuit architectures that can enhance the performance of a given op amp.

SECTION 7.1 – BUFFERED OP AMPS

Objective
The objective of this presentation is:
1.) Illustrate the method of lowering the output resistance of simple op amps
2.) Show examples

Outline
• Open-loop MOSFET buffered op amps
• Closed-loop MOSFET buffered op amps (shunt negative feedback)
• BJT output op amps
• Summary
What is a Buffered Op Amp?
A buffered op amp is an op amp with a low value of output resistance, $R_o$.
Typically, $10 \Omega \leq R_o \leq 1000 \Omega$
The result is a voltage-controlled, voltage-source amplifier.

Requirements
Generally the same as for the output amplifier:
- Low output resistance
- Large output signal swing
- Low distortion
- High efficiency

The Source Follower as a Buffer
Class-A Follower:
- Simple, gain < 1
- Lower efficiency
- $R_{out} = \frac{1}{g_m + g_{mbs}} \approx 500$ to $1000 \Omega$
- Level shift from input to output

Push-Pull Follower:
- Voltage loss from 2 cascaded followers
- Higher efficiency

Current in M1 and M2 determined by:
$$V_{GS4} + V_{SG3} = V_{GS1} + V_{SG2}$$
$$\sqrt{\frac{2I_6}{K_n(W_4/L_4)}} + \sqrt{\frac{2I_5}{K_p(W_3/L_3)}}$$
$$= \sqrt{\frac{2I_1}{K_n(W_1/L_1)}} + \sqrt{\frac{2I_2}{K_p(W_2/L_2)}}$$

Use the $W/L$ ratios to define $I_1$ and $I_2$ from $I_5$ and $I_6$
Two-Stage Op Amp with Follower

Power dissipation now becomes \((I_5 + I_7 + I_9)V_{DD}\)

Gain becomes,

\[
A_v = \left( \frac{g_{m1}}{g_{ds2}+g_{ds4}} \right) \left( \frac{g_{m6}}{g_{ds6}+g_{ds7}} \right) \left( \frac{g_{m8}}{g_{m8}+g_{mb}+g_{ds8}+g_{ds9}} \right)
\]

Source-Follower, Push-Pull Output Op Amp

\[
R_{out} \approx \frac{1}{g_{m21}+g_{m22}} \leq 1000\Omega, \quad A_v(0)=65\text{dB} \quad (I_{Bias}=50\mu\text{A}), \quad \text{and} \quad GB = 60\text{MHz} \quad \text{for} \quad C_L = 1\text{pF}
\]
**Compensation of Op Amps with Output Amplifiers**

Compensation of a three-stage amplifier:

This op amp introduces a third pole, $p_3'$ (what about zeros?)

With no compensation,

\[
\frac{V_{out}(s)}{V_{in}(s)} = -A_{VO} \frac{s}{p_1' - 1} \frac{s}{p_2' - 1} \frac{s}{p_3' - 1}
\]

**Illustration of compensation choices:**

- Miller compensation applied around both the second and the third stage.
- Miller compensation applied around the second stage only.

**Crossover-Inverter, Buffer Stage Op Amp**

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small $R_L$ the gain of this stage is approximately unity.

This op amp is capable of delivering 160mW to a 100Ω load while only dissipating 7mW of quiescent power!
Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?
The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, \( v_{in}' \).

Consider the idealized voltage transfer characteristic of the crossover inverters:

Crossover voltage \( V_C = V_B - V_A \approx 0 \)

\( V_C \) is designed to be small and positive for worst case variations in processing.

Low Output Resistance Op Amp

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:

Comments:
- The output resistance will be equal to \( r_{ds1} \| r_{ds2} \) divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined
Low Output Resistance Op Amp - Continued

Offset correction circuitry:

![Circuit Diagram](image)

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When $V_{OS}$ is positive, M6 tries to turn off and so does M6A. $I_{M9}$ reduces thus reducing $I_{M12}$. A reduction in $I_{M12}$ reduces $I_{M8A}$ thus decreasing $V_{GS8A}$. $V_{GS8A}$ ideally decreases by an amount equal to $V_{OS}$. A similar result holds for negative offsets and offsets in $EA2$. 

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Low Output Resistance Op Amp - Continued

Error amplifiers:
**Low Output Resistance Op Amp - Complete Schematic**

![Diagram of a low output resistance op amp](image)

Short circuit protection (max. output ±60mA):
- MP3-MN3-MN4-MP4-MP5
- MN3A-MP3A-MP4A-MN4A-MN5A

\[ R_{out} \approx \text{Loop Gain} \approx \frac{50k\Omega}{5000} = 10\Omega \]

**Simpler Implementation of Negative Feedback to Achieve Low Output Resistance**

![Diagram of a simpler implementation](image)

Output Resistance:

\[ R_{out} = \frac{R_o}{1 + |LG|} \]

where

\[ R_o = \frac{1}{g_{ds6} + g_{ds7}} \]

and

\[ |LG| = \frac{g_{m2}}{2g_{m4}} (g_{m6} + g_{m7}) R_o \]

Therefore, the output resistance is:

\[ R_{out} = \frac{1}{(g_{ds6} + g_{ds7}) \left[ 1 + \left( \frac{g_{m2}}{2g_{m4}} \right) (g_{m6} + g_{m7}) R_o \right]} \]
**Example 7.1-1 - Low Output Resistance Using Shunt Negative Feedback Buffer**

Find the output resistance of above op amp using the model parameters of Table 3.1-2.

**Solution**

The current flowing in the output transistors, M6 and M7, is 1mA which gives $R_o$ of

$$ R_o = \left( \frac{1}{\lambda_N + \lambda_P} \right) 1 \text{mA} = \frac{1000}{0.09} = 11.11 \text{kΩ} $$

To calculate the loop gain, we find that

$$ g_m^2 = \sqrt{2K_N \cdot 10 \cdot 100 \mu A} = 469 \mu S $$

$$ g_m^4 = \sqrt{2K_P \cdot 1 \cdot 100 \mu A} = 100 \mu S $$

and

$$ g_m^6 = \sqrt{2K_P \cdot 1 \cdot 1000 \mu A} = 1 \text{mS} $$

Therefore, the loop gain is

$$ |L_G| = \frac{469}{100} \cdot 12 \cdot 11.11 = 104.2 $$

Solving for the output resistance, $R_{out}$, gives

$$ R_{out} = \frac{11.11 \text{kΩ}}{1 + 104.2} = 106 \Omega \text{ (Assumes that } R_L \text{ is large)} $$

---

**BJTs Available in CMOS Technology**

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

![BJT Illustration](image)

**Comments:**

- $g_m$ of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Can use the lateral or substrate BJT but since the collector is on ac ground, the substrate BJT is preferred
- Current is required to drive the BJT
Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:
1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by 1+$\beta_F$)
2.) Reduces the output load at the drains of M6 and M7

Small-signal output resistance:

$$R_{out} \approx \frac{r_{\pi 10} + (1/g_{m9})}{1+\beta_F} = \frac{1}{g_{m10}} + \frac{1}{g_{m9}(1+\beta_F)}$$

$$= 51.6\Omega + 6.7\Omega = 58.3\Omega \text{ where } I_{10} = 500\mu A, I_8 = 100\mu A, W_9/L_9 = 100 \text{ and } \beta_F \text{ is 100}$$

$$v_{OUT}(\text{max}) = V_{DD} - V_{SD8(\text{sat})} - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P}{I_{S10}}} \cdot I_{S10}$$

Voltage gain:

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m1}{g_{ds2} + g_{ds4} + g_{ds7} + g_{ds6} + g_{m9} + g_{m10} + g_{mb9} + g_{ds8} + g_{m10}R_L}{1 + g_{m10}R_L}$$

Compensation will be more complex because of the additional stages.

Example 7.1-2 - Designing the Class-A, Buffered Op Amp

Use the parameters of Table 3.1-2 along with the BJT parameters of $I_s = 10^{-14}A$ and $\beta_F = 100$ to design the class-A, buffered op amp to give the following specifications.

Assume the channel length is to be 1$\mu$m.

$V_{DD} = 2.5V$ $V_{SS} = -2.5V$ $GB = 5MHz$ $A_{vd}(0) \geq 5000V/V$ $\text{Slew rate} \geq 10V/\mu s$

$R_L = 500\Omega$ $R_{out} \leq 100\Omega$ $C_L = 100pF$ $ICMR = -1V \text{ to } 2V$

Solution

Because the specifications above are similar to the two-stage design of Ex. 6.3-1, we can use these results for the first two stages of our design. However, we must convert the results of Ex. 6.3-1 to a PMOS input stage. The results of doing this give $W_1 = W_2 = 6\mu m$, $W_3 = W_4 = 7\mu m$, $W_5 = 11\mu m$, $W_6 = 43\mu m$, and $W_7 = 34\mu m$.

BJT follower:

$SR = 10V/\mu s$ and 100pF capacitor give $I_{11} = 1mA$.

$I_{11} = 1mA \Rightarrow 1/g_{m10} = 0.0258V/1mA = 25.8\Omega$

MOS follower:

To source 1mA, the BJT requires 20$\mu A$ ($\beta = 100$) from the MOS follower. Therefore, select a bias current of 100$\mu A$ for M8.

If $W_{12} = 44\mu m$, then $W_8 = 44\mu m(100\mu A/30\mu A) = 146\mu m$. 

\[ CMOS \ Analog \ Circuit \ Design \]
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Example 7.1-2 - Continued

If $1/gm_{10}$ is 25.8Ω, then design $gm_9$ as

$$\frac{1}{gm_{10}} = \frac{1}{gm_9(1+\beta_F)} = 25.8\Omega \quad \Rightarrow \quad gm_9 = \frac{1}{(25.8\Omega)(1+\beta_F)} = \frac{1}{25.8\cdot101} = 384\mu S$$

:. $gm_9$ and $I_9 \Rightarrow W/L = 6.7$

To calculate the voltage gain of the MOS follower we need to find $gm_{bs9}$.

$$gm_{bs9} = \frac{gm_9\gamma_N}{2\sqrt{2\phi_F + V_{BS9}}} = \frac{384\cdot0.4}{2\sqrt{0.7+2}} = 46.7\mu S$$

where we have assumed that the value of $V_{SB9}$ is approximately 2V.

:. $A_{MOS} = \frac{384\mu S+46.7\mu S+4\mu S+5\mu S}{0.873}$

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951\text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0) = (7777)(0.873)(0.951) = 6459\text{ V/V}$$

The power dissipation of this amplifier is,

$$P_{diss.} = 5V(1255\mu A) = 6.27\text{mW}$$

SUMMARY

- A buffered op amp requires an output resistance between $10\Omega \leq R_o \leq 1000\Omega$
- Output resistance using MOSFETs only can be reduced by,
  - Source follower output ($1/gm$)
  - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT’s can reduce the output resistance because $gm$ is larger than the $gm$ of a MOSFET
- Adding a buffer stage to lower the output resistance will most likely complicate the compensation of the op amp
SECTION 7.2 – HIGH SPEED/FREQUENCY OP AMPS

Objective
The objective of this presentation is:
1.) Increase the GB of operational amplifiers
2.) Cascading of Amplifiers

Outline
• Extending the GB of conventional op amps
• Cascade Amplifiers
  - Voltage amplifiers
  - Voltage amplifiers using current feedback

INCREASING THE GB OF OP AMPS

What is the Influence of GB on the Frequency Response?
The unity-gainbandwidth represents a limit in the trade-off between closed loop voltage gain and the closed-loop -3dB frequency.
Example of a gain of -10 voltage amplifier:

What causes the GB?
We know that

$$GB = \frac{g_m}{C}$$

where $g_m$ is the transconductance that converts the input voltage to current and $C$ is the capacitor that causes the dominant pole.
This relationship assumes that all higher-order poles are greater than GB.
What is the Limit of $GB$?

The following illustrates what happens when the next higher pole is not greater than $GB$:

For a two-stage op amp, the poles and zeros are:

1.) Dominant pole \[ p_1 = \frac{-g_{m1}}{A_v(0)C_c} \]

2.) Output pole \[ p_2 = \frac{-g_{m6}}{C_L} \]

3.) Mirror pole \[ p_3 = \frac{-g_{m3}}{C_s3 + C_s4} \] and \[ z_3 = 2p_3 \]

4.) Nulling pole \[ p_4 = -\frac{1}{R_zC_I} \]

5.) Nulling zero \[ z_1 = -\frac{1}{R_zC_c(C_c/g_{m6})} \]

Higher-Order Poles

For reasonable phase margin, the smallest higher-order pole should be 2-3 times larger than $GB$ if all other higher-order poles are larger than $10GB$.

If the higher-order poles are not greater than $10GB$, then the distance from $GB$ to the smallest non-dominant pole should be increased for reasonable phase margin.
Increasing the $GB$ of a Two-Stage Op Amp

1.) Use the nulling zero to cancel the closest pole beyond the dominant pole.
2.) The maximum $GB$ would be equal to the magnitude of the second closest pole beyond the dominant pole.
3.) Adjust the dominant pole so that $2.2GB$ = (second closest pole beyond the dominant pole)

Illustration which assumes that $p_2$ is the next closest pole beyond the dominant pole:

Example 7.2-1 - Increasing the $GB$ of the Op Amp Designed in Ex. 6.3-1

Use the two-stage op amp designed in Example 6.3-1 and apply the above approach to increase the gainbandwidth as much as possible.

Solution

1.) First find the values of $p_2$, $p_3$, and $p_4$.
   (a.) From Ex. 6.3-2, we see that $p_2 = -94.25 \times 10^6$ rad/s.
   (b.) $p_3$ was found in Ex. 6.3-1 as $p_3 = -2.81 \times 10^9$ rad/s. (also there is a zero at $-5.62 \times 10^9$ rad/s.)
   (c.) To find $p_4$, we must find $C_I$ which is the output capacitance of the first stage of the op amp. $C_I$ consists of the following capacitors,

\[ C_I = C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4} \]

For $C_{bd2}$ the width is $3 \mu m \Rightarrow L1+L2+L3=3 \mu m \Rightarrow AS/AD=9 \mu m^2$ and PS/PD=12 $\mu m$.
For $C_{bd4}$ the width is $15 \mu m \Rightarrow L1+L2+L3=3 \mu m \Rightarrow AS/AD=45 \mu m^2$ and PS/PD=36 $\mu m$.
From Table 3.2-1:

\[ C_{bd2} = (9 \mu m^2)(770 \times 10^{-6} F/m^2) + (12 \mu m)(380 \times 10^{-12} F/m) = 6.93 fF + 4.56 fF = 11.5 fF \]

\[ C_{bd4} = (45 \mu m^2)(560 \times 10^{-6} F/m^2) + (36 \mu m)(350 \times 10^{-12} F/m) = 25.2 fF + 12.6 F = 37.8 fF \]
Example 7.2-1 - Continued

$C_{gs6}$ is given by Eq. (10b) of Sec. 3.2 and is

$$C_{gs6} = CGD0 \cdot W_6 + 0.67(C_{ox} W_6 L_6) = (220 \times 10^{-12})(94 \times 10^{-6}) + (0.67)(24.7 \times 10^{-4})(94 \times 10^{-12})$$

$$= 20.7 \text{fF} + 154.8 \text{fF} = 175.5 \text{fF}$$

$C_{gd2} = 220 \times 10^{-12} \times 3 \text{μm} = 0.66 \text{fF}$ and $C_{gd4} = 220 \times 10^{-12} \times 15 \text{μm} = 3.3 \text{fF}$

Therefore, $C_I = 11.5 \text{fF} + 37.8 \text{fF} + 175.5 \text{fF} + 0.66 \text{fF} + 3.3 \text{fF} = 228.8 \text{fF}$. Although $C_{bd2}$ and $C_{bd4}$ will be reduced with a reverse bias, let us use these values to provide a margin. In fact, we probably ought to double the whole capacitance to make sure that other layout parasitics are included. Thus let $C_I$ be 300fF.

In Ex. 6.3-2, $R_z$ was 4.591kΩ which gives $p_4 = -0.726 \times 10^9$ rads/sec.

2.) Using the nulling zero, $z_1$, to cancel $p_2$, gives $p_4$ as the next smallest pole.

For 60° phase margin $\frac{GB}{|p_4|/2.2}$ if the next smallest pole is more than 10$GB$.

$$\Rightarrow \quad GB = 0.726 \times 10^9 / 2.2 = 0.330 \times 10^9 \text{ rads/sec. or 52.5MHz.}$$

This value of $GB$ is designed from the relationship that $GB = g_{m1}/C_c$. Assuming $g_{m1}$ is constant, then $C_c = g_{m1}/GB = (94.25 \times 10^{-6})/(0.330 \times 10^9) = 286 \text{fF}$. It might be useful to increase $g_{m1}$ in order to keep $C_c$ above the surrounding parasitic capacitors ($C_{gd6} = 20.7 \text{fF}$). The success of this method assumes that there are no other roots with a magnitude smaller than 10$GB$.

Example 7.2-2 - Increasing the GB of the Folded Cascode Op Amp of Ex. 6.5-3

Use the folded-cascode op amp designed in Example 6.5-3 and apply the above approach to increase the gainbandwidth as much as possible. Assume that the drain/source areas are equal to 2μm times the width of the transistor and that all voltage dependent capacitors are at zero voltage.

Solution

The poles of the folded cascode op amp are:

$$p_A \approx \frac{-1}{R_A C_A} \quad \text{(the pole at the source of M6)}$$

$$p_B \approx \frac{-1}{R_B C_B} \quad \text{(the pole at the source of M7)}$$

$$p_6 \approx \frac{-g_{m10}}{C_6} \quad \text{(the pole at the drain of M6)}$$

$$p_8 \approx \frac{-g_{m8} r_{ds8} g_{m10}}{C_8} \quad \text{(the pole at the source of M8)}$$

$$p_9 \approx \frac{-g_{m9}}{C_9} \quad \text{(the pole at the source of M9)}$$
**Example 7.2-2 - Continued**

Let us evaluate each of these poles.

1.) For \( p_A \), the resistance \( R_A \) is approximately equal to \( g_{m6} \) and \( C_A \) is given as

\[
C_A = C_{gs6} + C_{bd1} + C_{gd1} + C_{bd4} + C_{bs6} + C_{gd4}
\]

From Ex. 6.5-3, \( g_{m6} = 744.6 \mu S \) and capacitors giving \( C_A \) are found using the parameters of Table 3.2-1 as,

\[
C_{gs6} = (220 \times 10^{-12} \times 80 \times 10^{-6}) + (0.67)(80 \times 10^{-6} \times 10^{-6} \times 24.7 \times 10^{-4}) = 149 \text{ fF}
\]

\[
C_{bd1} = (770 \times 10^{-6})(35.9 \times 10^{-6} \times 2 \times 10^{-6}) + (380 \times 10^{-12})(2 \times 37.9 \times 10^{-6}) = 84 \text{ fF}
\]

\[
C_{gd1} = (220 \times 10^{-12} \times 35.9 \times 10^{-6}) = 8 \text{ fF}
\]

\[
C_{bd4} = C_{bs6} = (560 \times 10^{-6})(80 \times 10^{-6} \times 2 \times 10^{-6}) + (350 \times 10^{-12})(2 \times 82 \times 10^{-6}) = 147 \text{ fF}
\]

and

\[
C_{gd4} = (220 \times 10^{-12})(80 \times 10^{-6}) = 17.6 \text{ fF}
\]

Therefore,

\[
C_A = 149 \text{ fF} + 84 \text{ fF} + 8 \text{ fF} + 147 \text{ fF} + 147 \text{ fF} = 0.553 \text{ pF}
\]

Thus,

\[
\frac{-744.6 \times 10^{-6}}{0.553 \times 10^{-12}} = -1.346 \times 10^9 \text{ rad/s}.
\]

2.) For the pole, \( p_B \), the capacitance connected to this node is

\[
C_B = C_{gd2} + C_{bd2} + C_{gs7} + C_{gd5} + C_{bd5} + C_{bs7}
\]

The various capacitors above are found as

\[
C_{gd2} = (220 \times 10^{-12} \times 35.9 \times 10^{-6}) = 8 \text{ fF}
\]

\[
C_{bd2} = (770 \times 10^{-6})(35.9 \times 10^{-6} \times 2 \times 10^{-6}) + (380 \times 10^{-12})(2 \times 37.9 \times 10^{-6}) = 84 \text{ fF}
\]

\[
C_{gs7} = (220 \times 10^{-12} \times 80 \times 10^{-6}) + (0.67)(80 \times 10^{-6} \times 10^{-6} \times 24.7 \times 10^{-4}) = 149 \text{ fF}
\]

\[
C_{gd5} = (220 \times 10^{-12})(80 \times 10^{-6}) = 17.6 \text{ fF}
\]

and

\[
C_{bd5} = C_{bs7} = (560 \times 10^{-6})(80 \times 10^{-6} \times 2 \times 10^{-6}) + (350 \times 10^{-12})(2 \times 82 \times 10^{-6}) = 147 \text{ fF}
\]

The value of \( C_B \) is the same as \( C_A \) and \( g_{m6} \) is assumed to be the same as \( g_{m7} \) giving \( p_B = p_A = -1.346 \times 10^9 \text{ rad/s} \).

3.) For the pole, \( p_6 \), the capacitance connected to this node is

\[
C_6 = C_{bd6} + C_{gd6} + C_{gs8} + C_{gs9}
\]

The various capacitors above are found as

\[
C_{bd6} = (560 \times 10^{-6})(80 \times 10^{-6} \times 2 \times 10^{-6}) + (350 \times 10^{-12})(2 \times 82 \times 10^{-6}) = 147 \text{ fF}
\]

\[
C_{gs8} = (220 \times 10^{-12} \times 36.4 \times 10^{-6}) + (0.67)(36.4 \times 10^{-6} \times 10^{-6} \times 24.7 \times 10^{-4}) = 67.9 \text{ fF}
\]

and

\[
C_{gs9} = C_{gs8} = 67.9 \text{ fF}
\]

\[
C_{gd6} = C_{gd5} = 17.6 \text{ fF}
\]

Therefore,

\[
C_6 = 147 \text{ fF} + 17.6 \text{ fF} + 67.9 \text{ fF} + 67.9 \text{ fF} = 0.300 \text{ pF}
\]
Example 7.2-2 - Continued

From Ex. 6.5-3, \( g_{m6} = 744.6 \times 10^{-6} \). Therefore, \( p_6 \), can be expressed as

\[
744.6 \times 10^{-6} \quad -p_6 = \frac{0.300 \times 10^{-12}}{2.482 \times 10^9 \text{ rads/sec.}}
\]

4.) Next, we consider the pole, \( p_8 \). The capacitance connected to this node is

\[
C_8 = C_{bd10} + C_{gd10} + C_{gs8} + C_{bs8}
\]

These capacitors are given as,

\[
C_{bs8} = C_{bd10} = (770 \times 10^{-6})(36.4 \times 10^{-6} \cdot 2 \times 10^{-6}) + (380 \times 10^{-12})(2 \cdot 38.4 \times 10^{-6}) = 85.2 \text{ fF}
\]

\[
C_{gs8} = (220 \times 10^{-12} \cdot 36.4 \times 10^{-6}) + (0.67)(36.4 \times 10^{-6} \cdot 10^{-6} \cdot 24.7 \times 10^{-4}) = 67.9 \text{ fF}
\]

and

\[
C_{gd10} = (220 \times 10^{-12})(36.4 \times 10^{-6}) = 8 \text{ fF}
\]

The capacitance \( C_8 \) is equal to

\[
C_8 = 67.9 \text{ fF} + 8 \text{ fF} + 85.2 \text{ fF} + 85.2 \text{ fF} = 0.246 \text{ pF}
\]

Using the values of Ex. 6.5-3 of \( 774.6 \mu \text{S} \), the pole \( p_8 \) is found as,

\[
-p_8 = g_{m8} r_{ds8} g_{m10}/C_8 = -774.6 \mu \text{S} \cdot 774.6 \mu \text{S} / 3 \mu \text{S} = 812.4 \times 10^9 \text{ rads/sec.}
\]

5.) The capacitance for the pole at \( p_9 \) is identical with \( C_8 \). Therefore, since \( g_{m9} \) is \( 774.6 \mu \text{S} \), the pole \( p_9 \) is found to be \(-p_9 = 3.149 \times 10^9 \text{ rads/sec.}

The poles are summarized below:

\[
\begin{align*}
P_A &= -1.346 \times 10^9 \text{ rads/sec} & P_B &= -1.346 \times 10^9 \text{ rads/sec} & P_6 &= -2.482 \times 10^9 \text{ rads/sec} \\
P_8 &= -812.4 \times 10^9 \text{ rads/sec} & P_9 &= -3.149 \times 10^9 \text{ rads/sec}
\end{align*}
\]

The smallest of these poles is \( p_A \) or \( p_B \). Since \( p_6 \) and \( p_9 \) are not much larger than \( p_A \) or \( p_B \), we will find the new \( GB \) by dividing \( p_A \) or \( p_B \) by 6 (rather than 2.2) to get \( 224 \times 10^6 \text{ rads/sec} \approx 200 \times 10^6 \). Thus the new \( GB \) will be \( 200/2\pi \) or \( 32 \text{MHz} \). The magnitude of the dominant pole is given as

\[
P_{\text{dominant}} = \frac{GB}{A_{vd}(0)} = \frac{200 \times 10^6}{7.464} = 26.795 \text{ rads/sec}.
\]

The value of load capacitor that will give this pole is

\[
C_L = \frac{1}{P_{\text{dominant}} R_{out}} = \frac{1}{26.795 \times 10^3 \cdot 19.4 \text{M\Omega}} \approx 1.9 \text{pF}
\]

Therefore, the new \( GB = 32 \text{MHz} \) compared with the old \( GB = 10 \text{MHz} \).
Elimination of Higher-Order Poles

The minimum circuitry for a cascode op amp is shown below:

If the source-drain area between M1 and M2 and M3 and M4 can be minimized, the non-dominant poles will be quite large.

Dynamically Biased, Push-Pull, Cascode Op Amp

Push-pull, cascode amplifier: M1-M2 and M3-M4
Bias circuitry: M5-M6-C2 and M7-M8-C1
**Dynamically Biased, Push-Pull, Cascode Op Amp - Continued**

**Operation:**

Equivalent circuit during the $\phi_1$ clock period

**Equivalent circuit during the $\phi_2$ clock period.**

$\text{Fig. 7.2-6}$

---

This circuit will operate on both clock phases$^1$.

**Performance (1.5$\mu$m CMOS):**
- 1.6mW dissipation
- $GB = 130$MHz ($C_L=2.2pF$)
- Settling time of 10ns ($C_L=10pF$)

This amplifier was used with a 28.6MHz clock to realize a 5th-order switched capacitor filter having a cutoff frequency of 3.5MHz.

CASCADED AMPLIFIERS USING VOLTAGE AMPLIFIERS

Bandwidth of Cascaded Amplifiers
Cascading of low-gain, wide-bandwidth amplifiers:

\[
\frac{A_o}{s/\omega_1 + 1} \cdot \frac{A_o}{s/\omega_1 + 1} \cdot \frac{A_o}{s/\omega_1 + 1} \ldots \frac{A_o}{s/\omega_1 + 1} = \left(\frac{A_o}{s/\omega_1 + 1}\right)^n
\]

Overall gain is \(A_o^n\)

-3dB frequency is,

\[\omega_{-3dB} = \omega_1 \sqrt{2^{1/n} - 1}\]

If \(A_o = 10\), \(\omega_1 = 300 \pi \times 10^6\) rad/s and \(n = 3\), then

Overall gain is 60dB and \(\omega_{-3dB} = 0.51 \omega_1 = 480 \times 10^6\) rad/s → 76.5 MHz

Voltage Amplifier Suitable for Cascading

\[
\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{K_{n'}(W_1/L_1)(I_3+I_5)}{K_{p'}(W_3/L_3)I_3}}
\]

\[\omega_{-3dB} \approx \frac{g_{m3}}{C_{gs1}}\]
Ex. 7.2-3 - Design of a Voltage Amplifier for Cascading

Design the previous voltage amplifier for a gain of $A_o = 10$ and a power dissipation of no more than 1mW. The design should permit $A_o$ to be well defined. What is the $\omega_{3\text{dB}}$ for this amplifier and what would be the $\omega_{3\text{dB}}$ for a cascade of three identical amplifiers?

**Solution**

To keep enhance the accuracy of the gain, we replace M3 and M4 with NMOS transistors to avoid the variation of the transconductance parameter. This assumes a $p$-well technology to avoid bulk effects. The gain of 10 requires,

$$\frac{W_1}{L_1}(I_3+I_5) = 100\frac{W_3}{L_4} I_3$$

If $V_{DD} = 2.5V$, then $2(I_3+I_5)\cdot2.5V = 1000\mu W.$ Therefore, $I_3+I_5 = 200\mu A$. Let $I_3 = 20\mu A$ and $W_1/L_1 = 10W_3/L_3$.

Choose $W_1/L_1 = 5\mu m/0.5\mu m$ which gives $W_3/L_3 = 0.5\mu m/0.5\mu m$. M5 and M6 are designed to give $I_5 = 180\mu A$ and M7 is designed to give $I_7 = 400\mu A$.

The dominant pole is $g_{m3}/C_{out}$.

---

**Ex. 7.2-3 – Continued**

$$C_{out} = C_{gs3}+C_{bs3}+C_{bd1}+C_{bd5}+C_{gd1}+C_{gd5}+C_{gs1}(\text{next stage}) \approx C_{gs3} + C_{gs1}$$

Using $C_{ox} = 60.6 \times 10^{-4} \text{ F/m}^2$, we get,

$$C_{out} \approx (2.5+0.25) \times 10^{-12} \text{ m}^2 \times 60.6 \times 10^{-4} \text{ F/m}^2 = 16.7 \text{fF} \rightarrow C_{out} \approx 20\text{fF}$$

$$g_{m3} = \sqrt{2 \cdot 120 \cdot 1 \cdot 20} \mu S = 69.3 \mu S$$

Therefore, dominant pole $\approx 69.3 \mu S/20\text{fF} = 34.65 \times 10^8 \text{ rad/s} \rightarrow f_{3\text{dB}} = 551\text{MHz}$

The bandwidth of three identical cascaded amplifiers giving a low-frequency gain of 60dB would have a $f_{3\text{dB}}$ of

$$f_{3\text{dB}(\text{Overall})} = f_{3\text{dB}} \sqrt{2^{1/3} - 1} = 551\text{MHz} \times (0.5098) = 281\text{MHz}.$$

$P_{\text{diss}} = 3\text{mW}$
A 71 MHz CMOS Programmable Gain Amplifier†

Uses 3 ac-coupled stages.
First stage (0-20dB, common gate for impedance matching and NF):

- $R_{in} = 330\Omega$ to match source driving requirement
- All current sinks are identical for the differential switches.
- Dominant pole at 150MHz.

---

A 71 MHz PGA – Continued

Second stage (-10dB to 20dB):

- Dominant pole is also at 150MHz
- For $V_{DD} = 2.5V$, at 60dB gain, the total current is 2.6mA
- $I_{IP3} \approx +1\text{dBm}$

---


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CASCaded AMPLIFIERS USING CURRENT FEEDBACK AMPLIFIERS

Advantages of Using Current Feedback
Why current feedback:
• Higher $GB$
• Less voltage swing ⇒ more dynamic range

What is a current amplifier?

\[ \text{Current Amplifier} \]

\[ R_{i1} \quad i_1 \quad - \quad + \quad i_2 \quad R_{i2} \]

\[ R_{o} \]

\[ i_o \]

Requirements:
\[ i_o = A_i(i_1 - i_2) \]
\[ R_{i1} = R_{i2} = 0 \Omega \]
\[ R_{o} = \infty \]

Ideal source and load requirements:
\[ R_{source} = \infty \]
\[ R_{load} = 0 \Omega \]

Bandwidth Advantage of a Current Feedback Amplifier
Consider the inverting voltage amplifier shown using a current amplifier with negative current feedback:

The output current, $i_o$, of the current amplifier can be written as
\[ i_o = A_i(s)(i_1 - i_2) = -A_i(s)(i_{in} + i_o) \]

The closed-loop current gain, $i_o/i_{in}$, can be found as
\[ \frac{i_o}{i_{in}} = \frac{-A_i(s)}{1+A_i(s)} \]

However, $v_{out} = i_oR_2$ and $v_{in} = i_{in}R_1$. Solving for the voltage gain, $v_{out}/v_{in}$ gives
\[ \frac{v_{out}}{v_{in}} = \frac{i_oR_2}{i_{in}R_1} = \frac{-R_2}{R_1} \left( \frac{A_i(s)}{1+A_i(s)} \right) \]

If $A_i(s) = \frac{A_o}{s\omega A + 1}$, then
\[ \frac{v_{out}}{v_{in}} = \frac{-R_2}{R_1} \left( \frac{A_o}{1+A_o} \right) \left( \frac{\omega A(1+A_o)}{s + \omega A(1+A_o)} \right) \Rightarrow A_v(0) = \frac{-R_2A_o}{R_1(1+A_o)} \]

and $\omega_{3dB} = \omega_A(1+A_o)$
**Bandwidth Advantage of a Current Feedback Amplifier - Continued**

The unity-gainbandwidth is,

\[ GB = |A_v(0)| \omega_{-3dB} = \frac{R_2 A_o}{R_1(1+A_o)} \cdot \omega_A(1+A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i \]

where \( GB_i \) is the unity-gainbandwidth of the current amplifier.

*Note that if \( GB_i \) is constant, then increasing \( \frac{R_2}{R_1} \) (the voltage gain) increases \( GB \).*

Illustration:

Note that \( GB_2 > GB_1 > GB_i \)

The above illustration assumes that the \( GB \) of the voltage amplifier realizing the voltage buffer is greater than the \( GB \) achieved from the above method.

---

**A Wide-Swing, Cascode Current Mirror Implementation of a High Frequency Amplifier**

The current mirror shown below increases the value of \( R_2 \) by increasing the output resistance of the current mirror.

**Limitations:**

\[ R_1 > \frac{1}{g_{m1}} \text{ and } R_2 < g_{m4}r_{ds4}r_{ds2} || g_{m6}r_{ds6}r_{ds8} \Rightarrow \frac{R_2}{R_1} \ll g_{m1}(g_{m4}r_{ds4}r_{ds2} || g_{m6}r_{ds6}r_{ds8}) \]
Example 7.2-4 - Design of a High GB Voltage Amplifier using Current Feedback

Design the wide-swing, cascode voltage amplifier to achieve a gain of -10V/V and a GB of 500MHz which corresponds to a -3dB frequency of 50MHz.

Solution

Since we know what the gain is to be, let us begin by assuming that $C_o$ will be 100fF. Thus to get a $GB$ of 500MHz, $R_1$ must be 3.2kΩ and $R_2 = 32$kΩ. Therefore, $\frac{1}{g_{m1}}$ must be less than 3200 (say 300). Therefore we can write

$$g_{m1} = \sqrt{2K'\frac{W}{L}} = \frac{1}{300\Omega} \rightarrow 5.56 \times 10^{-6} = K' \cdot I \cdot \frac{W}{L} \rightarrow 0.0505 = I \cdot \frac{W}{L}$$

At this point we have a problem because if $W/L$ is small to minimize $C_o$, the current will be too high. If we select $W/L = 200\mu$m/$1\mu$m we will get a current of 0.25mA. However, using this $W/L$ for M4 and M6 will give a value of $C_o$ that is greater than 100fF. Therefore, select $W/L = 200$ for M1, M3, M5 and M7 and $W/L = 20\mu$m/$1\mu$m for M2, M4, M6, and M8 which gives a current in these transistors of 25μA.

Since $R_2/R_1$ is multiplied by 1/11 let $R_2$ be 110 times $R_1$ or 352kΩ.

Now select a $W/L$ for M12 of $20\mu$m/$1\mu$m which will now permit us to calculate $C_o$. We will assume zero-bias on all voltage dependent capacitors. Furthermore, we will assume the diffusion area as 2μm times the $W$. $C_o$ can be written as

$$C_o = C_{gd4} + C_{bd4} + C_{gd6} + C_{bd6} + C_{gs12}$$

Example 7.2-4 - Design of a High GB Voltage Amplifier using Current Feedback - Cont’d

The information required to calculate these capacitors is found from Table 3.2-1.

The various capacitors are,

- $C_{gd4} = C_{gd6} = CGDO \times 10\mu$m = (220x10-12)(20x10-6) = 4.4fF
- $C_{bd4} = CJxAD4+CJSWxPD4 = (770x10^{-6})(20x10^{-12})+(380x10^{-12})(44x10^{-6})$
  = 15.4fF+16.7fF = 32.1fF
- $C_{bd6} = (560x10^{-6})(20x10^{-12})+(350x10^{-12})(44x10^{-6}) = 26.6fF$
- $C_{gs12} = (220x10^{-12})(20x10^{-6}) + (0.67)(20x10^{-6} \cdot 10^{-6} \cdot 24.7 \times 10^{-4}) = 37.3fF$

Therefore,

$$C_o = 4.4fF+32.1fF+4.4fF+26.6fF+37.3fF = 105fF$$

Note that if we had not reduced the $W/L$ of M2, M4, M6, and M8 that $C_o$ would have easily exceeded 100fF. Since 105fF is close to our original guess of 100fF, let us keep the values of $R_1$ and $R_2$. If this value was significantly different, then we would adjust the values of $R_1$ and $R_2$ so that the $GB$ is 500MHz. One must also check to make sure that the input pole is greater than 500MHz.

The design is completed by assuming that $IBias = 100\mu$A and that the current in M9 through M12 be 100μA. Thus $W_{13}/L_{13} = W_{14}/L_{14} = 20\mu$m/$1\mu$m and $W_{9}/L_{9}$ through $W_{12}/L_{12}$ are $20\mu$m/$1\mu$m.
**Example 7.2-4 - Continued**

![Graph showing frequency response with labels](image)

Simulation Results:

\[ f_{-3dB} = 38 \text{MHz} \quad GB = 300 \text{MHz} \quad \text{Closed-loop gain} = 18 \text{dB} \]

(Loss of -2dB is attributed to source follower and \( R_1 \))

Note second pole at about 1GHz. To get these results, it was necessary to bias the input at -1.7VDC using ±3V power supplies.

If \( R_1 \) is decreased to 1k\( \Omega \) results in:

- Gain of 26.4dB, \( f_{-3dB} = 32 \text{MHz} \), and \( GB = 630 \text{MHz} \)

---

**Current Feedback Amplifier**

The difficulties of making the input resistance of the current amplifier small compared to \( R_1 \) can be solved with the following block diagram:

\[
\frac{V_{out}}{V_{in}} = \frac{-G_M R_F A_i}{1 + A_i}
\]
Differential Implementation of the Current Feedback Amplifier

\[ I_{in} = \frac{g_{m1}}{1 + 0.5g_{m1}R_{in}} \left( V_{in^+} - V_{in^-} \right) \quad \text{and} \quad V_{out} = \frac{n (2R_F)}{1+n} I_{in} \]

\[ \frac{V_{out}}{V_{in}} \approx \frac{2nR_F}{R_{in}} \]

A 20dB Voltage Amplifier using a Current Amplifier

The following circuit is a programmable voltage amplifier with up to 20dB gain:

\[ R_1 \] and the current mirrors are used for gain variation while \[ R_2 \] is fixed.
**Programmability of the Previous Stage**

**Input OTA:**

Changes $G_M$ in 6dB steps.

**Programmability of the Voltage Stage – Cont’d**

**Current Amplifier:**

Changes $R_F$ in 2dB steps ($R_{F20\text{dB}} = 2.1\,\text{k\Omega}$, $R_{F18\text{dB}} = 1.6\,\text{k\Omega}$, $R_{F16\text{dB}} = 1.3\,\text{k\Omega}$, and $R_{F14\text{dB}} = 5\,\text{k\Omega}$).

$R_{F\text{Total}} = 10\,\text{k\Omega}$. 
Frequency Response of the Current Feedback PGA Stage

0.5pF load:

![Graph showing frequency response of the current feedback PGA stage with 0.5pF load.](image)

Frequency Response of the Entire 60dB PGA

Includes output buffer:

![Graph showing frequency response of the entire 60dB PGA including output buffer.](image)
SECTION 7.3 – DIFFERENTIAL OUTPUT OP AMPS

Objective
The objective of this presentation is:
1.) Design and analysis of differential output op amps
2.) Examine the problem of common mode stabilization

Outline
• Advantages and disadvantages of fully differential operation
• Examples of different differential output op amps
• Techniques of stabilizing the common mode output voltage
• Summary

Why Differential Output Op Amps?
• Cancellation of common mode signals including clock feedthrough
• Increased signal swing

![Figure 7.3-1](Fig. 7.3-1)

• Cancellation of even-order harmonics

Symbol:

![Figure 7.3-1A](Fig. 7.3-1A)
Common Mode Output Voltage Stabilization

If the common mode gain not small, it may cause the common mode output voltage to be poorly defined.

Illustration:

![Common Mode Output Voltage Stabilization Illustration](image)

EXAMPLES OF DIFFERENTIAL OUTPUT OP AMPS (OTA’S)

Two-Stage, Miller, Differential-In, Differential-Out Op Amp

Note that the upper ICMR is $V_{DD} - V_{SGP} + V_{TN}$

Output common mode range ($OCMR$) = $V_{DD} + |V_{SS}| - V_{SDP(sat)} - V_{DSN(sat)}$

The maximum peak-to-peak output voltage $\leq 2 \cdot OCMR$

Conversion between differential outputs and single-ended outputs:
Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Push-Pull Output

Comments:
- Able to actively source and sink output current
- Output quiescent current poorly defined

Folded-Cascode, Differential Output Op Amp

No longer has the low-frequency asymmetry in signal path gains.
Class A
Enhanced-Gain, Folded-Cascode, Differential Output Op Amp

What about the $A$ amplifier?

Below is the upper $A$ amplifier:

Note that $V_{Bias}$ controls the dc voltage at the input of the $A$ amplifier.

Push-Pull Cascode Op Amp with Differential-Outputs

Fig. 7.3-8
Folded-Cascode, Push-Pull, Differential Output Op Amp

\[ I_6 = I_7 = I_{14} = I_{15} > 0.5I_5 \]

\[ I_5 = I_1 + I_2 + I_3 + I_4 \]

\[ A_v = g_m R_{out}(\text{diff}) \]

Enhanced-Gain, Folded-Cascode with Push-Pull Outputs
Cross-Coupled Differential Amplifier Stage

The cross-coupled input stage allows the push-pull output quiescent current to be well defined.

![Cross-Coupled Differential Amplifier Stage Diagram](image)

Operation:

Voltage loop: \( v_{i2} - v_{i1} = -v_{GS1} + v_{GS1} + v_{SG4} - V_{SG4} = V_{SG3} - v_{SG3} - v_{GS2} + V_{GS2} \)

Using the notation for ac, dc, and total variables gives,

\[ v_{i2} - v_{i1} = v_{id} = (v_{sg1} + v_{gs4}) = -(v_{sg3} + v_{gs2}) \]

If \( g_{m1} = g_{m2} = g_{m3} = g_{m4} \), then half of the differential input is applied across each transistor with the correct polarity.

\[ i_1 = \frac{g_{m1}v_{id}}{2} = \frac{g_{m4}v_{id}}{2} \quad \text{and} \quad i_2 = -\frac{g_{m2}v_{id}}{2} = -\frac{g_{m3}v_{id}}{2} \]

Class AB, Differential Output Op Amp using a Cross-Coupled Differential Input Stage

![Class AB, Differential Output Op Amp Diagram](image)

Quiescent output currents are defined by the current in the input cross-coupled differential amplifier.
COMMON MODE OUTPUT VOLTAGE STABILIZATION

**Common Mode Feedback Circuits**

Because the common mode gain is undefined, any common mode signal at the input can cause the output common mode voltage to be improperly defined. The common mode output voltage is stabilized by sensing the common mode output voltage and using negative feedback to adjust the common mode voltage to the desired value.

Model for the Output of Differential Output Op Amps:

\[ V_{DD} \]

\[ \text{Class A Output} \]

\[ R_{O1} \]

\[ v_{o1} \]

\[ I_{o1}(\text{sink}) \]

\[ R_{O3} \]

\[ i_{o1}(\text{source}) \]

\[ R_{O2} \]

\[ v_{o2} \]

\[ I_{o2}(\text{sink}) \]

\[ R_{O4} \]

\[ i_{o2}(\text{source}) \]

\[ \text{Push-Pull Output} \]

\[ R_{Oj} \]

represents the self-resistance of the output sink/sources.

1.) If the common mode output voltage increases the sourcing current is too large.
2.) If the common mode output voltage decreases the sinking current is too large.

Conceptual View of Common-Mode Feedback

Function of the common-mode feedback circuit:

1.) If the common-mode output voltage increases, decrease the upper currents sources or increase the lower current sink until the common-mode voltage is equal to \( V_{CMREF} \).
2.) If the common-mode output voltage decreases, increase the upper currents sources or decrease the lower current sink until the common-mode voltage is equal to \( V_{CMREF} \).
Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Common-Mode Feedback

Fig. 7.3-12

Comments:
- Simple
- Unreferenced

Common Mode Feedback Circuits

Implementation of common mode feedback circuit:

This scheme can be applied to any differential output amplifier. CM Loop Gain = \(-g_{mC1}R_{o1}\) which can be large if the output of the differential output amplifier is cascaded or a gain-enhanced cascode. The common-mode loop gain may need to be compensated for proper dynamic performance.
Common Mode Feedback Circuits – Continued

The previous circuit suffers when the input common mode voltage is low because the transistors MC2A and MC2B have a poor negative input common mode voltage. The following circuit alleviates this disadvantage:

![Common-Mode Feedback Circuit](image1)

An Improved Common-Mode Feedback Circuit

The resistance loading of the previous circuit can be avoided in the following CM feedback implementation:

![CM Correction Circuitry](image2)

This circuit is capable of sustaining a large differential voltage without loading the output of the differential output op amp.
**Frequency Response of the CM Feedback Circuit**

Consider the following CM feedback circuit implementation:

![CM Feedback Circuit Diagram](image)

The CM feedback path has two poles – one at the gates of M10 and M11 and the dominant output pole of the differential output op amp.

---

**Improved CM Feedback Frequency Response**

The circuit on the previous page can be modified to eliminate the pole at the gates of M10 and M11 as follows:

![Improved CM Feedback Circuit Diagram](image)
External Common-Mode Output Voltage Stabilization Scheme for Discrete-Time Applications

![Diagram of the stabilization scheme](image)

**Operation:**
1. During the $\phi_1$ phase, both $C_{cm}$ are charged to the desired value of $V_{ocm}$ and $CMbias = V_{ocm}$.
2. During the $\phi_2$ phase, the $C_{cm}$ capacitors are connected between the differential outputs and the $CMbias$ node. The average value applied to the $CMbias$ node will be $V_{ocm}$.

**SUMMARY**

- **Advantages of differential output op amps:**
  - 6 dB increase in signal amplitude
  - Cancellation of even harmonics
  - Cancellation of common mode signals including clock feedthrough
- **Disadvantages of differential output op amps:**
  - Need for common mode output voltage stabilization
  - Compensation of common mode feedback loop
  - Difficult to interface with single-ended circuits
- Most differential output op amps are truly balanced
- For push-pull outputs, the quiescent current should be well defined
- Common mode feedback schemes include,
  - Unreferenced
  - Referenced
SECTION 7.4 – LOW POWER OP AMPS

Objective
The objective of this presentation is:
1.) Examine op amps that have minimum static power
   - Minimize power dissipation
   - Work at low values of power supply
   - Tradeoff speed for less power

Outline
• Weak inversion
• Methods of creating an overdrive
• Examples
• Summary

Subthreshold Operation
Most micropower op amps use transistors in the subthreshold region. Subthreshold characteristics:

\[ i_D = \frac{W}{L} \cdot I_{DO} \cdot \exp\left(\frac{q}{nkT}(v_{GS})\right) \left(1 + \lambda v_{DS}\right) \]

\[ \Rightarrow \quad g_m = \frac{qI_D}{nkT} \quad \text{and} \quad g_{ds} = \lambda I_D \]

Operation with channel length = \( L_{\text{min}} \) also will normally be in weak inversion.
Two-Stage, Miller Op Amp Operating in Weak Inversion

![Circuit Diagram](Image)

Low frequency response:

\[ A_{vo} = g_{m2}g_{m6} \left( \frac{r_{o2}r_{o4}}{r_{o2} + r_{o4}} \right) \left( \frac{r_{o6}r_{o7}}{r_{o6} + r_{o7}} \right) = \frac{1}{n_2n_6(kT/q)^2(\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \] (No longer \( \propto \frac{1}{\sqrt{I_D}} \))

**GB and SR:**

\[ GB = \frac{I_{D1}}{(n_1kT/q)C} \quad \text{and} \quad SR = \frac{I_{D5}}{C} = 2 \cdot \frac{I_{D1}}{C} = 2GB \left( n_1 \frac{kT}{q} \right) = 2GBn_1V_t \]

Example 7.4-1 Gain and GB Calculations for Subthreshold Op Amp.

Calculate the gain, GB, and SR of the op amp shown above. The currents are \( I_{D5} = 200 \text{ nA} \) and \( I_{D7} = 500 \text{ nA} \). The device lengths are 1 \( \mu \text{m} \). Values for \( n \) are 1.5 and 2.5 for p-channel and n-channel transistors respectively. The compensation capacitor is 5 pF. Use Table 3.1-2 as required. Assume that the temperature is 27 °C. If \( V_{DD} = 1.5V \) and \( V_{SS} = -1.5V \), what is the power dissipation of this op amp?

**Solution**

The low-frequency small-signal gain is,

\[ A_v = \frac{1}{(1.5)(2.5)(0.026)(0.04 + 0.05)(0.04 + 0.05)} = 43,701 \text{ V/V} \]

The gain bandwidth is

\[ GB = \frac{100 \times 10^{-9}}{2.5(0.026)(5 \times 10^{-12})} = 307,690 \text{ rps} \approx 49.0 \text{ kHz} \]

The slew rate is

\[ SR = (2)(307690)(2.5)(0.026) = 0.04 \text{ V/µs} \]

The power dissipation is,

\[ P_{diss} = 3(0.7 \mu A) = 2.1 \mu W \]
Push-Pull Output Op Amp in Weak Inversion

First stage gain is,

\[ A_{vo} = \frac{g_{m2}}{g_{m4}} = \frac{I_{D2}n_4V_t}{I_{D4}n_2V_t} = \frac{I_{D2}n_4}{I_{D4}n_2} \approx 1 \]

Total gain is,

\[ A_{vo} = \frac{g_{m1}(S_6/S_4)}{(g_{ds6} + g_{ds7})} = \frac{(S_6/S_4)}{(\lambda_6 + \lambda_7)n_1V_t} \]

At room temperature \((V_t = 0.0259V)\) and for typical device lengths, gains of 60dB can be obtained.

The GB is,

\[ GB = \frac{g_{m1}}{C} \frac{(S_6)}{(S_4)} = \frac{g_{m1}b}{C} \]

Increasing the Gain of the Previous Op Amp

1.) Can reduce the currents in M3 and M4 and introduce gain in the current mirrors.

2.) Use a cascode output stage (can’t use self-biased cascode, currents are too low).

\[ A_v = \left( \frac{g_{m1} + g_{m2}}{2} \right) R_{out} \]

\[ = \frac{8ds68ds10}{g_{m10}} + \frac{8ds78ds11}{g_{m11}} \]

\[ = \frac{I_5}{I_7^2 \lambda_n^2} + \frac{I_5^2}{I_7} \frac{1}{n_nV_t^2(n_n\lambda_n^2 + n_p\lambda_p^2)} \]

Can easily achieve gains greater than 80dB with power dissipation of less than 1\(\mu\)W.
Increasing the Output Current for Weak Inversion Operation

A significant disadvantage of the weak inversion is that very small currents are available to drive output capacitance so the slew rate becomes very small.

Dynamically biased differential amplifier input stage:

Note that the sinking current for M1 and M2 is
\[ I_{\text{sink}} = I_5 + A(i_2 - i_1) + A(i_1 - i_2) \]
where \((i_2 - i_1)\) and \((i_1 - i_2)\) are only positive or zero.

If \(v_{i1} > v_{i2}\), then \(i_2 > i_1\) and the sinking current is increased by \(A(i_2 - i_1)\).
If \(v_{i2} > v_{i1}\), then \(i_1 > i_2\) and the sinking current is increased by \(A(i_1 - i_2)\).

Dynamically Biased Differential Amplifier - Continued

How much output current is available from this circuit if there is no current gain from the input to output stage?

Assume transistors M18 through M21 are equal to M3 and M4 and that transistors M22 through M27 are all equal.

Let \[ \frac{W_{28}}{L_{28}} = A \left( \frac{W_{26}}{L_{26}} \right) \quad \text{and} \quad \frac{W_{29}}{L_{29}} = A \left( \frac{W_{27}}{L_{27}} \right) \]

The output current available can be found by assuming that \(v_{in} = v_{i1} - v_{i2} > 0\).

\[ \therefore i_1 + i_2 = I_5 + A(i_2 - i_1) \]

The ratio of \(i_2\) to \(i_1\) can be expressed as
\[ \frac{i_2}{i_1} = \exp \left( \frac{v_{in}}{nV_t} \right) \]

Defining the output current as \(i_{OUT} = b(i_2 - i_1)\) and combining the above two equations gives,
\[ i_{OUT} = \frac{bI_5 \exp \left( \frac{v_{in}}{nV_t} \right) - 1}{(1+A) - (A-1)\exp \left( \frac{v_{in}}{nV_t} \right)} \Rightarrow i_{OUT} = \infty \quad \text{when} \quad A = 2.16 \quad \text{and} \quad \frac{v_{in}}{nV_t} = 1 \]

where \(b\) corresponds to any current gain through current mirrors (M6-M4 and M8-M3).
Overdrive of the Dynamically Biased Differential Amplifier

The enhanced output current is accomplished by the use of positive feedback (M28-M2-M19-M28). The loop gain is,

\[ LG = \frac{g_{m28}}{g_{m4}} \frac{g_{m19}}{g_{m26}} = A \frac{g_{m19}}{g_{m4}} = A \]

Note that as the output current increases, the transistors leave the weak inversion region and the above analysis is no longer valid.

Increasing the Output Current for Strong Inversion Operation

An interesting technique is to bias the output transistor of a current mirror in the active region and then during large overdrive cause the output transistor to become saturated causing a significant current gain.

Illustration:
Example 7.4-2  Current Mirror with M2 operating in the Active Region

Assume that M2 has a voltage across the drain-source of 0.1 V_{ds}(sat). Design the W_2/L_2 ratio so that I_1 = I_2 = 100\mu A if W_1/L_1 = 10. Find the value of I_2 if M2 is saturated.

Solution

Using the parameters of Table 3.1-2, we find that the saturation voltage of M2 is

\[ V_{ds1}(sat) = \sqrt{\frac{2I_1}{K_N' (W_2/L_2)}} = \sqrt{\frac{200}{110\cdot 10}} = 0.4264V \]

Now using the active equation of M2, we set I_2 = 100\mu A and solve for W_2/L_2.

\[
100\mu A = K_N' (W_2/L_2) [V_{ds1}(sat) V_{ds2} - 0.5 V_{ds2}^2]
\]

Thus,

\[
100 = 1.883(W_2/L_2) \rightarrow \frac{W_2}{L_2} = 53.12
\]

Now if M2 should become saturated, the value of the output current of the mirror with 100\mu A input would be 531\mu A or a boosting of 5.31 times I_1.

Implementation of the Current Mirror Boosting Concept

\(k = \text{overdrive factor of the current mirror}\)
A Better Way to Achieve the Current Mirror Boosting

It was found that when the current mirror boosting idea illustrated on the previous slide was used that when the current increased through the cascode device (M16) that $V_{GS16}$ increased limiting the increase of $V_{DS12}$. This can be overcome by the following circuit.

\[ \text{Fig. 7.4-7A} \]

SUMMARY

- Operation of transistors is generally in weak inversion
- Boosting techniques are needed to get output sourcing and sinking currents that are larger than that available during quiescent operation
- Be careful about using circuits at weak inversion, i.e. the self-biased cascode will cause the resistor to be too large
SECTION 7.5 – LOW NOISE OP AMPS

Objective
The objective of this presentation is:
1.) Review the principles of low noise design
2.) Show how to reduce the noise of op amps

Outline
• Review of noise analysis
• Low noise op amps
• Low noise op amps using lateral BJTs
• Low noise op amps using doubly correlated sampling
• Summary

Introduction
Why do we need low noise op amps?
Dynamic range:

\[
\text{Signal-to-noise ratio (SNR)} = \frac{\text{Maximum RMS Signal}}{\text{Noise}}
\]
(SNDR includes both noise and distortion)

Consider a 14 bit digital-to-analog converter with a 1V reference with a bandwidth of 1MHz.

\[
\text{Maximum RMS signal is } \frac{0.5V}{\sqrt{2}} = 0.3535 \text{ Vrms}
\]

A 14 bit D/A converter requires 14x6dB dynamic range or 84 dB or 16,400.

\[
\therefore \quad \text{The value of the least significant bit (LSB)} = \frac{0.3535}{16,400} = 21.6\mu\text{Vrms}
\]

If the equivalent input noise of the op amp is not less than this value, then the LSB cannot be resolved and the D/A converter will be in error. An op amp with an equivalent input-noise spectral density of 10nV/\sqrt{Hz} will have an rms noise voltage of approximately \((10nV/\sqrt{Hz})(1000\sqrt{Hz}) = 10\mu\text{Vrms in a 1MHz bandwidth}\).
**Transistor Noise Sources (Low-Frequency)**

Drain current model:

\[ i_n^2 = \left[ \frac{8kTg_m}{3} + \frac{(KF)I_D}{fC_{ox}L^2} \right] \]

or

\[ i_n^2 = \left[ \frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2} \right] \text{ if } v_{BS} \neq 0 \]

Recall that \( \eta = \frac{g_{mbs}}{g_m} \)

Gate voltage model assuming common source operation:

\[ e_n^2 = \left[ \frac{8kT}{3g_m} + \frac{KfC_{ox}WLK'}{g_m^2} \right] \]

or

\[ e_n^2 = \left[ \frac{8kT}{3g_m(1+\eta)} + \frac{KfC_{ox}WLK'}{2g_m^2} \right] \text{ if } v_{BS} \neq 0 \]

---

**Minimization of Noise in Op Amps**

1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)

2.) To minimize the 1/f noise:
   a.) Use PMOS input transistors with appropriately selected dc currents and \( W \) and \( L \) values.
   b.) Use lateral BJTs to eliminate the 1/f noise.
   c.) Use chopper stabilization to reduce the low-frequency noise.

**Noise Analysis**

1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)

2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.

3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.
A Low-Noise, Two-Stage, Miller Op Amp

The total output-noise voltage spectral density, $e_{\text{to}}^2$, is as follows where $g_{m8}(\text{eff}) = 1/r_{ds1}$,

$$e_{\text{to}}^2 = g_{m6}^2 R_{II}^2 \left[ e_{n6}^2 + e_{n7}^2 + R_e^2 \left( g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 + \left( \frac{e_{n8}}{r_{ds1}} \right)^2 + \left( \frac{e_{n9}}{r_{ds2}} \right)^2 \right) \right]$$

Divide by $(g_{m1} R_I g_{m6} R_{II})^2$ to get the eq. input-noise voltage spectral density, $e_{\text{eq}}^2$, as

$$e_{\text{eq}}^2 = \frac{2 e_{n1}^2}{\left( g_{m1} g_{m6} R_{II} R_I \right)^2} = 2 e_{n1}^2 + 2 \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left( \frac{e_{n3}}{e_{n1}} \right)^2 + 2 \left( \frac{g_{m2}}{g_{m1}} \right)^2 \left( \frac{e_{n2}}{e_{n1}} \right)^2 + \frac{e_{n8}}{r_{ds1}^2} e_{n1}^2$$

where $e_{n6} = e_{n7}$, $e_{n3} = e_{n4}$, $e_{n1} = e_{n2}$ and $e_{n8} = e_{n9}$ and $g_{m1} R_I$ is large.

1/f Noise of a Two-Stage, Miller Op Amp

Consider the 1/f noise:

Therefore the noise generators are replaced by,

$$e_{ni} = \frac{B}{f W L_i} \quad (\text{V}^2/\text{Hz}) \quad \text{and} \quad i_{ni} = \frac{2 BK' I_i}{f L_i^2} \quad (\text{A}^2/\text{Hz})$$

Therefore, the approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2 e_{n1}^2 \left[ 1 + \left( \frac{K' B' N}{K P B P} \right)^2 \left( \frac{L_1}{L_3} \right)^2 \right] \quad (\text{V}^2/\text{Hz})$$

Comments:

- Because we have selected PMOS input transistors, $e_{n1}^2$ has been minimized if we choose $W_1 L_1$ ($W_2 L_2$) large.
- Make $L_1 << L_3$ to remove the influence of the second term in the brackets.
Thermal Noise of a Two-Stage, Miller Op Amp

Let us focus next on the thermal noise:
The noise generators are replaced by,
\[ \frac{2}{n_i} \approx \frac{8kT}{3g_m} \text{ (V}^2/\text{Hz)} \quad \text{and} \quad i_{ni} \approx \frac{8kTg_m}{3} \text{ (A}^2/\text{Hz)} \]
where the influence of the bulk has been ignored.
The approximate equivalent input-noise voltage spectral density is,
\[ \frac{2}{e_{eq}} = 2e_n \left[ 1 + \left( \frac{g_m3}{g_m2} \right) \left( \frac{e_n3}{e_n1} \right) \right] = 2e_n \left[ 1 + \sqrt[3]{\frac{K_NW_3L_1}{K_PW_1L_3}} \right] \text{ (V}^2/\text{Hz)} \]

Comments:
• The choices that reduce the 1/f noise also reduce the thermal noise.

Noise Corner:
Equating the equivalent input-noise voltage spectral density for the 1/f noise and the thermal noise gives the noise corner, \( f_c \), as
\[ f_c = \frac{3g_mB}{8kTWL} \]

Example 7.5-1  Design of A Two-Stage, Miller Op Amp for Low 1/f Noise

Use the parameters of Table 3.1-2 along with the value of \( KF = 4 \times 10^{-28} \text{ F} \cdot \text{A} \) for NMOS and \( 0.5 \times 10^{-28} \text{ F} \cdot \text{A} \) for PMOS and design the previous op amp to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

Solution
1.) The 1/f noise constants, \( B_N \) and \( B_P \) are calculated as follows.
\[ B_N = \frac{KF}{2C_{ox}K_N^+} = \frac{4 \times 10^{-28} \text{ F} \cdot \text{A}}{2 \cdot 2.47 \times 10^{-4} \text{ F/m}^2 \cdot 1.1 \times 10^{-6} \text{ A}^2/\text{V}} = 7.36 \times 10^{-22} \text{ (V} \cdot \text{m})^2 \]
and
\[ B_P = \frac{KF}{2C_{ox}K_P^+} = \frac{0.5 \times 10^{-28} \text{ F} \cdot \text{A}}{2 \cdot 2.47 \times 10^{-4} \text{ F/m}^2 \cdot 5 \times 10^{-6} \text{ A}^2/\text{V}} = 2.02 \times 10^{-22} \text{ (V} \cdot \text{m})^2 \]
2.) Now select the geometry of the various transistors that influence the noise performance.

To keep \( e_{n1}^2 \) small, let \( W_1 = 100 \mu \text{m} \) and \( L_1 = 1 \mu \text{m} \). Select \( W_3 = 100 \mu \text{m} \) and \( L_3 = 20 \mu \text{m} \) and let \( W_8 \) and \( L_8 \) be the same as \( W_1 \) and \( L_1 \) since they little influence on the noise.
Example 7.5-1 - Continued

Of course, M1 is matched with M2, M3 with M4, and M8 with M9.

\[ e_{n1} = \frac{B_P}{fW_1L_1} = \frac{2.02 \times 10^{-22}}{f \times 100 \mu m \times 1 \mu m} = \frac{2.02 \times 10^{-12}}{f} \text{ (V}^2/\text{Hz)} \]

\[ e_{eq} = 2 \times 2.02 \times 10^{-12} \left[ 1 + \left( \frac{110.736}{50 \times 2.02} \right)^2 \right] = \frac{4.04 \times 10^{-12}}{f} \times 1.1606 = \frac{4.689 \times 10^{-12}}{f} \text{ (V}^2/\text{Hz)} \]

Note at 100Hz, the voltage noise in a 1Hz band is \( \approx 4.7 \times 10^{-14} \text{V}^2/\text{Hz} \) or \( 0.216 \mu \text{V} \) (rms).

3.) The thermal noise at room temperature is

\[ e_{n1} = \frac{8kT}{3g_m} = \frac{8 \times 1.38 \times 10^{-23} \cdot 300}{3 \cdot 707 \times 10^{-6}} = 1.562 \times 10^{-17} \text{ (V}^2/\text{Hz)} \]

which gives

\[ e_{eq} = 2 \times 1.562 \times 10^{-17} \left[ 1 + \sqrt{\frac{110 \cdot 100}{50 \cdot 100 \cdot 20}} \right] = 3.124 \times 10^{-17} \cdot 1.33 = 4.164 \times 10^{-17} \text{ (V}^2/\text{Hz)} \]

4.) The noise corner frequency is found by equating the two expressions for \( e_{eq} \) to get

\[ f_c = \frac{4.689 \times 10^{-12}}{4.164 \times 10^{-17}} = 112.6 \text{kHz} \]

This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

Example 7.5-1 - Continued

5.) To estimate the rms noise in the bandwidth from 1Hz to 100,000Hz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

\[ V_{eq}(\text{rms})^2 = \int_{1}^{10^5} \frac{4.689 \times 10^{-12}}{f} df = 4.689 \times 10^{-12} \left[ \ln(100,000) - \ln(1) \right] \]

\[ = 0.540 \times 10^{-10} \text{ (Vrms}^2/\text{Vrms} = 7.34 \mu \text{V rms} \]

The maximum signal in rms is 0.353V. Dividing this by 7.34\mu V gives 48,044 or 93.6dB which is equivalent to about 15 bits of resolution.

6.) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.
Lateral BJT

Since the $1/f$ noise is associated with current flowing at the surface of the channel, the lateral BJT offers a lower $1/f$ noise input device because the majority of current flows beneath the surface.

![Cross-section of a NPN lateral BJT.](image)

**Comments:**
- Base of the BJT is the well
- Two collectors—one horizontal (desired) and one vertical (undesired)
- Collector efficiency is defined as $\frac{\text{Lateral collector current}}{\text{Total collector current}}$ and is 60-70%
- Reverse biased collector-base acts like a photodetector and is often used for light-sensing purposes
- A triple well process allows the vertical collector current to avoid the substrate.

Field-Aided Lateral BJT

Polysilicon gates are used to ensure that the region beneath the gate does not invert forcing all current flow away from the surface and further eliminating the $1/f$ noise.

![Cross-section of a field-aided NPN lateral BJT.](image)

The effective base length becomes the minimum channel length minus the lateral diffusion and can be quite small for deep submicron technologies. This means the beta and frequency response should be quite good.
Physical Layout of a Lateral PNP Transistor

Experimental Results for a x40 PNP lateral BJT:

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor area</td>
<td>0.006mm²</td>
</tr>
<tr>
<td>Lateral β</td>
<td>90</td>
</tr>
<tr>
<td>Lateral efficiency</td>
<td>70%</td>
</tr>
<tr>
<td>Base resistance</td>
<td>150Ω</td>
</tr>
<tr>
<td>$e_n$ at 5 Hz</td>
<td>2.46nV/√Hz</td>
</tr>
<tr>
<td>$e_n$ at midband</td>
<td>1.92nV/√Hz</td>
</tr>
<tr>
<td>$f_c(e_n)$</td>
<td>3.2Hz</td>
</tr>
<tr>
<td>$i_n$ at 5 Hz</td>
<td>3.53µA/√Hz</td>
</tr>
<tr>
<td>$i_n$ at midband</td>
<td>0.61µA/√Hz</td>
</tr>
<tr>
<td>$f_c(i_n)$</td>
<td>162 Hz</td>
</tr>
<tr>
<td>$f_T$</td>
<td>85 MHz</td>
</tr>
<tr>
<td>Early voltage</td>
<td>16V</td>
</tr>
</tbody>
</table>

Generally, the above structure is made as small as possible and then paralleled with identical geometries to achieve the desired BJT.

CMOS Analog Circuit Design © P.E. Allen - 2006

Low-Noise Op Amp using Lateral BJTs at the Input

Experimental noise performance:

CMOS Analog Circuit Design © P.E. Allen - 2006
### Summary of Experimental Performance for the Low-Noise Op Amp

<table>
<thead>
<tr>
<th>Experimental Performance</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit area (1.2μm)</td>
<td>0.211 mm²</td>
</tr>
<tr>
<td>Supply Voltages</td>
<td>±2.5 V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>2.1 mA</td>
</tr>
<tr>
<td>-3dB frequency (at a gain of 20.8 dB)</td>
<td>11.1 MHz</td>
</tr>
<tr>
<td>$e_n$ at 1Hz</td>
<td>23.8 nV/√Hz</td>
</tr>
<tr>
<td>$e_n$ (midband)</td>
<td>3.2 nV/√Hz</td>
</tr>
<tr>
<td>$f_c(e_n)$</td>
<td>55 Hz</td>
</tr>
<tr>
<td>$i_n$ at 1Hz</td>
<td>5.2 pA/√Hz</td>
</tr>
<tr>
<td>$i_n$ (midband)</td>
<td>0.73 pA/√Hz</td>
</tr>
<tr>
<td>$f_c(i_n)$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Input bias current</td>
<td>1.68 μA</td>
</tr>
<tr>
<td>Input offset current</td>
<td>14.0 nA</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>1.0 mV</td>
</tr>
<tr>
<td>CMRR(DC)</td>
<td>99.6 dB</td>
</tr>
<tr>
<td>PSRR+(DC)</td>
<td>67.6 dB</td>
</tr>
<tr>
<td>PSRR-(DC)</td>
<td>73.9 dB</td>
</tr>
<tr>
<td>Positive slew rate (60 pF, 10 kΩ load)</td>
<td>39.0 V/μS</td>
</tr>
<tr>
<td>Negative slew rate (60 pF, 10 kΩ load)</td>
<td>42.5 V/μS</td>
</tr>
</tbody>
</table>

---

### Chopper-Stabilized Op Amps - Doubly Correlated Sampling (DCS)

Illustration of the use of chopper stabilization to remove the undesired signal, $v_{u}$, from the desired signal, $v_{in}$.
Chopper-Stabilized Amplifier

Chopper-stabilized Amplifier:

Circuit equivalent during $\phi_1$ phase:

Circuit equivalent during the $\phi_2$ phase:

$$v_{ueq} = -v_{u1} + \frac{v_{u2}}{A_1}, \quad v_{ueq(aver)} = \frac{v_{u2}}{A_1}$$

Fig. 7.5-10

Experimental Noise Response of the Chopper-Stabilized Amplifier

Comments:
- The switches in the chopper-stabilized op amp introduce a thermal noise equal to $kT/C$ where $k$ is Boltzmann’s constant, $T$ is absolute temperature and $C$ are capacitors charged by the switches (parasitics in the case of the chopper-stabilized amplifier).
- Requires two-phase, non-overlapping clocks.
- Trade-off between the lowering of $1/f$ noise and the introduction of the $kT/C$ noise.
**Improved Chopper Operation**

In some cases, there are spurious signals in the neighborhood of the chopping frequencies and its harmonics. These spurious signals such as common-mode interference can mix to the baseband since the chopper amplifier is a time variant system and therefore inherently nonlinear.

A bandpass filter centered at the clock frequency can be used to eliminate the aliasing of the spurious signals and achieve a reduction in effective offset.

Let \( \epsilon = \frac{f_c - f_o}{f_o} \) and \( \sigma_{\epsilon} \) be a given bound of \( \epsilon \). It can be shown† that the achievable effective offset reduction, \( EOR \), and the optimum \( Q \) for the bandpass filter, \( Q_{opt} \), is

\[
EOR = \frac{8Q}{\sqrt{1 + 8Q^2\epsilon^2}}, \quad \epsilon << 1
\]

and

\[
Q_{opt} = \frac{1}{\sqrt{8\sigma_{\epsilon}}}
\]

Improvements of 14dB reduction in effective offset are possible for \( \epsilon = 0.8\% \).

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**SUMMARY**

- Primary sources of noise for CMOS circuits is thermal and 1/f
- Noise analysis:
  1. Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)
  2. Find the output noise voltage across an open-circuit or output noise current into a short circuit.
  3. Reflect the total output noise back to the input resulting in the equivalent input noise voltage.
- Noise is reduced in op amps by making the input stage gain as large as possible and reducing the noise of this stage as much as possible.
- The input stage noise can be reduced by using lateral BJTs (particularly the 1/f noise)
- Doubly correlated sampling can transfer the noise at low frequencies to the clock frequency (this technique is used to achieve low input offset voltage op amps).
SECTION 7.6 – LOW VOLTAGE OP AMPS

Objective
The objective of this presentation is:

1.) How to design standard circuit blocks with reduced power supply voltage
2.) Introduce new methods of designing low voltage circuits

Outline

• Low voltage input stages
• Low voltage gain stages
• Low voltage bias circuits
• Low voltage op amps
• Summary

Implications of Low-Voltage, Strong-Inversion Operation

• Reduced power supply means decreased dynamic range
• Nonlinearity will increase because the transistor is working close to $V_{DS}(sat)$
• Large values of $\lambda$ because the transistor is working close to $V_{DS}(sat)$
• Increased drain-bulk and source-bulk capacitances because they are less reverse biased.
• Large values of currents and $W/L$ ratios to get high transconductance
• Small values of currents and large values of $W/L$ will give small $V_{DS}(sat)$
• Severely reduced input common mode range
• Switches will require charge pumps
What are the Limits of Power Supply?
The limit comes when there is no signal range left when the dc drops are subtracted from $V_{DD}$.

Minimum power supply (no signal swing range):

$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$

For differential amplifiers, the minimum power supply is:

$$V_{DD}(\text{min.}) = 3V_{ON}$$

However, to have any input common mode range, the effective minimum power supply is,

$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$

Minimum Power Supply Limit – Continued

The previous consideration of the differential amplifier did not consider getting the signal out of the amplifier. This will add another $V_{ON}$.

Therefore,

$$V_{DD}(\text{min.}) = V_T + 3V_{ON}$$

This could be reduced to $3V_{ON}$ with the floating battery but its implementation probably requires more than $3V_{ON}$ of power supply.

Note the output signal swing is $V_T + V_{ON}$ while the input common range is $V_{ON}$. 
LOW VOLTAGE INPUT STAGES

Input Common Mode Voltage Range

Minimum power supply \((ICMR = 0)\):
\[
V_{DD}(\text{min}) = V_{SD3}(\text{sat}) - V_{T1} + V_{GS1} + V_{DS5}(\text{sat}) = V_{SD3}(\text{sat}) + V_{DS1}(\text{sat}) + V_{DS5}(\text{sat})
\]

Input common-mode range:
\[
V_{icm}(\text{upper}) = V_{DD} - V_{SD3}(\text{sat}) + V_{T1}
\]
\[
V_{icm}(\text{lower}) = V_{DS5}(\text{sat}) + V_{GS1}
\]

If the threshold magnitudes are 0.7V, \(V_{DD} = 1.5V\) and the saturation voltages are 0.3V, then
\[
V_{icm}(\text{upper}) = 1.5 - 0.3 + 0.7 = 1.9V \quad \text{and} \quad V_{icm}(\text{lower}) = 0.3 + 1.0 = 1.3V
\]
giving an \(ICMR\) of 0.6V.

Increasing \(ICMR\) using Parallel Input Stages

Turn-on voltage for the n-channel input:
\[
V_{onn} = V_{DSN5}(\text{sat}) + V_{GSN1}
\]

Turn-on voltage for the p-channel input:
\[
V_{onp} = V_{DD} - V_{SDP5}(\text{sat}) - V_{SGP1}
\]
The sum of \(V_{onn}\) and \(V_{onp}\) equals the minimum power supply.

Regions of operation:
\[
V_{DD} > V_{icm} > V_{onp}: \quad \text{(n-channel on and p-channel off)} \quad g_m(\text{eq}) = g_{mN}
\]
\[
V_{onp} > V_{icm} \geq V_{onn}: \quad \text{(n-channel on and p-channel on)} \quad g_m(\text{eq}) = g_{mN} + g_{mP}
\]
\[
V_{onn} > V_{icm} > 0: \quad \text{(n-channel off and p-channel on)} \quad g_m(\text{eq}) = g_{mP}
\]

where \(g_m(\text{eq})\) is the equivalent input transconductance of the above input stage, \(g_{mN}\) is the input transconductance for the n-channel input and \(g_{mP}\) is the input transconductance for the p-channel input.
Removing the Nonlinearity in Transconductances as a Function of ICMR

Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

Three regions of operation depending on the value of $V_{icm}$:

1.) $V_{icm} < V_{onn}$: n-channel diff. amp. off and p-channel on with $I_p = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_P W_P}{L_P}} 2\sqrt{I_b}$$

2.) $V_{onn} < V_{icm} < V_{onp}$: both on with $I_n = I_p = I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N W_N}{L_N}} \sqrt{I_b} + \sqrt{\frac{K_P W_P}{L_P}} \sqrt{I_b}$$

3.) $V_{icm} > V_{onp}$: p-channel diff. amp. off and n-channel on with $I_n = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N W_N}{L_N}} 2\sqrt{I_b}$$

How Does the Current Compensation Work?

Set $V_{B1} = V_{onn}$ and $V_{B2} = V_{onp}$.

Result:

The above techniques and many similar ones are good for power supply values down to about 1.5V. Below that, different techniques must be used or the technology must be modified (natural devices).
**Natural Transistors**

Natural or native NMOS transistors normally have a threshold voltage around 0.1V before the threshold is increased by increasing the $p$ concentration in the channel.

If these transistors are characterized, then they provide a means of achieving low voltage operation.

Minimum power supply ($ICMR = 0$):

$$V_{DD}(\text{min}) = 3V_{ON}$$

Input common mode range:

- $V_{icm}^{\text{(upper)}} = V_{DD} - V_{ON} + V_T^{\text{(natural)}}$
- $V_{icm}^{\text{(lower)}} = 2V_{ON} + V_T^{\text{(natural)}}$

If $V_T^{\text{(natural)}} \approx V_{ON} = 0.1V$, then

- $V_{icm}^{\text{(upper)}} = V_{DD}$
- $V_{icm}^{\text{(lower)}} = 3V_{ON} = 0.3V$

Therefore,

$$ICMR = V_{DD} - 3V_{ON} = V_{DD} - 0.3V \quad \Leftrightarrow \quad V_{DD}(\text{min}) \approx 1V$$

---

**Bulk-Driven MOSFET**

A depletion device would permit large $ICMR$ even with very small power supply voltages because $V_{GS}$ is zero or negative.

When a MOSFET is driven from the bulk with the gate held constant, it acts like a depletion transistor.

Cross-section of an n-channel bulk-driven MOSFET:

Large signal equation:

$$i_D = \frac{K_N W}{2L} [V_{GS} - V_{TD} - \gamma \sqrt{2 |\phi_F|} - V_{BS} + \gamma \sqrt{2 |\phi_F|}]^2$$

Small-signal transconductance:

$$g_{ms} = \frac{\gamma \sqrt{(2K_N W/L)}i_D}{2\sqrt{2 |\phi_F|} - V_{BS}}$$
Bulk-Driven MOSFET - Continued

Transconductance characteristics:

Saturation: \( V_{DS} > V_{BS} - V_P \) gives,
\[
V_{BS} = V_P + V_{ON}
\]
\[
i_D = I_{DSS}\left(1 - \frac{V_{BS}}{V_P}\right)^2
\]

Comments:
- \( g_m \) (bulk) > \( g_m \) (gate) if \( V_{BS} > 0 \)
  (forward biased)
- Noise of both configurations are the same (any differences comes from the gate versus bulk noise)
- Bulk-driven MOSFET tends to be more linear at lower currents than the gate-driven MOSFET
- Very useful for generation of \( I_{DSS} \) floating current sources.

---

Bulk-Driven, n-channel Differential Amplifier

What is the \( ICMR \)?
\[
V_{icm}(\text{min}) = V_S + V_{DS5}(\text{sat}) + V_{BS1} = V_S + V_{DS5}(\text{sat}) - |V_P| + V_{DS1}(\text{sat})
\]
Note that \( V_{icm} \) can be less than \( V_S \) if \( |V_P| > V_{DS5}(\text{sat}) + V_{DS1}(\text{sat}) \)
\[
V_{icm}(\text{max}) = \text{?}
\]

As \( V_{icm} \) increases, the current through M1 and M2 is constant so the source increases. However, the gate voltage stays constant so that \( V_{GS1} \) decreases. Since the current must remain constant through M1 and M2 because of M5, the bulk-source voltage becomes less negative causing \( V_{TN1} \) to decrease and maintain the currents through M1 and M2 constant. If \( V_{icm} \) is increased sufficiently, the bulk-source voltage will become positive. However, current does not start to flow until \( V_{BS} \) is greater than 0.3 volts so the effective \( V_{icm}(\text{max}) \) is
\[
V_{icm}(\text{max}) \approx V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{BS1}.
\]
### Illustration of the ICMR of the Bulk-Driven, Differential Amplifier

![Graph showing the Bulk-Source Current vs. Input Common-Mode Voltage](image)

**Fig. 7.6-10A**

**Comments:**
- Effective ICMR is from \( V_{SS} \) to \( V_{DD} -0.3 \) V
- The transconductance of the input stage can vary as much as 100% over the ICMR which makes it very difficult to compensate

---

### Reduction of \( V_T \) through Forward Biasing the Bulk-Source

The bulk can be used to reduce the threshold sufficiently to permit low voltage applications. The key is to control the amount of forward bias of the bulk-source.

**Current-Driven Bulk Technique**

\[
I_{BB} = \frac{I_{max}}{\beta_{CS} + \beta_{CD} + 1}
\]

---


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**Current-Driven Bulk Technique**

Bias circuit for keeping the $I_{max}$ defined independent of BJT betas.

Note:
\[
I_{D,C} = I_{CD} + I_D \\
I_{S,E} = I_D + I_E + I_R
\]

The circuit feedback causes a bulk bias current $I_{BB}$ and hence a bias voltage $V_{BIAS}$ such that
\[
I_{S,E} = I_D + I_{BB}(1+\beta CS + \beta CD) + I_R
\]

Use $V_{Bias1}$ and $V_{Bias2}$ to set $I_{D,C} \approx 1.1I_D$ , $I_{S,E} \approx 1.3I_D$ and $I_R \approx 0.1I_D$ which sets $I_{BB}$ at 0.1$I_D$ assuming we can neglect $I_{CS}$ with respect to $I_{CD}$.

For this circuit to work, the following conditions must be satisfied:
\[
V_{BE} < V_{TN} + I_{RR} \quad \text{and} \quad |V_{TP}| + V_{DS(sat)} < V_{TN} + I_{RR}
\]

If $|V_{TP}| > V_{TN}$, then the level shifter $I_{RR}$ can be eliminated.

---

**LOW VOLTAGE GAIN STAGES**

**Cascade Stages**

Simple cascade of inverters:

The problem with this approach is the number of poles that occur (one per stage) if the amplifier is to be used in a closed loop application.
Nested Miller Compensation

Principle: Use Miller compensation to split the poles within a feedback loop.

Compensating Results:
1) $C_m1$ pushes $p_4$ to higher frequencies and $p_3$ down to lower frequencies
2) $C_m2$ pushes $p_2$ to higher frequencies and $p_1$ down to lower frequencies
3) $C_m3$ pushes $p_3$ to higher frequencies (feedback path) & pulls $p_1$ further to lower frequencies

Equations:

\[
GB = \frac{g_m1}{C_m3} \quad p_2 = \frac{g_m2}{C_m3} \quad p_3 = g_m3C_m3/(C_m1C_m2) \quad p_4 = \frac{g_m4}{CL}
\]

Design:

\[
GB < p_2, p_3, p_4
\]

Illustration of the Nested Miller Compensation Technique

This approach is complicated by the feedforward creating RHP zeros.
**Elimination of the RHP Zeros**

The following are least three ways in which the RHP zeros can be eliminated.

1.) Nulling resistor.  
2.) Feedback only – buffer.  
3.) Feedback only – gain.

\[ z_1 = \frac{1}{C_c(1/g_m - R_z)} \]

Increases the minimum power supply by \( V_{ON} \).

Increases the pole and increases the minimum power supply by \( V_{ON} \).

---

**Use of LHP Zeros to Compensate Cascaded Amplifiers**

Principle: Feedforward around a noninverting stage creates a LHP zero or inverting feedforward around an inverting stage also creates a LHP zero.

Example of Multipath, Nested Miller Compensation†:

Unfortunately, the analysis becomes quite complex and for the details refer to the reference below.

**Cascoding**

Possibilities that trade off output resistance for headroom:

- **No Cascoding**
- **Normal Cascoding**
- **Reduced Headroom Cascoding**
- **Gate-Connected Cascode**

<table>
<thead>
<tr>
<th></th>
<th>No Cascode</th>
<th>Normal Cascode</th>
<th>Reduced Headroom Cascode</th>
<th>Gate-Connected Cascode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{v_{out}}{V_{on1}}$</td>
<td>1</td>
<td>$1 + \sqrt{\frac{\beta_1}{\beta_2}}$</td>
<td>$1 + \sqrt{\frac{\beta_1}{\beta_2}} (2x-x^2)$</td>
<td>$2x + \sqrt{\frac{\beta_1}{\beta_2}} (2x-x^2)$</td>
</tr>
<tr>
<td>$\frac{R_{out}}{r_{ds}}$</td>
<td>1</td>
<td>$\sqrt{\frac{2\beta_2}{\lambda^2 I_D}}$</td>
<td>$\sqrt{2\beta_2 (x-0.5x^2)} \div \sqrt{\beta_1 (1-x) + \lambda \sqrt{I_D} \sqrt{x-0.5x^2}}$</td>
<td>$\sqrt{2\beta_2 (x-0.5x^2)} \div \sqrt{\beta_1 (1-x) + \lambda \sqrt{I_D} \sqrt{x-0.5x^2}}$</td>
</tr>
</tbody>
</table>

Note: $v_{DS}(active) = x \cdot V_{on1} = x \cdot (V_{GG} - V_T)$

$x = 0.1$ and $\beta_2 = 9 \beta_1 \rightarrow v_{out} = 1.145 V_{on1}$ and $R_{out} = 1.45 r_{ds}$ for reduced headroom cascode.

---

**Solutions to the Low Headroom Problem – High Voltage Tolerant Circuits**

High voltage tolerant transistors in standard CMOS†:

- **Thick oxide transistor**
- **Upper gate switched to highest potential**
- **Retractable cascode composite transistor**

(Transistor symbols with additional separation between the gate line and the channel line represent thick oxide transistors.)

---


CMOS Analog Circuit Design © P.E. Allen - 2006
LOW VOLTAGE BIAS CIRCUITS

A Low-Voltage Current Mirror with Wide Input and Output Swings
The current mirror below requires a power supply of $V_T + 3V_{ON}$ and has a $V_{in}(\text{min}) = V_{ON}$ and a $V_{out}(\text{min}) = 2V_{ON}$ (less for the regulated cascode output mirror).

![Current Mirror Diagram](image)

Low-Voltage Current Mirrors using the Bulk-Driven MOSFET
The biggest problem with current mirrors is the large minimum input voltage required for previously examined current mirrors.
If the bulk-driven MOSFET is biased with a current that exceeds $I_{DSS}$ then it is enhancement and can be used as a current mirror.

![Bulk-Driven MOSFET Diagram](image)

The cascode current mirror gives a minimum input voltage of less than 0.5V for currents less than 100 μA.
Bandgap Topologies Compatible with Low Voltage Power Supply

Voltage-mode bandgap topology.  
Current-mode bandgap topology.  
Voltage-current mode bandgap topology.  

Method of Generating Currents with $V_{BE}$ and PTAT Temperature Coefficients

$$V_{out1} = I_{PTAT} R_2 = \frac{V_{PTAT}}{R_1} R_2 = V_{PTAT} \frac{R_2}{R_1}$$

$$V_{out2} = I_{VBE} R_4 = \frac{V_{BE}}{R_3} R_4 = V_{BE} \frac{R_4}{R_3}$$
Technique for Canceling the Bandgap Curvature

\[ I_{NL} = \begin{cases} 0 & , \quad K_2I_{VBE} > K_1I_{PTAT} \\ K_1I_{PTAT} - K_2I_{VBE} & , \quad K_2I_{VBE} < K_1I_{PTAT} \end{cases} \]

The combination of the above concept with the previous slide yielded a curvature-corrected bandgap reference of 0.596\(V\) with a TC of 20ppm/\(C\)\(°\) from -15\(C\)\(°\) to 90\(C\)\(°\) using a 1.1\(V\) power supply.\(\dagger\) In addition, the line regulation was 408 ppm/V for 1.2\(\leq V_{DD}\leq 10V\) and 2000 ppm/V for 1.1\(\leq V_{DD}\leq 10V\). The quiescent current was 14\(\mu A\).


LOW VOLTAGE OP AMPS

A Low Voltage Op Amp using Normal Technology

\[ V_{DD}(\text{min}) = 3V_{ON} + V_T \ (ICMR = V_{ON}) : \]

\[ V_{PP1} \]
\[ M3 \quad M4 \]
\[ V_{PP2} \]
\[ M6 \quad M7 \]
\[ C_c \]
\[ v_{IN} \]
\[ v_{OUT} \]
\[ v_{NB1} \]
\[ M5 \quad M8 \quad M9 \]
\[ M10 \]

Performance:
Gain \( \approx g_m r_{ds} \)
Miller compensated
Output swing is \( V_{DD} - 2V_{ON} \)
Max. CM input = \( V_{DD} \)
Min. CM input = \( 2V_{ON} + V_T \)
A Low-Voltage, Wide ICMR Op Amp

\[ V_{DD}(\text{min}) = 4V_{ON} + 2V_T \]  
(\text{ICMR} = V_{DD})

\[ V_{DD} \]

\[ V_{DD} - V_T - V_{DS} \text{(sat)} \]

\[ V_{DD} - V_T - 2V_{DS} \text{(sat)} \]

\[ V_T + 2V_{DS} \text{(sat)} \]

\[ V_T + V_{DS} \text{(sat)} \]

041231-15

Performance:

Gain \approx g_m^2 r_{ds}^2, \text{ self compensated, and output swing is } V_{DD} - 4V_{ON}

An Alternate Low-Voltage, Wide ICMR Op Amp

\[ V_{DD}(\text{min}) = 4V_{ON} + 2V_T \]  
(\text{ICMR} = V_{DD})

\[ V_{PB1} \]

\[ V_{PB2} \]

\[ V_{NB2} \]

\[ V_{NB1} \]

060804-02
A 1-Volt, Two-Stage Op Amp
Uses a bulk-driven differential input amplifier.

![Circuit Diagram](Fig. 7.6-18)

**Performance of the 1-Volt, Two-Stage Op Amp**

<table>
<thead>
<tr>
<th>Specification ($V_{DD}$=0.5V, $V_{SS}$=-0.5V)</th>
<th>Measured Performance ($C_L$ = 22pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC open-loop gain</td>
<td>49dB ($V_{icm}$ mid range)</td>
</tr>
<tr>
<td>Power supply current</td>
<td>300μA</td>
</tr>
<tr>
<td>Unity-gainbandwidth (GB)</td>
<td>1.3MHz ($V_{icm}$ mid range)</td>
</tr>
<tr>
<td>Phase margin</td>
<td>57° ($V_{icm}$ mid range)</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>±3mV</td>
</tr>
<tr>
<td>Input common mode voltage range</td>
<td>-0.475V to 0.450V</td>
</tr>
<tr>
<td>Output swing</td>
<td>-0.475V to 0.491V</td>
</tr>
<tr>
<td>Positive slew rate</td>
<td>+0.7V/μsec</td>
</tr>
<tr>
<td>Negative slew rate</td>
<td>-1.6V/μsec</td>
</tr>
<tr>
<td>THD, closed loop gain of -1V/V</td>
<td>-60dB (0.75Vp-p, 1kHz sinewave)</td>
</tr>
<tr>
<td></td>
<td>-59dB (0.75Vp-p, 10kHz sinewave)</td>
</tr>
<tr>
<td>THD, closed loop gain of +1V/V</td>
<td>-59dB (0.75Vp-p, 1kHz sinewave)</td>
</tr>
<tr>
<td></td>
<td>-57dB (0.75Vp-p, 10kHz sinewave)</td>
</tr>
<tr>
<td>Spectral noise voltage density</td>
<td>367nV/√Hz @ 1kHz</td>
</tr>
<tr>
<td></td>
<td>181nV/√Hz @ 10kHz</td>
</tr>
<tr>
<td></td>
<td>81nV/√Hz @ 100kHz</td>
</tr>
<tr>
<td></td>
<td>444nV/√Hz @ 1MHz</td>
</tr>
<tr>
<td>Positive Power Supply Rejection</td>
<td>61dB at 10kHz, 55dB at 100kHz, 22dB at 1MHz</td>
</tr>
<tr>
<td>Negative Power Supply Rejection</td>
<td>45dB at 10kHz, 27dB at 100kHz, 5dB at 1MHz</td>
</tr>
</tbody>
</table>
A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique

Transistors with forward-biased bulks are in a shaded box.
For large common mode input changes, $C_x$, is necessary to avoid slewing in the input stage.
To get more voltage headroom at the output, the transistors of the cascode mirror have their bulks current driven.

Experimental results:

<table>
<thead>
<tr>
<th></th>
<th>Supply Voltage</th>
<th>Common-mode input range</th>
<th>High gain output range</th>
<th>Output saturation limits</th>
<th>DC gain</th>
<th>Gain-Bandwidth</th>
<th>Slew-Rate ($C_L=20\text{pF}$)</th>
<th>Phase margin ($C_L=20\text{pF}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.0V</td>
<td>0.0V-0.65V</td>
<td>0.35V-0.75V</td>
<td>0.1V-0.9V</td>
<td>62dB-69dB</td>
<td>2.0MHz</td>
<td>0.5V/\mu s</td>
<td>57°</td>
</tr>
<tr>
<td></td>
<td>0.8V</td>
<td>0.0V-0.4V</td>
<td>0.25V-0.5V</td>
<td>0.15V-0.65V</td>
<td>46dB-53dB</td>
<td>0.8MHz</td>
<td>0.4V/\mu s</td>
<td>54°</td>
</tr>
<tr>
<td></td>
<td>0.7V</td>
<td>0.0V-0.3V</td>
<td>0.2V-0.4V</td>
<td>0.1V-0.6V</td>
<td>33dB-36dB</td>
<td>1.3MHz</td>
<td>0.1V/\mu s</td>
<td>48°</td>
</tr>
</tbody>
</table>

The nominal value of bulk current is 10nA gives a 10% increase in differential pair quiescent current assuming a BJT $\beta$ of 100.
SUMMARY

- Integrated circuit power supplies are rapidly decreasing (today 2-3 Volts)
- Classical analog circuit design techniques begin to deteriorate at 1.5-2 Volts
- Approaches for lower voltage circuits:
  - Use natural NMOS transistors ($V_T \approx 0.1$V)
  - Drive the bulk terminal
  - Forward bias the bulk
  - Use depletion devices
- The dynamic range will be compressed if the noise is not also reduced
- Fortunately, the threshold reduction continues to allow the techniques of this section to be used in today’s technology

CHAPTER 7 - SUMMARY

This chapter has considered improved op amp performance in the areas of:
- Op amps that can drive low output load resistances and large output capacitances
- Op amps with improved bandwidth
- Op amps with differential output
- Op amps having low power dissipation
- Op amps having low noise
- Op amps that can work at low voltages

The objective of this chapter has been to show how to improve the performance of an op amp.
- We found that improvements are always possible
- The key is to balance the tradeoffs against the particular performance improvement
- This chapter is an excellent example of the degrees of freedom and choices that different circuit architectures can offer.

We also illustrated further the approaches to designing op amps
The next chapter begins the transition from analog to digital with the introduction of the comparator.