CHAPTER 5 – CMOS AMPLIFIERS
INTRODUCTION

Objective
Illustrate the analysis and design of amplifiers using CMOS technology.

Topics
- Introduction and Characterization
- Inverting Amplifiers
- Differential Amplifiers
- Cascode Amplifiers
- Current Amplifiers
- Output Amplifiers

Fig. 5.0-1

Types of Amplifiers

<table>
<thead>
<tr>
<th>Type of Amplifier</th>
<th>Gain = Output ( \frac{\text{Input}}{\text{Voltage}} )</th>
<th>Ideal Input Resistance</th>
<th>Ideal Output Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>( A_V = \frac{\text{Output Voltage}}{\text{Input Voltage}} )</td>
<td>Infinite</td>
<td>Zero</td>
</tr>
<tr>
<td>Current</td>
<td>( A_I = \frac{\text{Output Current}}{\text{Input Current}} )</td>
<td>Zero</td>
<td>Infinite</td>
</tr>
<tr>
<td>Transconductance</td>
<td>( G_m = \frac{\text{Output Current}}{\text{Input Voltage}} )</td>
<td>Infinite</td>
<td>Infinite</td>
</tr>
<tr>
<td>Transresistance</td>
<td>( R_m = \frac{\text{Output Voltage}}{\text{Input Current}} )</td>
<td>Zero</td>
<td>Zero</td>
</tr>
</tbody>
</table>

Most CMOS amplifiers fit naturally into the transconductance amplifier category as they have large input resistance and fairly large output resistance.

If the load resistance is high, the CMOS transconductance amplifier is essentially a voltage amplifier.
Characterization of an Amplifier

1.) Large signal static characterization:
   - Plot of output versus input (transfer curve)
   - Large signal gain
   - Output and input swing limits

2.) Small signal static characterization:
   - AC gain
   - AC input resistance
   - AC output resistance

3.) Small signal dynamic characterization:
   - Bandwidth
   - Noise
   - Power supply rejection

4.) Large signal dynamic characterization:
   - Slew rate
   - Nonlinearity

Components of a CMOS Voltage/Transconductance Amplifier

1.) A transconductance stage that converts the input voltage to current.
2.) A transresistance stage (load) that converts the current from the transconductance stage back to voltage.
Illustration of Voltage Amplifier Components

Transconductance stages are in the lower two shaded boxes
Transresistance stages (loads) are in the upper two shaded boxes (actually, the transconductance output also serves as a part of the load or transresistance stage)

Amplifier Notation

Simpler notation:
**Inverting and Noninverting Amplifiers**

The types of amplifiers are based on the various configurations of the actual transistors. If we assume that one terminal of the transistor is grounded, then three possibilities result:

1. **Common Source**
2. **Common Gate**
3. **Common Drain**

Note that there are two categories of amplifiers:

1. **Noninverting** - Those whose input and output are in phase (common gate and common drain)
2. **Inverting** - Those whose input and output are out of phase (common source)

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**SECTION 5.1 – INVERTING AMPLIFIERS**

**Types of Inverting Amplifiers**

The inverting amplifier or common source amplifier differs only by the type of load. Possible types of inverting amplifiers are shown below:

- **Class A Amplifiers**
- **Push-Pull Amplifier**

Class A amplifiers – The current in the load transistor (M2) flows during the entire period of a sinusoidal input.

Push-Pull (Class B and Class AB) amplifiers – The current flows in each transistor (M1 and M2) for less than the entire period of a sinusoidal input. Class B is 180° and Class AB is between 180° and 360°.
ACTIVE LOAD INVERTER

Voltage Transfer Characteristic of the Active Load Inverter

The boundary between active and saturation operation for M1 is

\[ V_{DS1} \approx V_{GS1} - V_{TH1} \rightarrow v_{OUT} \approx v_{IN} - 0.7V \]

Large-Signal Voltage Swing Limits of the Active Load Inverter

Maximum output voltage, \( v_{OUT}(\text{max}) \):

\[ v_{OUT}(\text{max}) = V_{DD} - |V_{TP}| \]

(ignores subthreshold current influence on the MOSFET)

Minimum output voltage, \( v_{OUT}(\text{min}) \):

Assume that M1 is nonsaturated and that \( V_{T1} = |V_{T2}| = V_T \).

\[ V_{DS1} \approx V_{GS1} - V_{TH} \rightarrow v_{OUT} \approx v_{IN} - 0.7V \]

The current through M1 is

\[ i_D = \frac{\beta_1}{2} \left( (V_{GS1} - V_T) V_{DS1} - \frac{V_{DS1}^2}{2} \right) = \beta_1 \left( (V_{DD} - V_T) (v_{OUT}) - \frac{(v_{OUT})^2}{2} \right) \]

\[ i_D = \frac{\beta_2}{2} (V_{SG2} - V_T)^2 = \frac{\beta_2}{2} (V_{DD} - v_{OUT} - V_T)^2 = \frac{\beta_2}{2} (v_{OUT} + V_T - V_{DD})^2 \]

Equating these currents gives the minimum \( v_{OUT} \) as,

\[ v_{OUT}(\text{min}) = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}} \]
**Small-Signal Midband Performance of the Active Load Inverter**

The development of the small-signal model for the active load inverter is shown below:

Sum the currents at the output node to get,

$$g_{m1}v_{in} + g_{ds1}v_{out} + g_{m2}v_{out} + g_{ds2}v_{out} = 0$$

Solving for the voltage gain, $v_{out}/v_{in}$, gives

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} = -\frac{g_{m1}}{g_{m2}} = -\frac{1}{g_{m2}}$$

The small-signal output resistance can also be found from the above by letting $v_{in} = 0$ to get,

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} = \frac{1}{g_{m2}}$$

---

**Frequency Response of the MOS Diode Load Inverter**

Incorporation of the parasitic capacitors into the small-signal model:

If we assume the input voltage has a small source resistance, then we can write the following:

$$sC_{M}(V_{out}-V_{in}) + g_{m}V_{in} + G_{out}V_{out} + sC_{out}V_{out} = 0$$

Hence,

$$V_{out}(G_{out} + sC_{M} + sC_{out}) = -(g_{m} - sC_{M})V_{in}$$

$$\frac{V_{out}}{V_{in}} = -\frac{(g_{m} - sC_{M})}{G_{out} + sC_{M} + sC_{out}} = -g_{m}R_{out} \left[\frac{1 - sC_{M}}{g_{m}} \right] \frac{1}{1 + sR_{out}(C_{M} + C_{out})} = -g_{m}R_{out} \left[\frac{1 - s}{\frac{1}{R_{out}C_{out} + C_{M}}} \right]$$

where $g_{m} = g_{m1}$, $p_{1} = \frac{-1}{R_{out}C_{out} + C_{M}}$, and $z_{1} = \frac{g_{m1}}{C_{M}}$

and

$$R_{out} = \left[ g_{ds1} + g_{ds2} + g_{m2} \right]^{-1} = \frac{1}{g_{m2}}, \quad C_{M} = C_{gd1}, \quad C_{out} = C_{bd1} + C_{bd2} + C_{gs2} + C_{L}$$
**Frequency Response of the MOS Diode Load Inverter - Continued**

If \(|p_1| < z_1\), then the -3dB frequency is approximately equal to \([R_{out}(C_{out}+C_M)]^{-1}\).

\[
0 \text{dB} \quad \left| p_1 \right| = \omega_{-3\text{dB}} \quad 20\log_{10}(g_mR_{out})
\]

**Observation:**

The poles in a MOSFET circuit can be found by summing the capacitance connected to a node and multiplying this capacitance times the equivalent resistance from this node to ground and inverting the product.

(See Appendix 5A for details on frequency response and Bode plots)

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**Example 5.1-1 - Performance of an Active Resistor-Load Inverter**

Calculate the output-voltage swing limits for \(V_{DD} = 5\) volts, the small-signal gain, the output resistance, and the -3 dB frequency of active load inverter if \((W_1/L_1) = 2 \mu m/1 \mu m\) and \(W_2/L_2 = 1 \mu m/1 \mu m\), \(C_{gd1} = 100\text{fF}\), \(C_{bd1} = 200\text{fF}\), \(C_{bd2} = 100\text{fF}\), \(C_{gs2} = 200\text{fF}\), \(C_L = 1\text{pF}\), and \(I_{D1} = I_{D2} = 100\mu A\), using the parameters in Table 3.1-2.

**Solution**

From the above results we find that:

- \(v_{OUT}(\text{max}) = 4.3\) volts
- \(v_{OUT}(\text{min}) = 0.418\) volts
- Small-signal voltage gain = -1.92V/V
- \(R_{out} = 9.17\text{k}\Omega\) including \(g_{ds1}\) and \(g_{ds2}\) and 10 k\(\Omega\) ignoring \(g_{ds1}\) and \(g_{ds2}\)
- \(z_1 = 2.10\times10^9\) rads/sec
- \(p_1 = -64.1\times10^6\) rads/sec.

Thus, the -3 dB frequency is 10.2 MHz.
CURRENT SOURCE INVERTER
Voltage Transfer Characteristic of the Current Source Inverter

Regions of operation for the transistors:
M1: \( v_{DS1} \geq v_{GS1} - V_{Th} \rightarrow v_{OUT} \geq v_{IN} - 0.7V \)
M2: \( v_{SD2} \geq v_{SG2} - |V_{Tp}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - V_{GG2} - |V_{Tp}| \rightarrow v_{OUT} \leq 3.2V \)

Large-Signal Voltage Swing Limits of the Current Source Load Inverter

Maximum output voltage, \( v_{OUT}(\text{max}) \):

\[
v_{OUT}(\text{max}) = V_{DD}
\]

Minimum output voltage, \( v_{OUT}(\text{min}) \):

Assume that M1 is nonsaturated. The minimum output voltage is,

\[
v_{OUT}(\text{min}) = \left[ V_{DD} - V_{T1} \right] \left[ 1 - \frac{\left( \frac{\beta_2}{\beta_1} \right) \left( V_{DD} - V_{GG} - |V_{T2}| \right)}{V_{DD} - V_{T1}} \right]
\]

This result assumes that \( v_{IN} \) is taken to \( V_{DD} \).
Small-Signal Midband Performance of the Current Source Load Inverter

Small-Signal Model:

Midband Performance:

\[
\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \left(\frac{2K'NW_1}{L \cdot I_D}\right)^{1/2} \left(\frac{1}{\lambda_1 + \lambda_2}\right) \times \frac{1}{\sqrt{I_D}} \quad \text{!!! and} \quad R_{out} = \frac{1}{g_{ds1} + g_{ds2}} \approx I_D(\lambda_1 + \lambda_2)
\]

Strong Inversion

log(I_{Bias})

\[= 1 \mu A\]

Frequency Response of the Current Source Load Inverter

Incorporation of the parasitic capacitors into the small-signal model (x is connected to \(V_{GG2}\)):

If we assume the input voltage has a small source resistance, then we can write the following:

\[
\frac{V_{out}(s)}{V_{in}(s)} = -g_mR_{out} \left[1 - \frac{s}{z_1}\right] \left[1 - \frac{s}{P_1}\right]
\]

where \(g_m = g_{m1}\), \(P_1 = R_{out}(C_{out} + C_M)\), and \(z_1 = \frac{g_m}{C_M}\)

and \(R_{out} = \frac{1}{g_{ds1} + g_{ds2}}\) and \(C_{out} = C_{gd2} + C_{bd1} + C_{bd2} + C_L\) \(C_M = C_{gd1}\)

Therefore, if \(|P_1| < |z_1|\), then the -3 dB frequency response can be expressed as

\[
\omega_{-3dB} = \frac{\omega_1}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}
\]
Example 5.1-2 - Performance of a Current-Sink Inverter

A current-sink inverter is shown in Fig. 5.1-7. Assume that $W_1 = 2 \ \mu m$, $L_1 = 1 \ \mu m$, $W_2 = 1 \ \mu m$, $L_2 = 1 \ \mu m$, $V_{DD} = 5$ volts, $V_{GG1} = 3$ volts, and the parameters of Table 3.1-2 describe $M_1$ and $M_2$. Use the capacitor values of Example 5.1-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance.

Solution

To attain the output signal-swing limitations, we treat Fig. 5.1-7 as a current source CMOS inverter with PMOS parameters for the NMOS and NMOS parameters for the PMOS and use NMOS equations. Using a prime notation to designate the results of the current source CMOS inverter that exchanges the PMOS and NMOS model parameters,

$$v_{OUT}(\text{max})' = 5V \quad \text{and} \quad v_{OUT}(\text{min})' = (5-0.7)
\frac{1}{1 - \sqrt{1 - \frac{110 \cdot 1}{50 \cdot 2}}} = 0.74V$$

In terms of the current sink CMOS inverter, these limits are subtracted from 5V to get

$$v_{OUT}(\text{max}) = 4.26V \quad \text{and} \quad v_{OUT}(\text{min}) = 0V.$$

To find the small signal performance, first calculate the dc current. The dc current, $I_D$, is

$$I_D = \frac{K_N W_1}{2L_1} (V_{GG1} - V_{TN})^2 = \frac{110 \cdot 1}{2 \cdot 1} (3-0.7)^2 = 291 \mu A$$

$$\frac{v_{out}}{v_{in}} = -9.2V/V, \quad R_{\text{out}} = 38.1 \ \text{k}\Omega, \quad \text{and} \quad f_{3\text{dB}} = 2.78 \ \text{MHz}.$$
Small-Signal Performance of the Push-Pull Amplifier

Small-signal analysis gives the following results:

\[
\frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} = -\sqrt{\left(\frac{2}{I_D}\right) \left[ \frac{K'_N(W_1/L_1) + K'_P(W_2/L_2)}{\lambda_1 + \lambda_2} \right]},
\]

\[
R_{out} = \frac{1}{g_{ds1} + g_{ds2}}
\]

\[
z = \frac{g_{m1} + g_{m2}}{C_M} = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}}
\]

and \( p_1 = \frac{-g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L} \)

If \( z_1 > |p_1| \), then

\[
\omega_{3\,dB} = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}
\]

Example 5.1-3 - Performance of a Push-Pull Inverter

The performance of a push-pull CMOS inverter is to be examined. Assume that \( W_1 = 1 \ \mu m, L_1 = 1 \ \mu m, W_2 = 2 \ \mu m, L_2 = 1 \ \mu m, V_{DD} = 5 \) volts, and use the parameters of Table 3.1-2 to model M1 and M2. Use the capacitor values of Example 5.1-1 \( (C_{gd1} = C_{gd2}) \). Calculate the output-swing limits and the small-signal performance assuming that \( I_{D1} = I_{D2} = 300 \mu A \).

**Solution**

The output swing is seen to be from 0V to 5V. In order to find the small signal performance, we will make the important assumption that both transistors are operating in the saturation region. Therefore:

\[
\frac{v_{out}}{v_{in}} = \frac{-257 \mu S - 245 \mu S}{12 \mu S + 15 \mu S} = -18.6 \text{V/V}
\]

\[
R_{out} = 37 \text{ k}\Omega
\]

\[
f_{-3\,dB} = 2.86 \text{ MHz}
\]

and

\[
z_1 = 399 \text{ MHz}
\]
**Noise Analysis of Inverting Amplifiers**

Noise model:

1. Assume a mean-square input-voltage-noise spectral density $e_n^2$ in series with the gate of each MOSFET.
   (This step assumes that the MOSFET is the common source configuration.)
2. Calculate the output-voltage-noise spectral density, $e_{out}^2$ (Assume all sources are additive).
3. Refer the output-voltage-noise spectral density back to the input to get equivalent input noise $e_{eq}^2$.
4. Substitute the type of noise source, 1/f or thermal.

**Noise Analysis of the Active Load Inverter**

1.) See model to the right.

2.) $e_{out}^2 = e_n^2 \left( \frac{g_{m1}}{g_{m2}} \right)^2 + e_n^2$

3.) $e_{eq}^2 = e_n^2 \left[ 1 + \frac{g_{m2}}{g_{m1}} \left( \frac{e_{n2}}{e_{n1}} \right)^2 \right]$

Up to now, the type of noise is not defined.

1/f Noise

Substituting $e_n^2 = \frac{K F}{2 f C_{ox} W L K} = \frac{B}{f W L}$ into the above gives,

$$e_{eq(1/f)}^2 = \left( \frac{B_1}{f W_1 L_1} \right)^{1/2} \left[ 1 + \left( \frac{K_2 B_2}{K_1 B_1} \right)^2 \right]^{1/2}$$

To minimize 1/f noise, 1.) Make $L_2 >> L_1$, 2.) increase the value of $W_1$ and 3.) choose M1 as a PMOS.

Thermal Noise

Substituting $e_n^2 = \frac{8kT}{3g_{m}}$ into the above gives,

$$e_{eq(th)} = \left[ \frac{8kT}{3 \left( 2 K_1 W_1 L_1 \right)^{1/2}} \left[ 1 + \left( \frac{W_2 L_1 K_2}{L_2 W_1 K_1} \right)^{1/2} \right]^{1/2} \right]$$

To minimize thermal noise, maximize the gain of the inverter.
**Noise Analysis of the Active Load Inverter - Continued**

When calculating the contribution of $e_{n2}^2$ to $e_{out}^2$, it was assumed that the gain was unity. To verify this assumption consider the following model:

![Fig. 5.1-11](image)

We can show that,

\[
\frac{e_{out}^2}{e_{n2}^2} = \left[ \frac{g_m r_{ds1} || r_{ds2}}{1 + g_m r_{ds1} || r_{ds2}} \right]^2 \approx 1
\]

**Noise Analysis of the Current Source Load Inverting Amplifier**

Model:

![Fig. 5.1-12](image)

The output-voltage-noise spectral density of this inverter can be written as,

\[
e_{out}^2 = (g_m r_{out})^2 e_{n1}^2 + (g_m r_{out})^2 e_{n2}^2
\]

or

\[
e_{eq}^2 = e_{n1}^2 + (g_m r_{out})^2 e_{n2}^2 = e_{n1}^2 \left[ 1 + \frac{(g_m r_{out})^2}{g_m} \right]^2
\]

This result is identical with the active load inverter. Thus the noise performance of the two circuits are equivalent although the small-signal voltage gain is significantly different.
Noise Analysis of the Push-Pull Amplifier

Model:

The equivalent input-voltage-noise spectral density of the push-pull inverter can be found as

\[ e_{eq} = \sqrt{\left(\frac{g_{m1}e_{n1}}{g_{m1} + g_{m2}}\right)^2 + \left(\frac{g_{m2}e_{n2}}{g_{m1} + g_{m2}}\right)^2} \]

If the two transconductances are balanced (\(g_{m1} = g_{m2}\)), then the noise contribution of each device is divided by two. The total noise contribution can only be reduced by reducing the noise contribution of each device. (Basically, both M1 and M2 act like the “load” transistor and “input” transistor, so there is no defined input transistor that can cause the noise of the load transistor to be insignificant.)

Summary of CMOS Inverting Amplifiers

<table>
<thead>
<tr>
<th>Inverter</th>
<th>AC Voltage Gain</th>
<th>AC Output Resistance</th>
<th>Bandwidth (CGB=0)</th>
<th>Equivalent, input-referred, mean-square noise voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>p-channel active load inverter</td>
<td>(-\frac{g_{m1}}{g_{m2}})</td>
<td>(\frac{1}{g_{m2}})</td>
<td>(\frac{g_{m2}}{g_{m1} + g_{m2}})</td>
<td>(e_{n1}^2 + e_{n2}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2)</td>
</tr>
<tr>
<td>Current source load inverter</td>
<td>(-\frac{g_{m1}}{g_{ds1}+g_{ds2}})</td>
<td>(\frac{1}{g_{ds1}+g_{ds2}})</td>
<td>(\frac{g_{ds1}+g_{ds2}}{g_{ds1}+g_{ds2}})</td>
<td>(e_{n1}^2 + e_{n2}^2\left(\frac{g_{m2}}{g_{m1}}\right)^2)</td>
</tr>
<tr>
<td>Push-Pull inverter</td>
<td>(-\frac{(g_{m1}+g_{m2})}{g_{ds1}+g_{ds2}})</td>
<td>(\frac{1}{g_{ds1}+g_{ds2}})</td>
<td>(\frac{g_{ds1}+g_{ds2}}{g_{ds1}+g_{ds2}})</td>
<td>(\frac{g_{ds1}+g_{ds2}}{g_{ds1}+g_{ds2}}\left(\frac{g_{m1}e_{n1}}{g_{m1} + g_{m2}}\right)^2 + \left(\frac{g_{m1}e_{n1}}{g_{m1} + g_{m2}}\right)^2)</td>
</tr>
</tbody>
</table>
SECTION 5.2 – DIFFERENTIAL AMPLIFIERS
CHARACTERIZATION OF A DIFFERENTIAL AMPLIFIER

What is a Differential Amplifier?
A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages. Differential and common mode voltages:

\[ v_1 \text{ and } v_2 \text{ are called single-ended voltages. They are voltages referenced to ac ground.} \]

The differential-mode input voltage, \( v_{ID} \), is the voltage difference between \( v_1 \) and \( v_2 \).

The common-mode input voltage, \( v_{IC} \), is the average value of \( v_1 \) and \( v_2 \).

\[
\begin{align*}
  v_{ID} &= v_1 - v_2 \\
  v_{IC} &= \frac{v_1 + v_2}{2}
\end{align*}
\]

\[
\begin{align*}
  \Rightarrow v_1 &= v_{IC} + 0.5v_{ID} \\
  v_2 &= v_{IC} - 0.5v_{ID}
\end{align*}
\]

\[
\begin{align*}
  v_{OUT} &= A_{VD}v_{ID} \pm A_{VC}v_{IC} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)
\end{align*}
\]

where

\[
\begin{align*}
  A_{VD} &= \text{differential-mode voltage gain} \\
  A_{VC} &= \text{common-mode voltage gain}
\end{align*}
\]

Differential Amplifier Definitions

- **Common mode rejection ratio (CMRR)**

\[
CMRR = \left| \frac{A_{VD}}{A_{VC}} \right|
\]

\[ CMRR \] is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

- **Input common-mode range (ICMR)**

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the \( ICMR \) is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

- **Output offset voltage (\( V_{OS(out)} \))**

The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

- **Input offset voltage (\( V_{OS(in)} = V_{OS} \))**

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

\[
V_{OS} = \frac{V_{OS(out)}}{A_{VD}}
\]
Transconductance Characteristic of the Differential Amplifier

Consider the following n-channel differential amplifier (sometimes called a source-coupled pair):

Where should bulk be connected? Consider a p-well, CMOS technology,

1.) Bulks connected to the sources: No modulation of $V_T$ but large common mode parasitic capacitance.
2.) Bulks connected to ground: Smaller common mode parasitic capacitors, but modulation of $V_T$.
If the technology is n-well CMOS, there is no choice. The bulks must be connected to ground.

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Transconductance Characteristic of the Differential Amplifier - Continued

Defining equations:

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2iD1}{\beta}\right)^{1/2} - \left(\frac{2iD2}{\beta}\right)^{1/2}$$

and

$$I_{SS} = iD1 + iD2$$

Solution:

$$iD1 = \frac{I_{SS}}{2} + \frac{I_{SS}}{2} \left(\frac{\beta v_{ID}}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}\right)^{1/2}$$

and

$$iD2 = \frac{I_{SS}}{2} - \frac{I_{SS}}{2} \left(\frac{\beta v_{ID}}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}\right)^{1/2}$$

which are valid for $v_{ID} < 2(I_{SS}/\beta)^{1/2}$.

Illustration of the result:

Differentiating $iD1$ (or $iD2$) with respect to $v_{ID}$ and setting $V_{ID} = 0$ gives

$$g_m = \frac{diD1}{dv_{ID}}(V_{ID} = 0) = (\beta I_{SS}/4)^{1/2} = \left(\frac{K_I}{4L_1}\right)^{1/2}$$

(half the $g_m$ of an inverting amplifier)
**Voltage Transfer Characteristic of the Differential Amplifier**

In order to obtain the voltage transfer characteristic, a load for the differential amplifier must be defined. We will select a current mirror load as illustrated below.

![Figure 5.2-5](image)

Note that output signal to ground is equivalent to the differential output signal due to the current mirror.

The short-circuit, transconductance is given as

\[
g_m = \frac{d i_{OUT}}{d v_{ID}} \quad (V_{ID} = 0) = (\beta I_{SS})^{1/2} = \left(\frac{K' I_{SS} W_1}{L_1}\right)^{1/2}
\]

**Voltage Transfer Function of the Differential Amplifier with a Current Mirror Load**

![Voltage Transfer Function](image)

Regions of operation of the transistors:

M2 is saturated when,

\[ v_{DS2} \geq v_{GS2} - V_{TN} \quad \rightarrow \quad v_{OUT} - V_{S1} \geq V_{IC} - 0.5v_{ID} - V_{S1} - V_{TN} \quad \rightarrow \quad v_{OUT} \approx V_{IC} - V_{TN} \]

where we have assumed that the region of transition for M2 is close to \( v_{ID} = 0 \) V.

M4 is saturated when,

\[ v_{SD4} \geq v_{SG4} - |V_{TP}| \quad \rightarrow \quad V_{DD} - V_{OUT} \geq V_{SG4} - |V_{TP}| \quad \rightarrow \quad v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}| \]

The regions of operations shown on the voltage transfer function assume \( I_{SS} = 100 \mu A \).

Note: \( V_{SG4} = \sqrt{\frac{2 \cdot 50}{20 \cdot 2}} + |V_{TP}| = 1 + |V_{TP}| \Rightarrow \) \( v_{OUT} \leq 5 - 1 - 0.7 + 0.7 = 4V \)
**Differential Amplifier Using p-channel Input MOSFETs**

![Differential Amplifier Diagram](image)

**Input Common Mode Range (ICMR)**

ICMR is found by setting $v_{ID} = 0$ and varying $v_{IC}$ until one of the transistors leaves the saturation.

**Highest Common Mode Voltage**
Path from G1 through M1 and M3 to $V_{DD}$:

$$V_{IC}(\text{max}) = V_{G1}(\text{max}) = V_{G2}(\text{max})$$

$$= V_{DD} - V_{SG3} - V_{DS1}(\text{sat}) + V_{GS1}$$

or

$$V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1}$$

Path from G2 through M2 and M4 to $V_{DD}$:

$$V_{IC}(\text{max})' = V_{DD} - V_{SD4}(\text{sat}) - V_{DS2}(\text{sat}) + V_{GS2}$$

$$= V_{DD} - V_{SD4}(\text{sat}) + V_{TN2}$$

$$\therefore V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN1}$$

**Lowest Common Mode Voltage** (Assume a $V_{SS}$ for generality)

$$V_{IC}(\text{min}) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}$$

where we have assumed that $V_{GS1} = V_{GS2}$ during changes in the input common mode voltage.
Example 5.2-1 - Small-Signal Analysis of the Differential-Mode of the Diff. Amp

A requirement for differential-mode operation is that the differential amplifier is balanced†.

\[
\frac{g_{m1}g_{m3}r_{p1}}{1 + g_{m3}r_{p1}} v_{gs1} - \frac{g_{m2}v_{gs2} - g_{m1}v_{gs1} - g_{m2}v_{gs2}}{g_{md}v_{id}}
\]

where \( g_{m1} = g_{m2} = g_{md} \), \( r_{p1} = r_{ds1} || r_{ds3} \) and \( i'_{out} \) designates the output current into a short circuit.

† It can be shown that the current mirror causes this requirement to be invalid because the drain loads are not matched. However, we will continue to use the assumption regardless.

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Small-Signal Analysis of the Differential-Mode of the Diff. Amplifier - Continued

Output Resistance:

\[
r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = r_{ds2} || r_{ds4}
\]

Differential Voltage Gain:

\[
A_v = \frac{v_{out}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}
\]

If we assume that all transistors are in saturation and replace the small signal parameters of \( g_m \) and \( r_d \) in terms of their large-signal model equivalents, we achieve

\[
A_v = \frac{v_{out}}{v_{id}} = \frac{K'_1 W_1/L_1}{(\lambda_2 + \lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2 + \lambda_4} \left( \frac{K'_1 W_1}{I_{SS}L_1} \right)^{1/2} \approx \frac{1}{\sqrt{I_{SS}}}
\]

Note that the small-signal gain is inversely proportional to the square root of the bias current!

Example:

If \( W_1/L_1 = 2\mu m/1\mu m \) and \( I_{SS} = 50\mu A \) (10\mu A), then

- \( A_v \) (n-channel) = 46.6V/V (104.23V/V)
- \( A_v \) (p-channel) = 31.4V/V (70.27V/V)

\[
r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{25\mu A \cdot 0.09V^{-1}} = 0.444M\Omega \ (2.22M\Omega)
\]

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**Common Mode Analysis for the Current Mirror Load Differential Amplifier**

The current mirror load differential amplifier is not a good example for common mode analysis because the current mirror rejects the common mode signal.

![Fig. 5.2-8A](image)

\[
\text{Total common mode Output due to } v_{ic} = \text{Common mode output due to M1-M3-M4 path} - \text{Common mode output due to M2 path}
\]

Therefore:
- The common mode output voltage should ideally be zero.
- Any voltage that exists at the output is due to mismatches in the gain between the two different paths.

**Small-Signal Analysis of the Common-Mode of the Differential Amplifier**

The common-mode gain of the differential amplifier with a current mirror load is ideally zero.

To illustrate the common-mode gain, we need a different type of load so we will consider the following:

![Fig. 330-05](image)

**Differential-Mode Analysis:**

\[
\frac{v_{o1}}{v_{id}} \approx -\frac{g_{m1}}{2g_{m3}} \quad \text{and} \quad \frac{v_{o2}}{v_{id}} \approx \frac{g_{m2}}{2g_{m4}}
\]

Note that these voltage gains are half of the active load inverter voltage gain.
Small-Signal Analysis of the Common-Mode of the Differential Amplifier – Cont’d

Common-Mode Analysis:

Assume that \( r_{ds1} \) is large and can be ignored (greatly simplifies the analysis).

\[
\begin{align*}
\dot{v}_{gs1} &= v_{g1} - v_{s1} = v_{ic} - 2g_m r_{ds5} v_{gs1} \\
\text{Solving for } v_{gs1} \text{ gives}
\end{align*}
\]

\[
v_{gs1} = \frac{v_{ic}}{1 + 2g_m r_{ds5}}
\]

The single-ended output voltage, \( v_{o1} \), as a function of \( v_{ic} \) can be written as

\[
\frac{v_{o1}}{v_{ic}} = -\frac{g_m [r_{ds3}] (1/g_m)}{1 + 2g_m r_{ds5}} = -\frac{g_{ds5}}{2g_m}
\]

Common-Mode Rejection Ratio (CMRR):

\[
CMRR = \left| \frac{v_{o1}}{v_{id}} \right| = \frac{g_m/2g_m}{g_{ds5}/2g_m} = g_m r_{ds5}
\]

How could you easily increase the CMRR of this differential amplifier?

Frequency Response of the Differential Amplifier

Back to the current mirror load differential amplifier:

\[
\begin{align*}
\text{If } C_3 &= 0, \text{ then we can write}
\end{align*}
\]

\[
V_{out}(s) = \frac{g_m}{g_{ds2} + g_{ds4}} \left( \frac{g_m}{g_{m3} + sC_1} \right) V_{gs1}(s) - V_{gs2}(s) \left( \frac{\omega_2}{s + \omega_2} \right)
\]

where \( \omega_2 \approx \frac{g_{ds2} + g_{ds4}}{C_2} \)

If we further assume that \( g_{m3}/C_1 >> (g_{ds2} + g_{ds4})/C_2 = \omega_2 \)

then the frequency response of the differential amplifier reduces to

\[
\frac{V_{out}(s)}{V_{id}(s)} = \frac{g_m}{g_{ds2} + g_{ds4}} \left( \frac{\omega_2}{s + \omega_2} \right)
\]

(A more detailed analysis will be made in Chapter 6)
AN INTUITIVE METHOD OF SMALL SIGNAL ANALYSIS

Simplification of Small Signal Analysis
Small signal analysis is used so often in analog circuit design that it becomes desirable to find faster ways of performing this important analysis.

Intuitive Analysis (or Schematic Analysis)
Technique:
1.) Identify the transistor(s) that convert the input voltage to current (these transistors are called transconductance transistors).
2.) Trace the currents to where they flow into an equivalent resistance to ground.
3.) Multiply this resistance by the current to get the voltage at this node to ground.
4.) Repeat this process until the output is reached.

Simple Example:
\[
\begin{align*}
\nu_1 &= -(g_{m1}\nu_{in})\, R_1 \quad \to \quad \nu_{out} = -(g_{m2}\nu_1)\, R_2 \\
\nu_{out} &= (g_{m1}R_1) (g_{m2}R_2) \nu_{in}
\end{align*}
\]

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Intuitive Analysis of the Current-Mirror Load Differential Amplifier

1.) \( i_1 = 0.5g_{m1}\nu_{id} \) and \( i_2 = -0.5g_{m2}\nu_{id} \)
2.) \( i_3 = i_1 = 0.5g_{m1}\nu_{id} \)
3.) \( i_4 = i_3 = 0.5g_{m1}\nu_{id} \)
4.) The resistance at the output node, \( r_{out} \), is \( r_{ds2}||r_{ds4} \) or \( \frac{1}{g_{ds2} + g_{ds4}} \)
5.) \( \nu_{out} = (0.5g_{m1}\nu_{id} + 0.5g_{m2}\nu_{id})r_{out} = \frac{g_{m1}\nu_{in}}{g_{ds2} + g_{ds4}} = \frac{g_{m2}\nu_{in}}{g_{ds2} + g_{ds4}} \to \nu_{out} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \nu_{in} \)
Some Concepts to Help Extend the Intuitive Method of Small-Signal Analysis

1.) Approximate the output resistance of any cascode circuit as
\[ R_{\text{out}} \approx (g_{m2}r_{ds2})r_{ds1} \]
where M1 is a transistor cascoded by M2.

2.) If there is a resistance, \( R \), in series with the source of the transconductance transistor, let the effective transconductance be
\[ g_{m(\text{eff})} = \frac{g_m}{1 + g_m R} \]

Proof:

\[ v_{gs2} = v_{g2} - v_{s2} = v_{in} - (g_{m2}r_{ds1})v_{gs2} \]
\[ v_{gs2} = \frac{v_{in}}{1 + g_{m2}r_{ds1}} \]

Thus, \( i_{\text{out}} = \frac{g_{m2}v_{in}}{1 + g_{m2}r_{ds1}} = g_{m(\text{eff})}v_{in} \)

FURTHER CONSIDERATIONS OF THE DIFFERENTIAL AMPLIFIER

Linearization of the Transconductance

Goal:

Method (degeneration):

\[ v_{DD} \]
\[ i_{out} \]
\[ M1 \]
\[ M2 \]
\[ M3 \]
\[ M4 \]
\[ M5 \]
\[ M6 \]
\[ V_{NBias1} \]
\[ V_{in} \]
\[ V_{SS} \]
\[ V_{SS} \]
\[ V_{SS} \]
\[ 060118-10 \]

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**Linearization with Active Devices**

![Circuit Diagram]

M6 is in deep triode region

M6 and M7 are in the triode region

Note that these transconductors on this slide and the last can all be adjusted by changing the value of $I_{SS}$.

**Slew Rate of the Differential Amplifier**

Slew Rate ($SR$) = Maximum output-voltage rate (either positive or negative)

It is caused by, $i_{OUT} = C_L \frac{dv_{OUT}}{dt}$. When $i_{OUT}$ is a constant, the rate is a constant.

Consider the following current-mirror load, differential amplifiers:

![Circuit Diagram]

Note that slew rate can only occur when the differential input signal is large enough to cause $I_{SS}$ ($I_{DD}$) to flow through only one of the differential input transistors.

$$SR = \frac{I_{SS}}{C_L} = \frac{I_{DD}}{C_L} \quad \Rightarrow \quad \text{If } C_L = 5\text{pF and } I_{SS} = 10\mu A, \text{ the slew rate is } SR = 2V/\mu s.$$

(For the BJT differential amplifier slewing occurs at ±100mV whereas for the MOSFET differential amplifier it can be ±2V or more.)
Noise Analysis of the Differential Amplifier

\[
i_{to}^2 = g_{m_1}^2 e_{n_1}^2 + g_{m_2}^2 e_{n_2}^2 + g_{m_3}^2 e_{n_3}^2 + g_{m_4}^2 e_{n_4}^2
\]

This output-noise current can be expressed in terms of an equivalent input noise voltage, \( e_{eq}^2 \), given as

\[
i_{to}^2 = g_{m_1}^2 e_{eq}^2
\]

Equating the above two expressions for the total output-noise current gives,

\[
e_{eq}^2 = e_{n_1}^2 + e_{n_2}^2 + \left( \frac{g_{m_3}}{g_{m_1}} \right)^2 \left( e_{n_3}^2 + e_{n_4}^2 \right)
\]

1/f Noise (\( e_{n_1}^2 = e_{n_2}^2 \) and \( e_{n_3}^2 = e_{n_4}^2 \)):

\[
e_{eq(1/f)} = \sqrt{\frac{2B_p}{fW_1L_1}} \sqrt{1 + \left( \frac{K'_N B_N}{K' p B_p} \right) \left( \frac{L_1}{L_3} \right)^2}
\]

Thermal Noise (\( e_{n_1}^2 = e_{n_2}^2 \) and \( e_{n_3}^2 = e_{n_4}^2 \)):

\[
e_{eq(th)} = \sqrt{\frac{16kT}{3L_3} \left[ \frac{W_3L_1K_3'}{L_3W_1K_1} \right]^{1/2}}
\]

Differential Amplifiers with Differential Output

Current-Source Load Differential Amplifier

Gives a truly balanced differential amplifier.

Also, the upper input common-mode range is extended.

However, a problem occurs if \( I_1 \neq I_3 \) or if \( I_2 \neq I_4 \).
A Differential-Output, Differential-Input Amplifier

Probably the best way to solve the current mismatch problem is through the use of common-mode feedback.

Consider the following solution to the previous problem.

![Diagram of a differential-output, differential-input amplifier](image)

**Operation:**
- Common mode output voltages are sensed at the gates of MC2A and MC2B and compared to $V_{CM}$.
- The current in MC3 provides the negative feedback to drive the common mode output voltage to the desired level.
- With large values of output voltage, this common mode feedback scheme has flaws.

---

Common-Mode Stabilization of the Diff.-Output, Diff.-Input Amplifier - Continued

The following circuit avoids the large differential output signal swing problems.

![Diagram of common-mode stabilized differential amplifier](image)

Note that $R_{CM1}$ and $R_{CM2}$ must not load the output of the differential amplifier.
DESIGNING DIFFERENTIAL AMPLIFIERS

Design of a CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

**Constraints**
- Power supply
- Technology
- Temperature

**Specifications**
- Small-signal gain
- Frequency response \((C_L)\)
- ICMR
- Slew rate \((C_L)\)
- Power dissipation

**Relationships**

\[
A_v = g_m R_{out}
\]

\[
\omega_{-3dB} = 1/R_{out} C_L
\]

\[
V_{IC}^{(max)} = V_{DD} - V_{SG3} + V_{TN1}
\]

\[
V_{IC}^{(min)} = V_{SS} + V_{DS5(sat)} + V_{GS1} = V_{SS} + V_{DS5(sat)} + V_{GS2}
\]

\[
SR = I_{SS}/C_L
\]

\[
P_{diss} = (V_{DD} + |V_{SS}|) \times \text{All dc currents flowing from } V_{DD} \text{ or to } V_{SS}
\]

Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued

Schematic-wise, the design procedure is illustrated as shown:

1. Pick \(I_{SS}\) to satisfy the slew rate knowing \(C_L\) or the power dissipation
2. Check to see if \(R_{out}\) will satisfy the frequency response, if not change \(I_{SS}\) or modify circuit
3. Design \(W_3/L_3\) \((W_4/L_4)\) to satisfy the upper ICMR
4. Design \(W_1/L_1\) \((W_2/L_2)\) to satisfy the gain
5. Design \(W_5/L_5\) to satisfy the lower ICMR
6. Iterate where necessary
Example 5.2-2 - Design of a MOS Differential Amp. with a Current Mirror Load

Design the currents and $W/L$ values of the current mirror load MOS differential amplifier to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5V$, $SR \geq 10V/\mu s$ ($C_L=5pF$), $f_{3dB} \geq 100kHz$ ($C_L=5pF$), a small signal gain of $100V/V$, $-1.5\leq ICMR\leq 2V$ and $P_{diss} \leq 1mW$. Use the parameters of $K'_N=110\mu A/V^2$, $K'_P=50\mu A/V^2$, $V_{TN}=0.7V$, $V_{TP}=-0.7V$, $\lambda_N=0.04V^{-1}$ and $\lambda_P=0.05V^{-1}$.

**Solution**

1.) To meet the slew rate, $I_{SS} \geq 50\mu A$. For maximum $P_{diss}$, $I_{SS} \leq 200\mu A$.

2.) $f_{3dB}$ of 100kHz implies that $R_{out} \leq 318k\Omega$. Therefore $R_{out} = \frac{2}{(\lambda_N+\lambda_P)I_{SS}} \leq 318k\Omega$

   $\therefore I_{SS} \geq 70\mu A$  Thus, pick $I_{SS} = 100\mu A$

3.) $V_{IC}(\text{max}) = V_{DD} - V_{SG3} + V_{TN} \rightarrow 2V = 2.5 - V_{SG3} + 0.7$

   
   $V_{SG3} = 1.2V = \sqrt{\frac{2\cdot50\mu A}{50\mu A/V^2(W_3/L_3)}} + 0.7$

   $\therefore \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(0.5)^2} = 8$

4.) $100=g_mR_{out}=\frac{g_m}{g_{ds2}+g_{ds4}} \Rightarrow \frac{W_5}{L_5} = \frac{2I_{SS}}{110\mu A/V^2(18.4)} + 0.7$

   $\frac{W_5}{L_5} = \frac{2I_{SS}}{110\mu A/V^2(18.4)} + 0.7 = 150.6$

   We probably should increase $W_1/L_1$ to reduce $V_{GS1}$. If we choose $W_1/L_1 = 40$, then $W_5/L_5 = 41$. (Larger than specified gain should be okay.)
SECTION 5.3 – CASCODE (COMMON GATE) AMPLIFIERS

VOLTAGE-DRIVEN COMMON GATE AMPLIFIER

Common Gate Amplifier

Circuit:

Large Signal Characteristics:

\[ V_{\text{OUT}}(\text{max}) \approx V_{\text{DD}} - V_{DS3}\text{(sat)} \]

\[ V_{\text{OUT}}(\text{min}) \approx V_{DS1}\text{(sat)} + V_{DS2}\text{(sat)} \]

Note \( V_{DS1}\text{(sat)} = V_{ON1} \)

Small Signal Performance of the Common Gate Amplifier

Small signal model:

\[ v_{\text{out}} = g_{m2}v_{s2} \left( \frac{r_{ds2}}{r_{ds2} + r_{ds3}} \right) r_{ds3} \frac{v_{in}}{} \]

\[ A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{g_{m2}r_{ds2}r_{ds3}}{r_{ds2} + r_{ds3}} \]

\[ R_{\text{in}} = R_{\text{in}}' || r_{ds1}, \quad R_{\text{in}}' \text{ is found as follows} \]

\[ v_{s2} = (i_1 - g_{m2}v_{s2})r_{ds2} + i_1r_{ds3} = i_1(r_{ds2} + r_{ds3}) - g_{m2}r_{ds2}v_{s2} \]

\[ R_{\text{in}}' = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}} \]

\[ R_{\text{out}} \approx r_{ds2} || r_{ds3} \]
**Frequency Response of the Common Gate Amplifier**

Circuit:

\[ r_{ds3} \leftarrow \frac{r_{ds3}}{sr_{ds3}C_{out}} + 1 \]

where \( C_{out} = C_{gd2} + C_{gd3} + C_{bd2} + C_{bd3} + C_L \)

\[ A_v(s) = \frac{V_{out}}{V_{in}} = \frac{gm2r_{ds2}r_{ds3}}{r_{ds2} + r_{ds3}} \left( \frac{1}{s} \right) \]

where \( p_1 = \frac{1}{r_{ds2}r_{ds3}C_{out}} \)

\[ \omega_{3dB} = |p_1| \]

**VOLTAGE-DRIVEN CASCODE AMPLIFIER**

**Cascode Amplifier**

Advantages of the cascode amplifier:

- Increases the output resistance and gain (if M3 is cascaded also)
- Eliminates the Miller effect when the input source resistance is large
Large-Signal Characteristics of the Cascode Amplifier

M1 sat. when \( V_{GG2} - V_{GS2} \geq V_{GS1} - V_T \rightarrow v_{IN} \leq 0.5(V_{GG2} + V_{TN}) \) where \( V_{GS1} = V_{GS2} \)

M2 sat. when \( V_{DS2} \geq V_{GS1} - V_{TN} \rightarrow v_{OUT} - V_{DS1} \geq V_{GG2} - V_{DS1} - V_{TN} \rightarrow v_{OUT} \geq V_{GG2} - V_{TN} \)

M3 is saturated when \( V_{DD} - v_{OUT} \geq V_{DD} - V_{GG3} - |V_Tp| \rightarrow v_{OUT} \leq V_{GG3} + |V_Tp| \)

Large-Signal Voltage Swing Limits of the Cascode Amplifier

Maximum output voltage, \( v_{OUT}(\text{max}) \):

\[
v_{OUT}(\text{max}) = V_{DD}
\]

Minimum output voltage, \( v_{OUT}(\text{min}) \):

Referencing all potentials to the negative power supply (ground in this case), we may express the current through each of the devices, M1 through M3, as

\[
i_D1 = \beta_1 \left( (V_{DD} - V_{T1})v_{DS1} - \frac{2}{2} v_{DS1} \right) \approx \beta_1 (V_{DD} - V_{T1})v_{DS1}
\]

\[
i_D2 = \beta_2 \left( (V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1}) - \frac{(v_{OUT} - v_{DS1})^2}{2} \right)
\]

\[
\approx \beta_2 (V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1})
\]

and

\[
i_D3 = \frac{\beta_3}{2} (V_{DD} - V_{GG3} - |V_{T3}|)^2
\]

where we have also assumed that both \( v_{DS1} \) and \( v_{OUT} \) are small, and \( v_{IN} = V_{DD} \).

Solving for \( v_{OUT} \) by realizing that \( i_D1 = i_D2 = i_D3 \) and \( \beta_1 = \beta_2 \) we get,

\[
v_{OUT}(\text{min}) = \frac{\beta_3}{2\beta_2} \left( V_{DD} - V_{GG3} - |V_{T3}| \right)^2 \left( \frac{1}{V_{GG2} - V_{T2}} + \frac{1}{V_{DD} - V_{T1}} \right)
\]
Example 5.3-1 - Calculation of the Min. Output Voltage for the Cascode Amplifier

(a.) Assume the values and parameters used for the cascode configuration plotted in the previous slide on the voltage transfer function and calculate the value of $v_{OUT}(\text{min})$.

(b.) Find the value of $v_{OUT}(\text{max})$ and $v_{OUT}(\text{min})$ where all transistors are in saturation.

Solution

(a.) Using the previous result gives,

$$v_{OUT}(\text{min}) = 0.50 \text{ volts}.$$  

We note that simulation gives a value of about 0.75 volts. If we include the influence of the channel modulation on M3 in the previous derivation, the calculated value is 0.62 volts which is closer. The difference is attributable to the assumption that both $v_{DS1}$ and $v_{OUT}$ are small.

(b.) The largest output voltage for which all transistors of the cascode amplifier are in saturation is given as

$$v_{OUT}(\text{max}) = V_{DD} - V_{SD3(\text{sat})}$$

and the corresponding minimum output voltage is

$$v_{OUT}(\text{min}) = V_{DS1(\text{sat})} + V_{DS2(\text{sat})}.$$  

For the cascode amplifier of Fig. 5.3-2, these limits are 3.0V and 2.7V. Consequently, the range over which all transistors are saturated is quite small for a 5V power supply.

Small-Signal Midband Performance of the Cascode Amplifier

Small-signal model:

Using nodal analysis, we can write,

$$[g_{ds1} + g_{ds2} + g_m]v_1 - g_{ds2}v_{out} = -g_m v_{in}$$

$$-[g_{ds2} + g_m]v_1 + (g_{ds2} + g_{ds3})v_{out} = 0$$

Solving for $v_{out}/v_{in}$ yields

$$\frac{v_{out}}{v_{in}} = \frac{-g_m (g_{ds2} + g_m)}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_m} \approx \frac{-g_m}{g_{ds}} = -\sqrt{\frac{2K'W}{LID\lambda_3}}$$

The small-signal output resistance is,

$$r_{out} = [r_{ds1} + r_{ds2} + gm2r_{ds1}r_{ds2}]r_{ds3} = r_{ds3}$$
Small-Signal Analysis of the Cascode Amplifier - Continued

It is of interest to examine the voltage gain of \( v_1/v_{in} \). From the previous nodal equations,

\[
\frac{v_1}{v_{in}} = \frac{-g_{m1}(g_{ds2}+g_{ds3})}{g_{ds1}g_{ds2}+g_{ds1}g_{ds3}+g_{ds2}g_{ds3}+g_{ds3}g_{m2}} \approx \frac{g_{ds2}+g_{ds3}}{g_{ds3}} \left( -\frac{g_{m1}}{g_{m2}} \right) = -2 \frac{g_{m1}}{g_{m2}} = -2 \sqrt{\frac{W_1L_2}{L_1W_2}}
\]

If the \( W/L \) ratios of M1 and M2 are equal and \( g_{ds2} = g_{ds3} \), then \( v_1/v_{in} \) is approximately -2.

Why is this gain -2 instead of -1?

Consider the small-signal model looking into the source of M2:
The voltage loop is written as,

\[
v_{s2} = (i_1 - g_{m2}v_{s2})r_{ds2} + i_1r_{ds3}
\]

\[
= i_1(r_{ds2} + r_{ds3}) - g_{m2}r_{ds2}v_{s2}
\]

Solving this equation for the ratio of \( v_{s2} \) to \( i_1 \) gives

\[
R_{s2} = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2}r_{ds2}}
\]

We see that \( R_{s2} \) equals \( 2/g_{m2} \) if \( r_{ds2} \approx r_{ds3} \). Thus, if \( g_{m1} \approx g_{m2} \), the voltage gain \( v_1/v_{in} \approx -2 \). Note that:

\( r_{ds3} \approx 0 \) that \( R_{s2} \approx 1/g_{m2} \) or \( r_{ds3}=r_{ds2} \) that \( R_{s2} \approx 2/g_{m2} \) or \( r_{ds3}=r_{ds2}g_{m2}r_{ds} \) that \( R_{s2} \approx r_{ds} \)!!!

Principle: The small-signal resistance looking into the source of a MOSFET depends on the resistance connected from the drain of the MOSFET to ac ground.

---

**Frequency Response of the Cascode Amplifier**

Small-signal model (\( R_S = 0 \)):

where

\[
C_1 = C_{gd1},
\]

\[
C_2 = C_{bd1} + C_{bd2} + C_{gs2}, \text{ and}
\]

\[
C_3 = C_{bd2} + C_{bd3} + C_{gd2} + C_{gd3} + C_L
\]

The nodal equations now become:

\[
(g_{m2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - g_{ds2}v_{out} = -(g_{m1} - sC_1)v_{in}
\]

and

\[
-(g_{ds2} + g_{m2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{out} = 0
\]

Solving for \( V_{out}(s)/V_{in}(s) \) gives,

\[
\frac{V_{out}(s)}{V_{in}(s)} = \left( \frac{1}{1 + as + bs^2} \right) \left( \frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})} \right)
\]

where

\[
a = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}
\]

and

\[
b = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}
\]
A Simplified Method of Finding an Algebraic Expression for the Two Poles

Assume that a general second-order polynomial can be written as:

\[ P(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \]

Now if \(|p_2| \gg |p_1|\), then \(P(s)\) can be simplified as

\[ P(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2} \]

Therefore we may write \(p_1\) and \(p_2\) in terms of \(a\) and \(b\) as

\[ p_1 = -\frac{a}{b} \quad \text{and} \quad p_2 = \frac{a}{b} \]

Applying this to the previous problem gives,

\[ p_1 = \frac{-[g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})]}{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})} \approx -\frac{g_{ds3}}{C_3} \]

The nondominant root \(p_2\) is given as

\[ p_2 = \frac{-[C_3(g_{ds1} + g_{ds2} + g_{m2})] + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{C_3(C_1 + C_2)} \approx \frac{-g_{m2}}{C_1 + C_2} \]

Assuming \(C_1, C_2,\) and \(C_3\) are the same order of magnitude, and \(g_{m2}\) is greater than \(g_{ds3}\), then \(|p_1|\) is smaller than \(|p_2|\). Therefore the approximation of \(|p_2| \gg |p_1|\) is valid.

Note that there is a right-half plane zero at \(z_1 = g_{m1}/C_1\).

NON-VOLTAGE DRIVEN CASCODE AMPLIFIER – THE MILLER EFFECT

Miller Effect

Consider the following inverting amplifier:

Solve for the input impedance:

\[ Z_{in}(s) = \frac{V_1}{I_1} \]

\[ I_1 = sC_M(V_1 - V_2) = sC_M(V_1 + A_vV_1) = sC_M(1 + A_v)V_1 \]

Therefore,

\[ Z_{in}(s) = \frac{V_1}{I_1} = \frac{V_1}{sC_M(1 + A_v)V_1} = \frac{1}{sC_M(1 + A_v)} = \frac{1}{sC_{eq}} \]

The Miller effect can take \(C_{gd} = 5fF\) and make it look like a 0.5pF capacitor in parallel with the input of the inverting amplifier \((A_v \approx -100)\).

If the source resistance is large, this creates a dominant pole at the input.
Simple Inverting Amplifier Driven with a High Source Resistance

Examine the frequency response of a current-source load inverter driven from a high resistance source:

Assuming the input is \( I_{in} \), the nodal equations are,

\[
G_1 + s(C_1 + C_2) \cdot V_1 - sC_2 \cdot V_{out} = I_{in} \quad \text{and} \quad (g_{m1} - sC_2) \cdot V_1 + [G_3 + s(C_2 + C_3)] \cdot V_{out} = 0
\]

where

\[
G_1 = G_s = 1/R_s, \quad G_3 = g_{ds1} + g_{ds2}, \quad C_1 = C_{gs1}, \quad C_2 = C_{gd1} \quad \text{and} \quad C_3 = C_{bd1} + C_{bd2} + C_{gd2}.
\]

Solving for \( V_{out}/V_{in} \) gives

\[
V_{out}/V_{in} = \frac{(sC_2 - g_{m1}) \cdot G_1}{G_3 + s[1 + (C_2 + C_3) + g_{m1} \cdot C_2]} + (C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3) s^2
\]

Assuming that the poles are split allows the use of the previous technique to get,

\[
p_1 = \frac{-1}{R_1 \cdot (C_1 + C_2) + R_3 \cdot (C_2 + C_3) + g_{m1} \cdot R_1 \cdot R_3 \cdot C_2} \quad \text{and} \quad p_2 = \frac{-g_{m1} \cdot C_2}{C_1 \cdot C_2 + C_1 \cdot C_3 + C_2 \cdot C_3}
\]

The Miller effect has caused the input pole, \( 1/R_1 \cdot C_1 \), to be decreased by a value of \( g_{m1} \cdot R_3 \).

How Does the Cascode Amplifier Solve the Miller Effect?

Cascode amplifier:

The Miller effect causes \( C_{gs1} \) to be increased by the value of \( 1 + (v_1/v_{in}) \) and appear in parallel with the gate-source of M1 causing a dominant pole to occur.

The cascode amplifier eliminates this problem by keeping the value of \( v_1/v_{in} \) small by making the value of \( R_{s2} \) approximately \( 2/g_{m2} \).
Comparison of the Inverting and Cascode Non-Voltage Driven Amplifiers

The dominant pole of the inverting amplifier with a large source resistance was found to be

\[ p_1(\text{inverter}) = \frac{-1}{R_1(C_1+C_2)+R_3(C_2+C_3)+g_{m1}R_1R_3C_2} \]

Now if a cascode amplifier is used, \( R_3 \) can be approximated as \( \frac{2}{g_m} \) of the cascoding transistor (assuming the drain sees an \( r_{ds} \) to ac ground).

\[ p_1(\text{cascode}) = \frac{-1}{R_1(C_1+C_2)+\left(\frac{2}{g_m}\right)(C_2+C_3)+g_{m1}R_1R_3C_2} \]

Thus we see that \( p_1(\text{cascode}) \gg p_1(\text{inverter}) \).

High Gain and High Output Resistance Cascode Amplifier

If the load of the cascode amplifier is a cascode current source, then both high output resistance and high voltage gain is achieved.

The output resistance is,

\[ r_{out} \approx [g_m r_{ds1} r_{ds2}] \left| \left| g_m r_{ds3} r_{ds4} \right| \right| \]

Knowing \( r_{out} \), the gain is simply

\[ A_v = -g_m r_{out} \approx -g_m \left\{ [g_m r_{ds1} r_{ds2}] \left| \left| g_m r_{ds3} r_{ds4} \right| \right| \right\} \approx \frac{2K_1(W/L)I_{D}}{\lambda_1 \lambda_2 + \sqrt{2K_3(W/L)^3}} \]
Example 5.3-2 - Comparison of the Cascode Amplifier Performance

Calculate the small-signal voltage gain, output resistance, the dominant pole, and the nondominant pole for the low-gain, cascode amplifier and the high-gain, cascode amplifier. Assume that $I_D = 200$ μA, that all $W/L$ ratios are $2 \mu m/1 \mu m$, and that the parameters of Table 3.1-2 are valid. The capacitors are assumed to be: $C_{gd} = 3.5$ fF, $C_{gs} = 30$ fF, $C_{bsn} = C_{bdn} = 24$ fF, $C_{bsp} = C_{bdp} = 12$ fF, and $C_L = 1$ pF.

Solution

The low-gain, cascode amplifier has the following small-signal performance:

- $A_v = -37.1 \text{V/V}$
- $R_{out} = 125k \Omega$
- $p_1 \approx -g_{ds3}/C_3 \to 1.22 \text{ MHz}$
- $p_2 \approx g_m2/(C_1+C_2) \to 605 \text{ MHz}$.

The high-gain, cascode amplifier has the following small-signal performance:

- $A_v = -414\text{V/V}$
- $R_{out} = 1.40 \text{ M\Omega}$
- $p_1 \approx 1/R_{out}C_3 \to 108 \text{ kHz}$
- $p_2 \approx g_m2/(C_1+C_2) \to 579 \text{ MHz}$

(Note at this frequency, the drain of M2 is shorted to ground by the load capacitance, $C_L$)

Designing Cascode Amplifiers

Pertinent design equations for the simple cascode amplifier.
**Example 5.3-3 - Design of a Cascode Amplifier**

The specs for a cascode amplifier are $A_v = -50\, \text{V/V}$, $v_{OUT}^{\text{max}} = 4\, \text{V}$, $v_{OUT}^{\text{min}} = 1.5\, \text{V}$, $V_{DD} = 5\, \text{V}$, and $P_{\text{diss}} = 1\, \text{mW}$. The slew rate with a 10pF load should be $10\, \text{V/\mu s}$ or greater.

**Solution**

The slew rate requires a current greater than $100\, \mu\text{A}$ while the power dissipation requires a current less than $200\, \mu\text{A}$. Compromise with $150\, \mu\text{A}$. Beginning with $M3$,

$$\frac{W_3}{L_3} = \frac{2I}{K_p[V_{DD} - v_{OUT}^{\text{max}}]^2} = \frac{2 \cdot 150}{50(1)^2} = 6$$

From this find $V_{GG3}$: $V_{GG3} = V_{DD} - |V_{TP}| - \sqrt{\frac{2I}{K_p(W_3/L_3)}} = 5 - 1 - \sqrt{\frac{2 \cdot 150}{50 \cdot 6}} = 3\, \text{V}$

Next,

$$\frac{W_1}{L_1} = \frac{(A_i \lambda)^2 I}{2K_N} = \frac{(50 \cdot 0.05)^2(150)}{2 \cdot 110} = 2.73$$

To design $W_2/L_2$, we will first calculate $V_{DS1}^{\text{sat}}$ and use the $v_{OUT}^{\text{min}}$ specification to define $V_{DS2}^{\text{sat}}$.

$$V_{DS1}^{\text{sat}} = \sqrt{\frac{2I}{K_N(W_1/L_1)}} = \sqrt{\frac{2 \cdot 150}{110 \cdot 4.26}} = 0.8\, \text{V}$$

Subtracting this value from $1.5\, \text{V}$ gives $V_{DS2}^{\text{sat}} = 0.7\, \text{V}$.

$$\therefore \frac{W_2}{L_2} = \frac{2I}{K_N V_{DS2}^{\text{sat}}^2} = \frac{2 \cdot 150}{110 \cdot 0.7^2} = 5.57$$

Finally,

$$V_{GG2} = V_{DS1}^{\text{sat}} + \sqrt{\frac{2I}{K_N(W_2/L_2)}} + V_{TN} = 0.8\, \text{V} + 0.7\, \text{V} + 0.7\, \text{V} = 2.2\, \text{V}$$

---

**SECTION 5.4 – CURRENT AMPLIFIERS**

**What is a Current Amplifier?**

- An amplifier that has a defined output-input current relationship
- Low input resistance
- High output resistance

**Application of current amplifiers:**

![Current Amplifier Diagram](Fig. 5.4-1)

$R_S \gg R_{in}$ and $R_{out} \gg R_L$

Advantages of current amplifiers:

- Currents are not restricted by the power supply voltages so that wider dynamic ranges are possible with lower power supply voltages.
- -3dB bandwidth of a current amplifier using negative feedback is independent of the closed loop gain.
**Frequency Response of a Current Amplifier with Current Feedback**

Consider the following current amplifier with resistive negative feedback applied.

Assuming that the small-signal resistance looking into the current amplifier is much less than $R_1$ or $R_2$,

\[ i_o = A_i (i_1 - i_2) = A_i \left( \frac{v_{in}}{R_1} - i_o \right) \]

Solving for $i_o$ gives

\[ i_o = \frac{A_i v_{in}}{1 + A_i} \]

\[ \rightarrow \quad v_{out} = R_2 i_o = \frac{R_2}{R_1} \frac{A_i}{1 + A_i} v_{in} \]

If $A_i(s) = \frac{A_o}{s \omega_A + 1}$, then

\[ \frac{v_{out}}{v_{in}} = \frac{R_2}{R_1} \left( \frac{1}{1 + A_i(s)} \right) = \frac{R_2}{R_1} \left( \frac{s}{s \omega_A + (1 + A_o)} \right) = \frac{R_2 A_o}{R_1 (1 + A_o)} \left( \frac{1}{s \omega_A (1 + A_o) + 1} \right) \]

\[ \therefore \quad \omega_{3dB} = \omega_A (1 + A_o) \]

**Bandwidth Advantage of a Current Feedback Amplifier**

The unity-gain bandwidth is,

\[ GB = |A_i(0)| \omega_{3dB} = \frac{R_2 A_o}{R_1 (1 + A_o)} \cdot \omega_A (1 + A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i \]

where $GB_i$ is the unity-gain bandwidth of the current amplifier.

*Note that if $GB_i$ is constant, then increasing $R_2/R_1$ (the voltage gain) increases $GB$.*

Illustration:

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the $GB$ of the voltage amplifier realizing the voltage buffer is greater than the $GB$ achieved from the above method.
Chapter 5 – Section 4 (7/5/06)

Current Amplifier using the Simple Current Mirror

\[ R_m = \frac{1}{g_{m1}} \quad R_{out} = \frac{1}{\lambda_1 I_o} \quad \text{and} \quad A_i = \frac{W_2/L_2}{W_1/L_1}. \]

Frequency response:

\[ p_1 = \frac{-g_{m1} + g_{ds1}}{C_{1} + C_{2}} = \frac{-g_{m1} + g_{ds1}}{C_{bs1} + C_{gs1} + C_{gs2} + C_{gd2}} \approx \frac{-g_{m1}}{C_{bs1} + C_{gs1} + C_{gs2} + C_{gd2}} \]

Note that the bandwidth can be almost doubled by including the resistor, \( R \). (\( R \) removes \( C_{gs1} \) from \( p_1 \))

Example 5.4-1 - Performance of a Simple Current Mirror as a Current Amplifier

Find the small-signal current gain, \( A_i \), the input resistance, \( R_{in} \), the output resistance, \( R_{out} \), and the -3dB frequency in Hertz for the current amplifier of Fig. 5.4-3(a) if \( I_1 = I_2 = 100 \mu A \) and \( W_2/L_2 = 10W_1/L_1 = 10\mu m/1\mu m \). Assume that \( C_{bd1} = 10fF \), \( C_{gs1} = C_{gs2} = 100fF \), and \( C_{gs2} = 50fF \).

**Solution**

Ignoring channel modulation and mismatch effects, the small-signal current gain,

\[ A_i = \frac{W_2/L_2}{W_1/L_1} = 10A/A. \]

The small-signal input resistance, \( R_{in} \), is approximately \( 1/g_{m1} \) and is

\[ R_{in} = \frac{1}{\sqrt{2K_A(1/1)10\mu A}} = \frac{1}{46.9\mu S} = 21.3k\Omega \]

The small-signal output resistance is equal to

\[ R_{out} = \frac{1}{\lambda_2 I_2} = 250k\Omega. \]

The -3dB frequency is

\[ \omega_{-3dB} = \frac{46.9\mu S}{260fF} = 180.4 \times 10^6 \text{ radians/sec.} \quad \rightarrow \quad f_{-3dB} = 28.7 \text{ MHz} \]
Wide-Swing, Cascode Current Mirror Implementation of a Current Amplifier

Example 5.4 -2 - Current Amplifier Implemented by the Wide-Swing, Cascode Current Mirror

Assume that $I_{IN}$ and $I_{OUT}$ of the wide-swing cascode current mirror are 100$\mu$A. Find the value of $R_{in}$, $R_{out}$, and $A_{i}$ if the W/L ratios of all transistors are 182$\mu$m/1$\mu$m.

Solution

The input resistance requires $g_{m1}$ which is $\sqrt{2\cdot110\cdot182\cdot100} = 2mS$

$\therefore R_{in} = 500\Omega$

From our knowledge of the cascode configuration, the small signal output resistance should be

$R_{out} \approx g_{m4}r_{ds2}g_{m4}r_{ds4} = (2001\mu S)(250k\Omega)(250k\Omega) = 125M\Omega$

Because $V_{DS1} = V_{DS2}$, the small-signal current gain is

$A_{i} = \frac{W_{2}/L_{2}}{W_{1}/L_{1}} = 1$

Simulation results using the level 1 model for this example give

$R_{in} = 497\Omega$, $R_{out} = 164.7M\Omega$ and $A_{i} = 1.000 A/A$.

The value of $V_{ON}$ for all transistors is

$V_{ON} = \sqrt{\frac{2\cdot100\mu A}{110\mu A/\sqrt{2\cdot182}}} = 0.1V$
Low-Input Resistance Current Amplifier

To decrease $R_{in}$ below $1/g_m$ requires the use of negative, shunt feedback. Consider the following example.

Feedback concept:

Input resistance without feedback $\approx r_{ds1}$.

Loop gain $\approx \left( \frac{g_m1}{g_{ds1}} \right) \left( \frac{g_m3}{g_{ds3}} \right)$ assuming that the resistances of $I_1$ and $I_3$ are very large.

$$R_{in}(\text{no fb.}) = \frac{r_{ds1}}{1 + \text{Loop gain}} = \frac{r_{ds1}}{g_m1r_{ds1}g_m3r_{ds3}} = \frac{1}{g_m1g_m3r_{ds3}}$$

Small signal analysis:

$$i_{in} = g_m1v_{gs1} - g_{ds1}v_{gs3}$$
and $v_{gs3} = -v_{in}$, $v_{gs1} = v_{in} - (g_m3v_{gs3}r_{ds3}) = v_{in}(1 + g_m3r_{ds3})$

$$\therefore i_{in} = g_m1(1 + g_m3r_{ds3})v_{in} + g_{ds1}v_{in} = g_m1g_m3r_{ds3}v_{in} \Rightarrow R_{in} \approx \frac{1}{g_m1g_m3r_{ds3}}$$

Differential-Input, Current Amplifiers

Definitions for the differential-mode, $i_{ID}$, and common-mode, $i_{IC}$, input currents of the differential-input current amplifier.

$$i_o = A_{ID}i_{ID} \pm A_{IC}i_{IC} = A_{ID}(i_1 - i_2) \pm A_{IC}\left(\frac{i_1 + i_2}{2}\right)$$

Implementations:
**Summary**

- Current amplifiers have a low input resistance, high output resistance, and a defined output-input current relationship.
- Input resistances less than \(1/g_m\) require feedback.
  
  However, all feedback loops have internal poles that cause the benefits of negative feedback to vanish at high frequencies.
  
  In addition, these feedback loops can have a slow time constant from a pole-zero pair.
- Voltage amplifiers using a current amplifier have high values of gain-bandwidth.
- Current amplifiers are useful at low power supplies and for switched current applications.

---

**SECTION 5.5 - OUTPUT AMPLIFIERS**

**INTRODUCTION**

**General Considerations of Output Amplifiers**

Requirements:

1. Provide sufficient output power in the form of voltage or current.
2. Avoid signal distortion.
3. Be efficient.
4. Provide protection from abnormal conditions (short circuit, over temperature, etc.).

Types of Output Amplifiers:

1. Class A amplifiers
2. Source followers
3. Push-pull amplifiers
4. Substrate BJT amplifiers
5. Amplifiers using negative shunt feedback
CLASS A AMPLIFIERS

**Current source load inverter**

A Class A circuit has current flow in the MOSFETs during the entire period of a sinusoidal signal. Characteristics of Class A amplifiers:
- Unsymmetrical sinking and sourcing
- Linear
- Poor efficiency

![Diagram of Class A Amplifier](image)

Efficiency \( \eta = \frac{P_{RL}}{P_{Supply}} = \frac{v_{OUT}^{\text{peak}}}{2} \frac{2R_L}{(V_{DD}-V_{SS})} = \frac{v_{OUT}^{\text{peak}}}{2} \frac{2R_L}{2R_L} = \left(\frac{v_{OUT}^{\text{peak}}}{V_{DD}-V_{SS}}\right)^2 \)

Maximum efficiency occurs when \( v_{OUT}^{\text{peak}} = V_{DD} = \left|V_{SS}\right| \) which gives 25%.

---

**Optimum Value of Load Resistor**

Depending on the value of \( R_L \), the signal swing can be symmetrical or asymmetrical. (This ignores the limitations of the transistor.)

![Diagram of Optimum Load Resistor](image)
**Specifying the Performance of a Class A Amplifier**

Output resistance:

\[ r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{(\lambda_1 + \lambda_2)I_D} \]

Current:

- Maximum sinking current is,
  \[ I_{OUT}^- = \frac{K'_1 W_1}{2 L_1} (V_{DD} - V_{SS} - V_T1)^2 - I_Q \]
- Maximum sourcing current is,
  \[ I_{OUT}^+ = \frac{K'_2 W_2}{2 L_2} (V_{DD} - V_{GG2} - |V_T2|)^2 \leq I_Q \]

Requirements:

- Want \( r_{out} \ll R_L \)
- \( |I_{OUT}| > C_L \cdot SR \)
- \( |I_{OUT}| > \frac{v_{OUT}(\text{peak})}{R_L} \)

The maximum current is determined by both the current required to provide the necessary slew rate \( (C_L) \) and to provide a voltage across the load resistor \( (R_L) \).

---

**Small-Signal Performance of the Class A Amplifier**

Although we have considered the small-signal performance of the Class A amplifier as the current source load inverter, let us include the influence of the load.

The modified small-signal model:

\[ \text{Fig. 5.5-2} \]

The small-signal voltage gain is:

\[ \frac{v_{out}}{v_{in}} = \frac{-g_m}{g_{ds1} + g_{ds2} + G_L} \]

The small-signal frequency response includes:

A zero at

\[ z = \frac{g_m}{C_{gd1}} \]

and a pole at

\[ p = \frac{-(g_{ds1} + g_{ds2} + G_L)}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L} \]
**Example 5.5-1 - Design of a Simple Class-A Output Stage**

Use Table 3.1-2 to design the \( W/L \) ratios of M1 and M2 so that a voltage swing of \( \pm 2 \text{V} \) and a slew rate of \( \pm 1 \text{V/\mu s} \) is achieved if \( R_L = 20 \text{k}\Omega \) and \( C_L = 1000 \text{pF} \). Assume \( V_{DD} = |V_{SS}| = 3 \text{V} \) and \( V_{GG2} = 0 \text{V} \). Let \( L = 2 \mu m \) and assume that \( C_{gd1} = 100\text{fF} \).

**Solution**

Let us first consider the effects of \( R_L \) and \( C_L \).

\[
i_{\text{OUT}}(\text{peak}) = \pm 2\text{V}/20\text{k}\Omega = \pm 100\mu\text{A}
\]

Since the slew rate current is so much larger than the current needed to meet the voltage specification across \( R_L \), we can safely assume that all of the current supplied by the inverter is available to charge \( C_L \).

Using a value of \( \pm 1 \text{mA} \),

\[
\frac{W_1}{L_1} = \frac{2(I_{\text{OUT}}+I_Q)}{K_N'(V_{DD}+|V_{SS}|-V_{TN})^2} = \frac{4000}{110 \cdot (5.3)^2} \approx \frac{3\mu m}{2\mu m}
\]

and

\[
\frac{W_2}{L_2} = \frac{2I_{\text{OUT}}^+}{K_P'(V_{DD}-V_{GG2}-|V_{TP}|)^2} = \frac{2000}{50 \cdot (2.3)^2} \approx \frac{15\mu m}{2\mu m}
\]

The small-signal performance is \( A_v = -8.21 \text{V/V} \) (includes \( R_L = 20\text{k}\Omega \)) and \( r_{\text{out}} = 50\text{k}\Omega \)

The roots are, zero = \( g_m1/C_{gd1} \Rightarrow .59\text{GHz} \) and pole = 1/[\( (R_L\|r_{\text{out}})C_L \)] \( \Rightarrow -11.14\text{kHz} \)

---

**Broadband Harmonic Distortion**

The linearity of an amplifier can be characterized by its influence on a pure sinusoidal input signal. Assume the input is,

\[ V_{\text{in}}(\omega) = V_p \sin(\omega t) \]

The output of an amplifier with distortion will be

\[ V_{\text{out}}(\omega) = a_1V_p \sin(\omega t) + a_2V_p \sin(2\omega t) + \cdots + a_nV_p \sin(n\omega t) \]

**Harmonic distortion (HD)** for the \( i \)th harmonic can be defined as the ratio of the magnitude of the \( i \)th harmonic to the magnitude of the fundamental. For example, second-harmonic distortion would be given as

\[ HD_2 = \frac{a_2}{a_1} \]

**Total harmonic distortion (THD)** is defined as the square root of the ratio of the sum of all of the second and higher harmonics to the magnitude of the first or fundamental

Thus, \( THD \) can be expressed as

\[ THD = \left[ \frac{\sum_{i=2}^{\infty} a_i^2}{a_1^2} \right]^{1/2} \]

The distortion of the class A amplifier is good for small signals and becomes poor at maximum output swings because of the nonlinearity of the voltage transfer curve for large-signal swing.
**Class-A Source Follower**

N-Channel Source Follower with current sink bias:

- **Voltage transfer curve:**
  - Maximum output voltage swings:
    - \( v_{OUT}(\text{min}) \approx V_{SS} - V_{ON2} \) (if \( R_L \) is large)
    - \( v_{OUT}(\text{max}) = V_{DD} - V_{ON1} \) (if \( V_{IN} > V_{DD} \))

\[
\begin{align*}
\text{Maximum output voltage swings:} \\
v_{OUT}(\text{min}) &= V_{SS} - V_{ON2} \quad \text{(if } R_L \text{ is large)} \\
v_{OUT}(\text{max}) &= V_{DD} - V_{ON1} \quad \text{(if } V_{IN} > V_{DD} \text{)}
\end{align*}
\]

Output Voltage Swing of the Follower

The previous results do not include the bulk effect on \( V_{T1} \) of \( V_{GS1} \).

Therefore,

\[
V_{T1} = V_{T01} + \gamma \sqrt{2|\phi_F|} - v_{BS} - \sqrt{2|\phi_F|} \approx V_{T01} + \gamma \sqrt{V_{SB}} = V_{T01} + \gamma \sqrt{v_{OUT}(\text{max})} - V_{SS}
\]

\[
\therefore \quad v_{OUT}(\text{max}) - V_{SS} \approx V_{DD} - V_{SS} - V_{ON1} - V_{T1} = V_{DD} - V_{SS} - V_{ON1} - V_{T01} - \gamma \sqrt{v_{OUT}(\text{max})} - V_{SS}
\]

Define \( v_{OUT}(\text{max}) - V_{SS} = v_{OUT}'(\text{max}) \)

which gives the quadratic,

\[
v_{OUT}'(\text{max}) + \gamma \sqrt{v_{OUT}'(\text{max})} - (V_{DD} - V_{SS} - V_{ON1} - V_{T01}) = 0
\]

Solving the quadratic gives,

\[
v_{OUT}'(\text{max}) = \frac{\gamma_1^2}{4} - \frac{\gamma_1}{2} \sqrt{\gamma_1^2 + 4(V_{DD} - V_{SS} - V_{ON1} - V_{T01})} + \frac{\gamma_1^2 + 4(V_{DD} - V_{SS} - V_{ON1} - V_{T01})}{4}
\]

If \( V_{DD} = 2.5 \text{V}, \gamma_N = 0.4 \text{V}^{1/2}, V_{TN1} = 0.7 \text{V}, \) and \( V_{ON1} = 0.2 \text{V}, \) then \( v_{OUT}'(\text{max}) = 3.661 \text{V} \)

\[
v_{OUT}(\text{max}) = 3.661 - 2.5 = 0.8661 \text{V}
\]
Maximum Sourcing and Sinking Currents for the Source Follower

Maximum Sourcing Current (into a short circuit):
We assume that the transistors are in saturation and \( V_{DD} = -V_{SS} = 2.5\text{V} \), thus
\[
I_{OUT}(\text{sourcing}) = \frac{K'W_1}{2L_1} [V_{DD} - v_{OUT} - V_{T1}]^2 - I_Q
\]
where \( v_{IN} \) is assumed to be equal to \( V_{DD} \).
If \( W_1/L_1 = 10 \) and if \( v_{OUT} = 0\text{V} \), then
\( V_{T1} = 1.08\text{V} \Rightarrow I_{OUT} \) equal to 1.11 mA.
However, as \( v_{OUT} \) increases above 0V, the current rapidly decreases.

Maximum Sinking Current:
For the current sink load, the sinking current is whatever the sink is biased to provide.
\( I_{OUT}(\text{sinking}) = I_Q \)

Efficiency of the Source Follower

Assume that the source follower input can swing to power supply.
Plotting
\[
i_D = \frac{\beta}{2} (v_{IN} - v_{OUT} - V_T)^2
\]
and
\[
i_D = I_Q - \frac{v_{OUT}}{R_L}
\]
Efficiency =
\[
\frac{P_{RL}}{P_{Supply}} = \frac{\left(\frac{v_{OUT(peak)}}{V_{DD} - V_{SS}}\right)^2}{\left(\frac{V_{DD} - V_{SS}}{2R_L}\right)^2} = \left(\frac{v_{OUT(peak)}}{V_{DD} - V_{SS}}\right)^2
\]
Maximum efficiency occurs when \( v_{OUT(peak)} = V_{DD} = |V_{SS}| \) which gives 25%.

Comments:
• Maximum efficiency occurs for the minimum value of \( R_L \) which gives max. swing.
• Other values of \( R_L \) result in less efficiency (and smaller signal swings before clipping)
• We have ignored the fact that the dynamic \( Q \) point cannot travel along the full length of the load line because of minimum and maximum voltage limits.
Small Signal Performance of the Source Follower

Small-signal model:

\[
\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + G_L} + \frac{g_{m1}}{T + g_{m1}R_L}
\]

If \(V_{DD} = -V_{SS} = 2.5\,\text{V}\), \(V_{out} = 0\,\text{V}\), \(W_1/L_1 = 10\,\mu\text{m}/1\,\mu\text{m}\), \(W_2/L_2 = 1\,\mu\text{m}/1\,\mu\text{m}\), and \(I_D = 500\,\mu\text{A}\), then

For the current sink load follower \((R_L = \infty)\):

\[
\frac{V_{out}}{V_{in}} = 0.869\,\text{V/V}, \text{ if the bulk effect were ignored, then } \frac{V_{out}}{V_{in}} = 0.963\,\text{V/V}
\]

For a finite load, \(R_L = 1000\,\Omega\):

\[
\frac{V_{out}}{V_{in}} = 0.512\,\text{V/V}
\]

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Small Signal Performance of the Source Follower - Continued

The output resistance is:

\[
R_{out} = \frac{1}{g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2}}
\]

For the current sink load follower:

\[R_{out} = 830\,\Omega\]

The frequency response of the source follower:

\[
\frac{V_{out}(s)}{V_{in}(s)} = \frac{(g_{m1} + sC_1)}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + G_L + s(C_1 + C_2)}
\]

where

\[C_1 = \text{capacitances connected between the input and output} = C_{GS1}\]
\[C_2 = C_{bs1} + C_{bd2} + C_{gd2}(\text{or } C_{gs2}) + C_L\]

\[z = \frac{g_{m1}}{C_1} \quad \text{and} \quad p = -\frac{g_{m1} + G_L}{C_1 + C_2}\]

The presence of a LHP zero leads to the possibility that in most cases the pole and zero will provide some degree of cancellation leading to a broadband response.
**PUSH-PULL AMPLIFIERS**

**Push-Pull Source Follower**
Can both sink and source current and provide a slightly lower output resistance.

Efficiency:
Depends on how the transistors are biased.
- **Class B** - one transistor has current flow for only 180° of the sinusoid (half period)

\[
\text{Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{v_{OUT}^{(\text{peak})^2}}{2RL} = \frac{\frac{1}{2}v_{OUT}^{(\text{peak})}}{(V_{DD} - V_{SS}) \frac{\pi}{2RL}}
\]

Maximum efficiency occurs when \( v_{OUT}^{(\text{peak})} = V_{DD} \) and is 78.5%
- **Class AB** - each transistor has current flow for more than 180° of the sinusoid. Maximum efficiency is between 25% and 78.5%

---

**Illustration of Class B and Class AB Push-Pull, Source Follower**
Output current and voltage characteristics of the push-pull, source follower (\( R_L = 1k\Omega \)):

Comments:
- Note that \( v_{OUT} \) cannot reach the extreme values of \( V_{DD} \) and \( V_{SS} \)
- \( I_{OUT}^{(\text{max})} \) and \( I_{OUT}^{(\text{max})} \) is always less than \( V_{DD}/R_L \) or \( V_{SS}/R_L \)
- For \( v_{OUT} = 0V \), there is quiescent current flowing in M1 and M2 for Class AB
- Note that there is significant distortion at \( v_{IN} = 0V \) for the Class B push-pull follower
Small-Signal Performance of the Push-Pull Follower

Model:

\[ v_{in} \frac{v_{out}}{g_m} = \frac{g_m \cdot v_{in} + r_{ds}}{r_{ds} + r_{ds} + \frac{1}{C_1}} \]

Fig. 060-03

\[ \frac{v_{out}}{v_{in}} = \frac{g_m + g_m}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_m + g_{mbs2} + G_L} \]

\[ R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_m + g_{mbs2}} \quad \text{(does not include } R_L) \]

If \( V_{DD} = -V_{SS} = 2.5V, V_{out} = 0V, I_{D1} = I_{D2} = 500\mu A, \) and \( W/L = 20\mu m/2\mu m, A_v = 0.787 \) (\( R_L = \infty \)) and \( R_{out} = 448\Omega \).

A zero and pole are located at

\[ z = \left( -\frac{g_m}{C_1} \right) \quad p = \left( -\frac{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_m + g_{mbs2} + G_L}{C_1 + C_2} \right). \]

These roots will be high-frequency because the associated resistances are small.

Push-Pull, Common Source Amplifiers

Similar to the class A but can operate as class B providing higher efficiency.

Comments:

- The batteries \( V_{TR1} \) and \( V_{TR2} \) are necessary to control the bias current in M1 and M2.
- The efficiency is the same as the push-pull, source follower.
Practical Implementation of the Push-Pull, Common Source Amplifier – Method 1

![Fig. 060-05](image)

$V_{GG3}$ and $V_{GG4}$ can be used to bias this amplifier in class AB or class B operation. Note, that the bias current in M6 and M8 is not dependent upon $V_{DD}$ or $V_{SS}$ (assuming $V_{GG3}$ and $V_{GG4}$ are not dependent on $V_{DD}$ and $V_{SS}$).

Practical Implementation of the Push-Pull, Common Source Amplifier – Method 2

![Fig. 060-055](image)

In steady-state, the current through M5 and M6 is $2I_b$. If $W_4/L_4 = W_9/L_9$ and $W_3/L_3 = W_8/L_8$, then the currents in M1 and M2 can be determined by the following relationship:

$$I_1 = I_2 = I_b \left( \frac{W_1/L_1}{W_7/L_7} \right) = I_b \left( \frac{W_2/L_2}{W_{10}/L_{10}} \right)$$

If $v_{in^+}$ goes low, M5 pulls the gates of M1 and M2 high. M4 shuts off causing all of the current flowing through M5 ($2I_b$) to flow through M3 shutting off M1. The gate of M2 is high allowing the buffer to strongly sink current. If $v_{in^-}$ goes high, M6 pulls the gates of M1 and M2 low. As before, this shuts off M2 and turns on M1 allowing strong sourcing.
Additional Methods of Biasing the Push-Pull Common-Source Amplifier

Illustration of Class B and Class AB Push-Pull, Inverting Amplifier

Output current and voltage characteristics of the push-pull, inverting amplifier ($R_L = 1k\Omega$):

Comments:
- Note that there is significant distortion at $v_{IN} = 0V$ for the Class B inverter
- Note that $v_{OUT}$ cannot reach the extreme values of $V_{DD}$ and $V_{SS}$
- $I_{OUT^+}(max)$ and $I_{OUT^-}(max)$ is always less than $V_{DD}/R_L$ or $V_{SS}/R_L$
- For $v_{OUT} = 0V$, there is quiescent current flowing in M1 and M2 for Class AB
BIPOLAR JUNCTION TRANSISTOR OUTPUT AMPLIFIERS

What about the use of BJTs?

![BJT Diagram](image)

Comments:
- Can use either substrate or lateral BJTs.
- Small-signal output resistance is $1/gm$ which can easily be less than 100$\Omega$.
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, $iB$, must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within $v_{BE}+V_{ON}$ of the power supply rails. This value can be 1V or more.

We will consider the BJT as an output stage in more detail in Sec. 7.1.

USING NEGATIVE FEEDBACK TO REDUCE THE OUTPUT RESISTANCE

Concept

![Feedback Diagram](image)

$$R_{out} = \frac{r_{ds1}||r_{ds2}}{1+\text{Loop Gain}}$$

Comments:
- Can achieve output resistances as low as 10$\Omega$.
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2.
- Great linearity because of the strong feedback.
- Can be efficient if operated in class B or class AB.
**Simple Implementation of Neg., Shunt Feedback to Reduce the Output Resistance**

![Fig. 060-08](image)

\[ \text{Loop gain} = \left( \frac{R_1}{R_1+R_2} \right) \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right) \]

\[ \therefore R_{out} = \frac{r_{ds1}\|r_{ds2}}{1+\left( \frac{R_1}{R_1+R_2} \right) \left( \frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}+G_L} \right)} \]

Let \( R_1 = R_2, \) \( R_L = \infty, \) \( I_{Bias} = 500 \mu A, \) \( W_1/L_1 = 100 \mu m/1 \mu m \) and \( W_2/L_2 = 200 \mu m/1 \mu m. \)

Thus, \( g_{m1} = 3.316 \text{mS}, \) \( g_{m2} = 3.162 \text{mS}, \) \( r_{ds1} = 50 \text{k}\Omega \) and \( r_{ds2} = 40 \text{k}\Omega. \)

\[ \therefore R_{out} = \frac{50 \text{k}\Omega\|40 \text{k}\Omega}{1+0.5(143.9)} = 22.22 \text{k}\Omega \]

\[ = \frac{304 \Omega}{143.9} \]  
\[ (R_{out} = 5.42 \text{k}\Omega \text{ if } R_L = 1 \text{k}\Omega) \]

---

**Summary of Output Amplifiers**

- The objectives are to provide output power in form of voltage and/or current.
- In addition, the output amplifier should be linear and be efficient.
- Low output resistance is required to provide power efficiently to a small load resistance.
- High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
- Types of output amplifiers considered:
  - Class A amplifier
  - Source follower
  - Class B and AB amplifier
  - Use of BJTs
  - Negative shunt feedback
SECTION 5.7 - SUMMARY

Summary of Chapter Topics

• Inverting Amplifiers
  - Class A (diode load and current sink/source load)
  - Class AB of B (push-pull)
• Differential Amplifiers
  - Need good common mode rejection
  - An excellent input stage for integrated circuit amplifiers
• Cascode Amplifiers
  - Useful for controlling the poles of an amplifier
• Current Amplifiers
  - Good for low power supplies
• Output Amplifiers
  - Minimize the output resistance
  - Maximize the current sinking/sourcing capability

APPENDIX 5A – FREQUENCY RESPONSE BASICS

Complex Frequency (s) Analysis of Circuits

The frequency response of linear circuits can be analyzed using the complex frequency variable \( s \) which avoids having to solve the circuit in the time domain and then transform into the frequency domain.

Passive components in the \( s \) domain are:

\[
Z_R(s) = R, \quad Z_L(s) = sL, \quad \text{and} \quad Z_C(s) = \frac{1}{sC}
\]

\( s \)-domain analysis uses the complex impedance of elements as if they were “resistors”.

Example:

Sum currents flowing away from node A to get,

\[
sC_1(V_2 - V_1) + g_mV_1 + G_2V_2 + sC_2V_2 = 0
\]

Solving for the voltage gain transfer function gives,

\[
T(s) = \frac{V_2(s)}{V_1(s)} = \frac{-sC_1 + g_m}{s(C_1 + C_2) + G_2} = -g_mR_2 \left( \frac{sC_1g_m - 1}{s(C_1 + C_2)R_2 + 1} \right)
\]
**Complex Frequency Plane**

The complex frequency variable, $s$, is really a complex number and can be expressed as

$$ s = \sigma + j\omega $$

where $\sigma = \text{Re}[s]$ and $\omega = \text{Im}[s]$.

Complex frequency plane:

It is useful to plot the roots of the transfer function on the complex frequency plane. For the previous $T(s)$, the roots are:

- The numerator root (zero) is $s = z_1 = +\left(\frac{g_m}{C_1}\right)$
- The denominator root (pole) is $s = p_1 = -\left[\frac{1}{R_2(C_1 + C_2)}\right]$

**Frequency Response**

Frequency response is the result when we replace the complex frequency variable $s$ with $j\omega$. (This amounts to evaluating $T(s)$ on the imaginary axis of the complex frequency plane.)

The frequency response is characterized by the magnitude and phase of $T(j\omega)$.

Example:

Assume $T(s) = \frac{a_0 + a_1s}{b_0 + b_1s} \quad s = j\omega \quad T(j\omega) = \frac{a_0 + a_1j\omega}{b_0 + b_1j\omega} = \frac{a_0 + j\omega a_1}{b_0 + j\omega b_1}$

Since $T(j\omega)$ is a complex number, we can express the magnitude and phase as,

$$ |T(j\omega)| = \sqrt{\frac{a_0^2 + (\omega a_1)^2}{b_0^2 + (\omega b_1)^2}} \quad \text{Arg}[T(j\omega)] = +\tan^{-1}\left(\frac{\omega a_1}{a_0}\right) - \tan^{-1}\left(\frac{\omega b_1}{b_0}\right) $$

For the previous example, the magnitude and phase would be,

$$ |T(j\omega)| = g_m R_2 \sqrt{\frac{1 + (\omega C_1/g_m)^2}{1 + [\omega R_2(C_1 + C_2)]^2}} $$

$$ \text{Arg}[T(j\omega)] = -\tan^{-1}(\omega C_1/g_m) - \tan^{-1}[\omega R_2(C_1 + C_2)] $$

Note: Because the zero is on the positive real axis, the phase due to the zero is $-\tan^{-1}()$ rather than $+\tan^{-1}()$. More about that later.
Graphical Illustration of Magnitude and Phase

The important concepts of frequency response are communicated through the graphical portrayal of the magnitude and phase.

Consider our example,

\[ T(s) = \frac{V_2(s)}{V_1(s)} = -g_m R_2 \left( \frac{s C_1 / g_m - 1}{s (C_1 + C_2) R_2 + 1} \right) = -T(0) \left( \frac{s / z_1 - 1}{s / p_1 - 1} \right) \]

where \( T(0) = g_m R_2 \), \( z_1 = +(g_m / C_1) \) and \( p_1 = -[1/R_2(C_1 + C_2)] \).

Replacing \( s \) with \( j \omega \) gives [remember \( \tan^{-1}(-x) = -\tan^{-1}(x) \)],

\[ |T(j \omega)| = T(0) \sqrt{\frac{1 + (\omega / z_1)^2}{1 + (\omega / p_2)^2}} \quad \text{and} \quad \text{Arg}[T(j \omega)] = -\tan^{-1}(\omega / z_1) - \tan^{-1}(\omega / p_2) \]

Graphically, we get the following if we assume \( |p_1| = 0.1 |z_1| \).

Graphical Illustration of Frequency Response – Continued

If the frequency range is large, it is more useful to use a logarithmic scale for the frequency. In addition, if one expresses the magnitude as \( 20 \log_{10}(|T(j \omega)|) \), the plots can be closely approximated with straight lines which enables quick analysis by hand. Such plots are called Bode plots.

To construct a Bode asymptotic magnitude plot for a low pass transfer function in the form of products of roots:
1.) Start at a low frequency and plot \( 20 \log_{10}(|T(0)|) \) until you reach the smallest root.
2.) At the frequency equal to magnitude of the smallest root, change to a line with a slope of +20dB/decade if the root is a zero or -20dB/decade if the root is a pole.
3.) Continue increasing in frequency until you have plotted the influence of all roots.
The Influence of the Complex Frequency Plane on Frequency Response

The root locations in the complex frequency plane have a direct influence on the frequency response as illustrated below. Consider the transfer function:

\[ T(s) = -T(0) \left( \frac{s}{z_1} - 1 \right) \left( \frac{|p_1|}{s/p_1} - 1 \right) = -0.1 T(0) \left( \frac{s-z_1}{s-p_1} \right) \]

where \( z_1 = 10|p_1| \).

Note: The roots maximally influence the magnitude when \( \omega \) is such that the angle between the vector and the horizontal axis is 45°. This occurs at \( j1 \) for \( p_1 \) and \( j10 \) for \( z_1 \).

Bandwidth of a Low-Pass Amplifier

One of the most important aspects of frequency analysis is to find the frequency at which the amplitude decreases by -3dB or \( 1/\sqrt{2} \). This can easily be found from the magnitude of the frequency response.

Amplifier with a Dominant Root:

Since the amplifier is low-pass, the poles will be smaller in magnitude than the zeros. If one of the poles is approximately 4-5 times smaller than the next smallest pole, the bandwidth of the amplifier is given as

\[ \text{Bandwidth} \approx |\text{Smallest pole}| \]

Amplifier with no Dominant Root:

If there are several poles with roughly the same magnitude, then one should use the graphical method above to find the bandwidth.
**Example of Finding the Bandwidth of an Amplifier**

Suppose an amplifier has a pole at -10 rads/sec and another at -20 rads/sec, and a zero at +50 radians/sec. Find the bandwidth of this amplifier if the low frequency gain is 100.

**Solution**

Since the poles are close together, construct a Bode plot and graphically find the bandwidth.

From the graph, we see that the -3dB bandwidth is close to 11-12 Rad/sec.