CHAPTER 3 – MODELS FOR CMOS COMPONENTS
INTRODUCTION

Chapter Outline
3.1 – Large Signal Transistor Models
3.2 – Process, Voltage, and Temperature Variations
3.3 – Small Signal Transistor Model
3.4 – Passive Component Models
3.5 – Matching of Components
3.6 – SPICE Models
3.7 – Model Extraction
3.8 – Summary

Models Suitable for Understanding Analog Design
The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

This chapter is devoted to the simple model suitable for design not using simulation.
Categorization of Electrical Models

<table>
<thead>
<tr>
<th>Linearity</th>
<th>Time Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear</td>
<td>Time Independent: Small-signal, midband ( R_{in}, A_v, R_{out} ) (.TF)</td>
</tr>
<tr>
<td></td>
<td>Time Dependent: Small-signal frequency response - poles and zeros (.AC)</td>
</tr>
<tr>
<td>Nonlinear</td>
<td>DC operating point: ( i_D = f(V_D, V_G, V_S, V_B) ) (.OP)</td>
</tr>
<tr>
<td></td>
<td>Large-signal transient response - Slew rate (.TRAN)</td>
</tr>
</tbody>
</table>

Based on the simulation capabilities of SPICE.

SECTION 3.1 – LARGE SIGNAL TRANSISTOR MOSFET MODELS

OPERATION OF THE MOSFET TRANSISTOR

Formation of the Channel for an Enhancement MOS Transistor

Subthreshold \((V_G < V_T)\)

Threshold \((V_G = V_T)\)

Strong Threshold \((V_G > V_T)\)
**Transconductance Characteristics of an Enhancement NMOSFET when \( V_{DS} = 0.1\, \text{V} \)**

- For \( V_{GS} \leq V_T \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = V_T \), \( V_D = 0.1\, \text{V} \)

- For \( V_{GS} = 2V_T \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = 2V_T \), \( V_D = 0.1\, \text{V} \)

- For \( V_{GS} = 3V_T \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = 3V_T \), \( V_D = 0.1\, \text{V} \)

**Output Characteristics of the Enhancement NMOS Transistor for \( V_{GS} = 2V_T \)**

- For \( V_{DS} = 0 \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = 2V_T \), \( V_D = 0\, \text{V} \)

- For \( V_{DS} = 0.5V_T \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = 2V_T \), \( V_D = 0.5V_T \)

- For \( V_{DS} = V_T \):
  - \( V_B = 0 \), \( V_S = 0 \), \( V_G = 2V_T \), \( V_D = V_T \)

A depletion region forms between the drain and channel.
Output Characteristics of the Enhanced NMOS when $V_{DS} = 2V_T$

$V_{GS} = V_T$

$V_G = 2V_T$

$V_{GS} = 3V_T$

Further increase in $V_G$ will cause the FET to become active.

Output Characteristics of an Enhancement NMOS Transistor

SPICE Input File:

```
MOS1 6 1 0 0 0 MOS1 w=5u l=1.0u VGS1 1 0 1.0
MOS2 6 2 0 0 0 MOS1 w=5u l=1.0u VGS2 2 0 1.5
MOS3 6 3 0 0 0 MOS1 w=5u l=1.0u VGS3 3 0 2.0
MOS4 6 4 0 0 0 MOS1 w=5u l=1.0u VGS4 4 0 2.5
MOS5 6 5 0 0 0 MOS1 w=5u l=1.0u VGS5 5 0 3.0
.model mos1 nmos (vto=0.7 kp=110u +gamma=0.4 +lambda=.04 phi=.7)
.dc vds 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4), ID(M5)
.end
```
Transconductance Characteristics of an Enhancement NMOS Transistor

SPICE Input File:

<table>
<thead>
<tr>
<th>Transconductance Characteristics for NMOS</th>
<th>M5 5 6 0 0 MOS1 w=5u l=1.0u</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 1 6 0 0 MOS1 w=5u l=1.0u</td>
<td>VDS 5 0 5.0</td>
</tr>
<tr>
<td>VDS1 1 0 1.0</td>
<td></td>
</tr>
<tr>
<td>M2 2 6 0 MOS1 w=5u l=1.0u</td>
<td>.model mos1 nmos (vto=0.7 kp=110u</td>
</tr>
<tr>
<td>VDS2 2 0 2.0</td>
<td>+gamma=0.4 lambda=.04 phi=.7)</td>
</tr>
<tr>
<td>M3 3 6 0 MOS1 w=5u l=1.0u</td>
<td>.dc vgs 0.5 .2</td>
</tr>
<tr>
<td>VDS3 3 0 3.0</td>
<td>.print dc ID(M1), ID(M2), ID(M3), ID(M4),</td>
</tr>
<tr>
<td>M4 4 6 0 MOS1 w=5u l=1.0u</td>
<td>ID(M5)</td>
</tr>
<tr>
<td>VDS4 4 0 4.0</td>
<td>.probe</td>
</tr>
<tr>
<td>VGS 6 0 5</td>
<td>.end</td>
</tr>
</tbody>
</table>

**Fig. 3.1-7**

SIMPLE LARGE SIGNAL MODEL (SAH MODEL)

**Large Signal Model Derivation**

1.) Let the charge per unit area in the channel inversion layer be

\[ Q_I(y) = -C_{ox}[V_{GS} - v(y) - V_T] \]  (coul./cm²)

2.) Define sheet conductivity of the inversion layer per square as

\[ \sigma_S = \mu_o Q_I(y) \left( \frac{cm^2}{v \cdot s \cdot coulombs \cdot cm^2} \right) = \text{amps/volt} = \frac{1}{\Omega/\text{sq}}. \]

3.) Ohm's Law for current in a sheet is

\[ J_S = \frac{i_D}{W} = -\alpha_S E_y = -\alpha_S \frac{dv}{dy} \rightarrow dv = \frac{-i_D}{\alpha_S W} \frac{dy}{dy} = \frac{-i_D dy}{\mu_o Q_I(y) W} \rightarrow i_D dy = -W \mu_o Q_I(y) dv \]

4.) Integrating along the channel for 0 to \( L \) gives

\[ \int_{0}^{L} i_D dy = - \int_{0}^{v_{DS}} W \mu_o Q_I(y) dv = \int_{0}^{v_{DS}} W \mu_o C_{ox}[V_{GS} - v(y) - V_T] dv \]

5.) Evaluating the limits gives

\[ i_D = \frac{W \mu_o C_{ox}}{L} \left[ (v_{GS} - V_T)v(y) - \frac{v^2(y) v_{DS}}{2} \right]_{0} \rightarrow i_D = \frac{W \mu_o C_{ox}}{L} \left[ (v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] \]
**Saturation Voltage - \( V_{DS(sat)} \)**

Interpretation of the large signal model:

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

\[
\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L} \left[ (v_{GS} - V_T) - v_{DS} \right] = 0
\]

\[
v_{DS(sat)} = v_{GS} - V_T
\]

Useful definitions:

\[
\frac{\mu_o C_{ox} W}{L} = K' W = \beta
\]

---

**The Simple Large Signal MOSFET Model**

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

\[v_{GS} - V_T < 0\]

\[i_D = 0\]

(Ignores subthreshold currents)

2.) Active Region

\[0 < v_{DS} < v_{GS} - V_T\]

\[i_D = \frac{\mu_o C_{ox} W}{2L} \left[ 2(v_{GS} - V_T) - v_{DS} \right] v_{DS}\]

3.) Saturation Region

\[0 < v_{GS} - V_T < v_{DS}\]

\[i_D = \frac{\mu_o C_{ox} W}{2L} (v_{GS} - V_T)^2\]
Illustration of the Need to Account for the Influence of $v_{DS}$ on the Simple Sah Model

Compare the Simple Sah model to SPICE level 2:

$V_{GS} = 2.0V$, $W/L = 100\mu m/100\mu m$, and no mobility effects.

Modification of the Previous Model to Include the Effects of $v_{DS}$ on $V_T$

From the previous derivation:

$$\int_0^L i_D \, dy = \int_0^{v_{DS}} VW_\mu Q(y) \, dv = \int_0^{v_{DS}} VW_\mu C_{ox} [V_{GS} - v(y) - V_T] \, dv$$

Assume that the threshold voltage varies across the channel in the following way:

$$V_T(y) = V_T + kv(y)$$

where $V_T$ is the value of $V_T$ the at the source end of the channel and $k$ is a constant.

Integrating the above gives,

$$i_D = \frac{W_\mu C_{ox}}{L} \left[ (V_{GS} - V_T)v(y) - (1+k) \frac{v^2(y)^{v_{DS}}}{2} \right]_0$$

or

$$i_D = \frac{W_\mu C_{ox}}{L} \left[ (V_{GS} - V_T)v_{DS} - (1+k) \frac{v_{DS}^2}{2} \right]$$

To find $v_{DS}(sat)$, set the $di_D/dv_{DS}$ equal to zero and solve for $v_{DS} = v_{DS}(sat)$,

$$v_{DS}(sat) = \frac{V_{GS} - V_T}{1 + k}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W_\mu C_{ox}}{2(1+k)L} (v_{GS} - V_T)^2$$

For $k = 0.5$ and $K' = 44.8 \mu A/V^2$, excellent correlation is achieved with SPICE 2.
**Influence of \( V_{DS} \) on the Output Characteristics**

Channel modulation effect:

As the value of \( V_{DS} \) increases, the effective \( L \) decreases causing the current to increase.

Illustration:

Note that \( L_{eff} = L - X_d \)

Therefore the model in saturation becomes,

\[
\begin{align*}
    i_D &= \frac{K'W}{2L_{eff}}(v_{GS} - V_T)^2 \rightarrow \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{eff}^2} (v_{GS} - V_T)^2 \frac{dL_{eff}}{dv_{DS}} = \frac{i_D}{L_{eff}} \frac{dX_d}{dv_{DS}} = \lambda i_D \\
\end{align*}
\]

Therefore, a good approximation to the influence of \( V_{DS} \) on \( i_D \) is

\[
    i_D \approx i_D(\lambda = 0) + di_D \frac{v_{DS}}{dv_{DS}} = i_D(\lambda = 0)(1 + \lambda v_{DS}) = \frac{K'W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})
\]

---

**Channel Length Modulation Parameter, \( \lambda \)**

Assume the MOS is transistor is saturated-

\[
    i_D = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})
\]

Define \( i_D(0) = i_D \) when \( v_{DS} = 0V \).

\[
    i_D(0) = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2
\]

Now,

\[
    i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0) v_{DS}
\]

Matching with \( y = mx + b \) gives the value of \( \lambda \)
Influence of Channel Length on $\lambda$

Note that the value of $\lambda$ varies with channel length, $L$. The data below is from a 0.25$\mu$m CMOS technology.

![Graph showing the influence of channel length on $\lambda$.](image)

Most analog designers stay away from minimum channel length to get better gains and matching at the sacrifice of speed.

Influence of the Bulk Voltage on the Large Signal MOSFET Model

The components of the threshold voltage are:

$V_T = \text{Gate-bulk work function} (\phi_{MS})$ + voltage to change the surface potential ($-2\phi_F$)

+ voltage to offset the channel-bulk depletion charge ($-Q_B/C_{OX}$)

+ voltage to compensate the undesired interface charge ($-Q_{SS}/C_{OX}$)

We know that $Q_B = \gamma \sqrt{2\phi_F + |v_{BS}|}$

Therefore, as the bulk becomes more reverse biased with respect to the source, the threshold voltage must increase to offset the increased channel-bulk depletion charge.
Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source ($v_{BS}$) influence on the transconductance characteristics:

In general, the simple model incorporates the bulk effect into $V_T$ by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma \sqrt{2|\phi_f| + |v_{BS}|} - \gamma \sqrt{2|\phi_f|}$$

Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

Non-saturation:

$$i_D = \frac{W\mu_oC_{ox}}{L} \left[ (v_{GS} - V_T) v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS})$$

Saturation:

$$i_D = \frac{W\mu_oC_{ox}}{L} \left[ (v_{GS} - V_T) v_{DS(sat)} - \frac{v_{DS(sat)}^2}{2} \right] (1 + \lambda v_{DS}) = \frac{W\mu_oC_{ox}}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

where:

$\mu_o$ = zero field mobility (cm$^2$/volt·sec)

$C_{ox}$ = gate oxide capacitance per unit area (F/cm$^2$)

$\lambda$ = channel-length modulation parameter (volts$^{-1}$)

$V_T = V_{T0} + \gamma \sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}$

$V_{T0}$ = zero bias threshold voltage

$\gamma$ = bulk threshold parameter (volts$^{-0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert the current.
**Silicon Constants**

<table>
<thead>
<tr>
<th>Constant Symbol</th>
<th>Constant Description</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_G$</td>
<td>Silicon bandgap (27°C)</td>
<td>1.205</td>
<td>V</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
<td>1.381x10^{-23}</td>
<td>J/K</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic carrier concentration (27°C)</td>
<td>1.45x10^{10}</td>
<td>cm^{-3}</td>
</tr>
<tr>
<td>$\varepsilon_o$</td>
<td>Permittivity of free space</td>
<td>8.854x10^{-14}</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_{si}$</td>
<td>Permittivity of silicon</td>
<td>11.7 $\varepsilon_o$</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_{ox}$</td>
<td>Permittivity of SiO2</td>
<td>3.9 $\varepsilon_o$</td>
<td>F/cm</td>
</tr>
</tbody>
</table>

**MOSFET Parameters**

Model Parameters for a Typical CMOS Bulk Process (0.25μm CMOS n-well):

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Parameter Description</th>
<th>Typical Parameter Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{T0}$</td>
<td>Threshold Voltage ($V_{BS} = 0$)</td>
<td>0.5± 0.15</td>
<td>V</td>
</tr>
<tr>
<td>$K'$</td>
<td>Transconductance Parameter (in saturation)</td>
<td>120.0 ± 10%</td>
<td>$\mu$A/V^{2}</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>Bulk threshold parameter</td>
<td>0.4</td>
<td>(V)^{1/2}</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Channel length modulation parameter</td>
<td>0.32 ($L=L_{min}$)</td>
<td>(V)^{-1}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.06 ($L \geq 2L_{min}$)</td>
<td></td>
</tr>
<tr>
<td>$2</td>
<td>\phi</td>
<td>F_l$</td>
<td>Surface potential at strong inversion</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.8</td>
<td></td>
</tr>
</tbody>
</table>
SUBTHRESHOLD MODEL

Large-Signal Model for Weak Inversion

The electrons in the substrate at the source side can be expressed as,
\[ n_p(0) = n_{po}\exp\left(\frac{\phi_s}{V_t}\right) \]
The electrons in the substrate at the drain side can be expressed as,
\[ n_p(L) = n_{po}\exp\left(\frac{\phi_s-V_{DS}}{V_t}\right) \]

Therefore, the drain current due to diffusion is,
\[ i_D = qADn \left(\frac{n_p(L)-n_p(0)}{L}\right) = \frac{W}{L} qXDn_{po}\exp\left(\phi_s\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right] \]

where \( X \) is the thickness of the region in which \( i_D \) flows.

In weak inversion, the changes in the surface potential, \( \Delta \phi_s \) are controlled by changes in the gate-source voltage, \( \Delta v_{GS} \), through a voltage divider consisting of \( C_{ox} \) and \( C_{js} \), the depletion region capacitance.

\[ \cdot \frac{d\phi_s}{dv_{GS}} = \frac{C_{ox}}{C_{ox}+C_{js}} = \frac{1}{n} \rightarrow \phi_s = \frac{v_{GS}}{n} + k_1 = \frac{v_{GS}-V_T}{n} + k_2 \]

where
\[ k_2 = k_1 + \frac{V_T}{n} \]

Define \( I_t \) as
\[ I_t = qXDn_{po}\exp\left(\frac{k_2}{V_t}\right) \]

to get,
\[ i_D = \frac{W}{L} I_t \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_t}\right)\right] \]

where \( n \approx 1.5 - 3 \)

If \( V_{DS} > 0 \), then
\[ i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left(1 + \frac{V_{DS}}{V_A}\right) \]

The boundary between nonsaturated and saturated is found as,
\[ V_{OV} = V_{DS}(sat) = V_{ON} = V_{GS} - V_T = 2nV_t \]
SHORT CHANNEL, STRONG INVERSION MODEL

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

An expression for the electron drift velocity as a function of the electric field is,

$$ v_d \approx \frac{\mu_n E}{1 + E/E_c} $$

where

- $v_d = \text{electron drift velocity (m/s)}$
- $\mu_n = \text{low-field mobility (≈ 0.07m}^2/\text{V} \cdot \text{s)}$
- $E_c = \text{critical electrical field at which velocity saturation occurs}$

Short-Channel Model Derivation

As before,

$$ J_D = J_S = \frac{i_D}{W} = Q_I(y)v_d(y) \rightarrow i_D = WQ_I(y)v_d(y) = \frac{WQ_I(y)\mu_n E}{1 + E/E_c} \rightarrow i_D \left(1 + \frac{E}{E_c}\right) = WQ_I(y)\mu_n E $$

Replacing $E$ by $dv/dy$ gives,

$$ i_D \left(1 + \frac{1}{E_c} \frac{dv}{dy}\right) = WQ_I(y)\mu_n \frac{dv}{dy} $$

Integrating along the channel gives,

$$ \int_0^L i_D \left(1 + \frac{1}{E_c} \frac{dv}{dy}\right)dy = \frac{v_{DS}}{W} \int_0^L WQ_I(y)\mu_n dv $$

The result of this integration is,

$$ i_D = \frac{\mu_n C_{OX}}{2(1 + \theta v_{DS})} \frac{W}{L} \left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right] = \frac{\mu_n C_{OX}}{2(1 + \theta v_{DS})} \frac{W}{L} \left[2(v_{GS} - V_T)v_{DS} - v_{DS}^2\right] $$

where $\theta = 1/(E_c L)$ with dimensions of $V^{-1}$. 

© P.E. Allen - 2006
Saturation Voltage
Differentiating $i_D$ with respect to $v_{DS}$ and setting equal to zero gives,

$$V'_{DS}(\text{sat}) = \frac{1}{\theta} \sqrt{1 + 2\theta(V_{GS}-V_T) - 1} \approx (V_{GS}-V_T) \left( 1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots \right)$$

if

$$\frac{\theta(V_{GS}-V_T)}{2} < 1$$

Therefore,

$$V'_{DS}(\text{sat}) \approx V_{DS}(\text{sat}) \left( 1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots \right)$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

Large Signal Model for the Saturation Region
Assuming that

$$\frac{\theta(V_{GS}-V_T)}{2} < 1$$

gives

$$V'_{DS}(\text{sat}) \approx (V_{GS}-V_T)$$

Therefore the large signal model in the saturation region becomes,

$$i_D = \frac{K'}{2[1 + \theta(V_{GS}-V_T)]} \frac{W}{L} [v_{GS} - V_T]^2, \quad v_{DS} \geq (V_{GS}-V_T) \left( 1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots \right)$$
The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for $K' = 110 \mu A/V^2$ and $W/L = 1$:

Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is the following:

We know that

$$i_D = \frac{K'W}{2L} (v_{GS'} - V_T)^2$$

and

$$v_{GS} = v_{GS'} + i_D R_{SX}$$

or

$$v_{GS'} = v_{GS} - i_D R_{XS}$$

Substituting $v_{GS'}$ into the current relationship gives,

$$i_D = \frac{K'W}{2L} (v_{GS} - i_D R_{SX} - V_T)^2$$

Solving for $i_D$ results in,

$$i_D = \frac{K'}{1 + \frac{K'W}{L} R_{SX}(v_{GS} - V_T)} \frac{W}{L} (v_{GS} - V_T)^2$$

Comparing with the previous result, we see that

$$\theta = K' \frac{W}{L} R_{SX} \quad \rightarrow \quad R_{SX} = \frac{\theta L}{K'W} = \frac{1}{E_c K'W}$$

Therefore for $K' = 110 \mu A/V^2$, $W = 1 \mu m$ and $E_c = 1.5 \times 10^6 V/m$, we get $R_{SX} = 6.06 \Omega$. 
CAPACITANCES OF THE MOSFET

Types of Capacitance

Physical Picture:

MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

MOSFET Depletion Capacitors

Model:

1.) \( v_{BS} \leq FC \cdot PB \)

\[
C_{BS} = \frac{CJ \cdot AS \cdot MJ}{(1 - \frac{v_{BS}}{PB})} + \frac{CJSW \cdot PS \cdot MJ \cdot SW}{(1 - \frac{v_{BS}}{PB})}
\]

and

2.) \( v_{BS} > FC \cdot PB \)

\[
C_{BS} = \frac{CJ \cdot AS \cdot MJ}{(1 - FC)} \left[ 1 - (1 + MJ)FC + MJ \frac{V_{BS}}{PB} \right] + \frac{CJSW \cdot PS \cdot MJ \cdot SW}{(1 - FC)} \left[ 1 - (1 + MJ)SWFC + MJ \frac{V_{BS}}{PB} \right]
\]

where

- \( AS \) = area of the source
- \( PS \) = perimeter of the source
- \( CJSW \) = zero bias, bulk source sidewall capacitance
- \( MJ \) = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "S" by "D" in the above.
**Charge Storage (Parallel Plate) MOSFET Capacitances - \( C_1, C_2, C_3 \) and \( C_4 \)**

Overlap capacitances:

\[
C_1 = C_3 = LD \cdot W_{eff} \cdot C_{ox} = CGSO \text{ or } CGDO
\]

(LD \approx 0.015 \ \mu m \text{ for LDD structures})

Channel capacitances:

\[
C_2 = \text{gate-to-channel} = C_{ox} \cdot W_{eff} \cdot (L-2LD) = C_{ox} \cdot W_{eff} \cdot L_{eff}
\]

\( C_4 = \text{voltage dependent channel-bulk/substrate capacitance} \)

---

**Charge Storage (Parallel Plate) MOSFET Capacitances - \( C_5 \)**

View looking down the channel from source to drain

\( C_5 = CGBO \)

Capacitance values based on an oxide thickness of 140 Å or \( C_{ox}=24.7 \times 10^{-4} \text{ F/m}^2 \):

<table>
<thead>
<tr>
<th>Type</th>
<th>P-Channel</th>
<th>N-Channel</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGSO</td>
<td>( 220 \times 10^{-12} )</td>
<td>( 220 \times 10^{-12} )</td>
<td>F/m</td>
</tr>
<tr>
<td>CGDO</td>
<td>( 220 \times 10^{-12} )</td>
<td>( 220 \times 10^{-12} )</td>
<td>F/m</td>
</tr>
<tr>
<td>CGBO</td>
<td>( 700 \times 10^{-12} )</td>
<td>( 700 \times 10^{-12} )</td>
<td>F/m</td>
</tr>
<tr>
<td>CJ</td>
<td>( 560 \times 10^{-6} )</td>
<td>( 770 \times 10^{-6} )</td>
<td>F/m^2</td>
</tr>
<tr>
<td>CJSW</td>
<td>( 350 \times 10^{-12} )</td>
<td>( 380 \times 10^{-12} )</td>
<td>F/m</td>
</tr>
<tr>
<td>MJ</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>MJSW</td>
<td>0.35</td>
<td>0.38</td>
<td></td>
</tr>
</tbody>
</table>
**Expressions for \( C_{GD}, C_{GS} \) and \( C_{GB} \)**

**Cutoff Region:**

\[
C_{GB} = C_2 + 2C_5 = C_{ox}(W_{eff})(L_{eff}) + 2CGBO(L_{eff})
\]

\[
C_{GS} = C_1 = C_{ox}(LD)W_{eff} = CGSO(W_{eff})
\]

\[
C_{GD} = C_3 = C_{ox}(LD)W_{eff} = CGDO(W_{eff})
\]

**Saturation Region:**

\[
C_{GB} = 2C_5 = CGBO(L_{eff})
\]

\[
C_{GS} = C_1 + (2/3)C_2 = C_{ox}(LD + 0.67L_{eff})(W_{eff})
\]

\[
= CGSO(W_{eff}) + 0.67C_{ox}(W_{eff})(L_{eff})
\]

\[
C_{GD} = C_3 = C_{ox}(LD)W_{eff} = CGDO(W_{eff})
\]

**Nonsaturated Region:**

\[
C_{GB} = 2C_5 = 2CGBO(L_{eff})
\]

\[
C_{GS} = C_1 + 0.5C_2 = C_{ox}(LD + 0.5L_{eff})(W_{eff})
\]

\[
= (CGSO + 0.5C_{ox}L_{eff})W_{eff}
\]

\[
C_{GD} = C_3 + 0.5C_2 = C_{ox}(LD + 0.5L_{eff})(W_{eff})
\]

\[
= (CGDO + 0.5C_{ox}L_{eff})W_{eff}
\]

**Illustration of \( C_{GD}, C_{GS} \) and \( C_{GB} \)**

Comments on the variation of \( C_{BG} \) in the cutoff region:

\[
C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4} + 2C_5}
\]

1.) For \( v_{GS} \approx 0 \), \( C_{GB} \approx C_2 + 2C_5 \)

\((C_4 \text{ is large because of the thin inversion layer in weak inversion where } V_{GS} \text{ is slightly less than } V_T)\)

2.) For \( 0 < v_{GS} \leq V_T \), \( C_{GB} \approx 2C_5 \)

\((C_4 \text{ is small because of the thicker inversion layer in strong inversion})\)
SECTION 3.2 – PROCESS, VOLTAGE, AND TEMPERATURE (PVT) VARIATIONS OF CMOS TECHNOLOGY

PROCESS VARIATIONS

How Does Technology Vary?

1.) Thickness variations in layers (dielectrics and metal)

2.) Doping variations

3.) Process biases – differences between the drawn and actual dimensions due to process (etching, lateral diffusion, etc.)

Large Signal Model Dependence on Process Variations

1.) Threshold voltage

\[ V_T = V_{T0} + \gamma \left( \sqrt{|-2\phi_F| + \sqrt{v_{SB}}} - \sqrt{|-2\phi_F|} \right) \]

where

\[ V_{T0} = \phi_{MS} - 2\phi_F \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \]

and

\[ \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \]

If \( V_{BS} = 0 \), then \( V_T \) is dependent on doping and oxide thickness because

\[ \phi_F = \frac{kT}{q} \ln \left( \frac{N_{SUB}}{n_i} \right) \]

and

\[ C_{ox} \propto \frac{1}{t_{ox}} \]

(Recall that the threshold is also determined by the threshold implant during processing)

2.) Transconductance parameter

\[ K' = \mu_o C_{ox} \propto \frac{1}{t_{ox}} \]

For short channel devices, the mobility is degraded as given by

\[ \mu_{eff} = \frac{\mu_o}{1 + \theta(V_{GS} - V_T)} \]

and

\[ \theta \approx \frac{2 \times 10^{-9} m/V}{t_{ox}} \]
**Process Variation “Corners”**

For strong inversion operation, the primary influence is the oxide thickness, $t_{OX}$. We see that $K'$ will tend to increase with decreasing oxide thickness whereas $V_T$ tends to decrease.

If the “speed” of a transistor is increased by increasing $K'$ and decreasing $V_T$, then the variation of technology can be expressed on a two-dimensional graph resulting in a rectangular area of “acceptable” process limitation.

![Diagram showing process variation corners]

**VOLTAGE VARIATION**

**What is Voltage Variation?**

Voltage variation is the influence of power supply voltage on the component. (There is also power supply influence on the circuit called power supply rejection ratio, PSRR. We will deal with this much later.)

Power supply variation comes from:

1. Influence of depletion region widths on components.
2. Nonlinearity
3. Breakdown voltage

Note: Because the large-signal model for the MOSFET includes all the influences of voltage on the transistor, we will focus on passive components except for breakdown.
**Models for Voltage Dependence of a Component**

1.) *i*th-order Voltage Coefficients

In general a variable \( y = f(v) \) which is a function of voltage, \( v \), can be expressed as a Taylor series,

\[
y(v = V_0) = y(V_0) + a_1(v - V_0) + a_2(v - V_0)^2 + a_3(v - V_0)^3 + \cdots
\]

where the coefficients, \( a_i \), are defined as,

\[
a_1 = \frac{df(v)}{dv} \bigg|_{v=V_0}, \quad a_2 = \frac{1}{2} \frac{d^2f(v)}{dv^2} \bigg|_{v=V_0}, \quad \ldots.
\]

The coefficients, \( a_i \), are called the first-order, second-order, … voltage coefficients.

2.) Fractional Voltage Coefficient or Voltage Coefficient

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional voltage coefficient*, \( VCF \), which is defined as,

\[
VCF(v=V_0) = \frac{1}{f(v=V_0)} \frac{df(v)}{dv} \bigg|_{v=V_0} \text{ parts per million/V (ppm/V)}
\]

or more simply,

\[
VCF = \frac{1}{f(v)} \frac{df(v)}{dv} \text{ parts per million/V (ppm/V)}
\]

---

**Influence of Voltage on a Diffused Resistor – Depletion Region**

Influence of the depletion region on the \( p^+ \) resistor:

As the voltage at the terminals of the resistor become smaller than the \( n \)-well potential, the depletion region will widen causing the thickness of the resistor to decrease.

\[
R = \frac{\rho L}{NW} \propto \sqrt{V_R}
\]

where \( V_R \) is the reverse bias voltage from the resistor to the well.

This effect is worse for well resistors because the doping concentration of the resistor is smaller.

Voltage coefficient for diffused resistors \( \approx 200-800 \text{ ppm/V} \)

Voltage coefficient for well resistors \( \approx 8000 \text{ ppm/V} \)
Voltage Nonlinearity

Conductivity modulation:
As the current in a resistor increases, the conductivity becomes modulated and the resistance increases.

Example of a $n$-well resistor:

As the reverse bias voltage across a $pn$ junction becomes large, at some point, called the breakdown voltage, the current will rapidly increase. Both transistors, diodes and depletion capacitors experience this breakdown.

Model for current multiplication factor:

$$M = \frac{1}{1 + \left(\frac{v_R}{BV}\right)^n}$$

TEMPERATURE VARIATIONS

Models for Voltage Dependence of a Component

1.) $i$th-order Temperature Coefficients

As for voltage, the temperature dependence can be expressed as,

$$y(T = T_0) = y(T_0) + a_1(T - T_0) + a_2(T - T_0)^2 + a_3(T - T_0)^3 + \cdots$$

where the coefficients, $a_i$, are defined as,

$$a_1 = \left. \frac{df(T)}{dT} \right|_{T = T_0}, \quad a_2 = \left. \frac{d^2f(T)}{dT^2} \right|_{T = T_0}, \quad \ldots.$$ 

The coefficients, $a_i$, are called the first-order, second-order, ..., temperature coefficients.

2.) Fractional Temperature Coefficient or Temperature Coefficient

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called fractional temperature coefficient, $TC_F$, which is defined as,

$$TC_F(T = T_0) = \left. \frac{df(T)}{dT} \right|_{T = T_0}$$

parts per million/°C (ppm/°C)

or more simply,

$$TC_F = \frac{1}{f(T)} \frac{df(T)}{dT}$$

parts per million/°C (ppm/°C)
**Temperature Dependence of the MOSFET**

Transconductance parameter:

\[ K'(T) = K'(T_0) \left( \frac{T}{T_0} \right)^{-1.5} \]

(Exponent becomes +1.5 below 77°K)

Threshold Voltage:

\[ V_T(T) = V_T(T_0) + \alpha(T - T_0) + \cdots \]

Typically \( \alpha_{\text{NMOS}} = -2\text{mV/°C} \) to \(-3\text{mV/°C} \) from 200°K to 400°K (PMOS has a + sign)

**Example**

Find the value of \( I_D \) for a NMOS transistor at 27°C and 100°C if \( V_{GS} = 2\text{V} \) and \( W/L = 5\mu m/1\mu m \) if \( K'(T_0) = 110\mu A/V^2 \) and \( V_T(T_0) = 0.7\text{V} \) and \( T_0 = 27°C \) and \( \alpha_{\text{NMOS}} = -2\text{mV/°C} \).

**Solution**

At room temperature, the value of drain current is,

\[ I_D(27°C) = \frac{110\mu A/V^2 \times 5\mu m}{2 \times 1\mu m} \times (2-0.7)^2 = 465\mu A \]

At \( T = 100°C \) (373°K),

\[ K'(100°C) = K'(27°C) \left( \frac{373}{300} \right)^{-1.5} = 110\mu A/V^2 \times 0.7 = 79.3\mu A/V^2 \]

\[ V_T(100°C) = 0.7 - (0.002)(73°C) = 0.554\text{V} \]

\[ I_D(100°C) = \frac{79.3\mu A/V^2 \times 5\mu m}{2 \times 1\mu m} \times (2-0.554)^2 = 415\mu A \] (Repeat with \( V_{GS} = 1.5\text{V} \))

---

**Zero Temperature Coefficient (ZTC) Point for MOSFETs**

For a given value of gate-source voltage, the drain current of the MOSFET will be independent of temperature. Consider the following circuit:

Assume that the transistor is saturated and that:

\[ \mu = \mu_0 \left( \frac{T}{T_0} \right)^{1.5} \]

and \( V_T(T) = V_T(T_0) + \alpha(T-T_0) \)

where \( \alpha = -0.0023\text{V/°C} \) and \( T_0 = 27°C \)

\[ I_D(T) = \frac{\mu_0 C_{ox} W}{2L} \left( \frac{T}{T_0} \right)^{-1.5} \left[ V_{GS} - V_{T0} - \alpha(T-T_0) \right]^2 \]

\[ \frac{dI_D}{dT} = -1.5 \frac{\mu_0 C_{ox}}{2T_0} \left( \frac{T}{T_0} \right)^{2.5} [V_{GS}-V_{T0}-\alpha(T-T_0)]^2 + \mu_0 C_{ox} \left[ \frac{T}{T_0} \right]^{-1.5} [V_{GS}-V_{T0}-\alpha(T-T_0)] = 0 \]

\[ \Rightarrow \quad V_{GS} - V_{T0} - \alpha(T-T_0) = \frac{-4T\alpha}{3} \quad \Rightarrow \quad V_{GS(\text{ZTC})} = V_{T0} - \alpha T_0 - \frac{\alpha T}{3} \]

Let \( K' = 10\mu A/V^2 \), \( W/L = 5 \) and \( V_{T0} = 0.71\text{V} \).

At \( T=27°C(300°K) \), \( V_{GS(\text{ZTC})} = 0.71 - (-0.0023)(300°K)-(0.333)(-0.0023)(300°K) = 1.63\text{V} \)

At \( T = 27°C (300°K) \), \( I_D = (10\mu A/V^2)(5/2)(1.63-0.71)^2 = 21.2\mu A \)

At \( T=200°C(473°K) \), \( V_{GS(\text{ZTC})} = 0.71 - (-0.0023)(300°K)-(0.333)(-0.0023)(473°K) = 1.76\text{V} \)
**Experimental Verification of the ZTC Point**

The data below is for a 5\(\mu\)m n-channel MOSFET with \(W/L=50\mu m/10\mu m\), \(N_A=10^{16} \text{ cm}^{-3}\), \(t_{ox} = 650\AA\), \(u_oC_{ox} = 10\mu A/V^2\), and \(V_{T0} = 0.71\text{V}\).

![Graph showing the ZTC point across different temperatures and voltage conditions.](image)

A similar result holds for the p-channel MOSFET. UDSM technology may not yield a well-defined ZTC point.

---

**Bulk-Drain (Bulk-Source) Leakage Currents**

Cross-section of a NMOS in a p-well:

\(V_{GS}>V_T\):

\(V_{GS}<V_T\):

![Cross-section diagram showing leakage currents under different gate-source voltages.](image)
**Temperature Modeling of the PN Junction**

PN Junctions (Reverse-biased only):

\[ -i_D \equiv I_s = qA \left[ \frac{D_{pp\text{no}}}{L_p} + \frac{D_{nn\text{po}}}{L_n} \right] \equiv \frac{qAD}{L} \frac{n_i^2}{N} = KT^3 \exp \left( \frac{-V_{Go}}{V_t} \right) \]

Differentiating with respect to temperature gives,

\[ \frac{dI_s}{dT} = \frac{3KT^3}{T} \exp \left( \frac{-V_{Go}}{V_t} \right) + \frac{qKT^3}{VT^2} \exp \left( \frac{-V_{Go}}{V_t} \right) = \frac{3I_s}{T} + I_s \frac{V_{Go}}{VT} \]

**TCF**

\[ TCF = \frac{dI_s}{I_s dT} = \frac{3}{T} + \frac{1}{T} \frac{V_{Go}}{V_t} \]

**Example**

Assume that the temperature is 300°K (room temperature) and calculate the reverse diode current change and the **TCF** for a 5°K increase.

**Solution**

The **TCF** can be calculated from the above expression as \( TCF = 0.01 + 0.155 = 0.165 \).

Since the **TCF** is change per degree, the reverse current will increase by a factor of 1.165 for every degree K (or °C) change in temperature. Multiplying by 1.165 five times gives an increase of approximately 2. Thus, the reverse saturation current approximately doubles for every 5°C temperature increase. Experimentally, the reverse current doubles for every 8°C increase in temperature because the reverse current is in part leakage current.

---

**Experimental Verification of the PN Junction Temperature Dependence**

![Graph showing leakage current vs. temperature for different minimum lengths](image)

**Theory:**

\[ I_s(T) \propto T^3 \exp \left( \frac{V_g(T)}{kT} \right) \]
Temperature Modeling of the PN Junction – Continued

PN Junctions (Forward biased – \( v_D \) constant):

\[ i_D \equiv I_s \exp \left( \frac{v_D}{V_T} \right) \]

Differentiating this expression with respect to temperature and assuming that the diode voltage is a constant (\( v_D = V_D \)) gives

\[ \frac{di_D}{dT} = I_s \frac{dI_s}{dT} \frac{1}{I_s} \frac{V_D}{V_T} i_D \]

The fractional temperature coefficient for \( i_D \) is

\[ \frac{1}{i_D} \frac{di_D}{dT} = \frac{dI_s}{dT} - \frac{V_D}{V_T} \left( \frac{1}{I_s} \frac{V_D}{V_T} \right) i_D \]

If \( V_D \) is assumed to be 0.6 volts, then the fractional temperature coefficient is equal to 0.01 + (0.155 - 0.077) = 0.0879. The forward diode current will approx. double for a 10°C.

PN Junctions (Forward biased – \( i_D \) constant):

\[ V_D = V_T \ln \left( \frac{i_D}{I_s} \right) \]

Differentiating with respect to temperature gives

\[ \frac{dV_D}{dT} = \frac{v_D}{T} \frac{1}{I_s} \frac{dI_s}{dT} = \frac{V_D}{T} \frac{3V_T}{T} \frac{V_G_T - V_D}{V_T} - \frac{3V_T}{T} \]

Assuming that \( V_D = V_D = 0.6 \text{ V} \) the temperature dependence of the forward diode voltage at room temperature is approximately -2.3 mV/°C.

Resistor Dependence on Temperature

Diffused Resistors:

The temperature dependence of resistors depends mostly on the doping level of diffused and implanted resistors. As the doping level or sheet resistance increases from 100 Ω/□ to 400 Ω/□, the temperature coefficient varies from about +1000 ppm/°C to +4000 ppm/°C. Diffused and implanted resistors have good thermal conduction to the substrate or well.

Poly silicon Resistors:

Typically has a sheet resistance of 20 Ω/□ to 80 Ω/□ and has poor thermal conduction because it is electrically isolated by oxide layers.

Metal:

Metal is often used for resistors and has a positive temperature coefficient.

Temperature Coefficients of Resistors:

- \( n \)-well = 4000 ppm/°C
- Diffusion = +1500 ppm/°C
- Polysilicon = 500-2000 ppm/°C
- Ion implanted = +400 ppm/°C
- Metal = +3800 ppm/°C (aluminum)
### SECTION 3.3 – SMALL SIGNAL TRANSISTOR MOSFET MODELS

#### FREQUENCY INDEPENDENT

**What is a Small Signal Model?**

The small signal model is a linear approximation of a nonlinear model.

Mathematically:

\[ i_D = \frac{\beta}{2} (v_{GS} - V_T)^2 \]

Large Signal to Small Signal

\[ i_d = g_m v_{gs} \]

Graphically:

The large signal curve at point \( Q \) has been approximated with a small signal model going through the point \( Q \) and having a slope of \( g_m \).

---

**Why Small Signal Models?**

The small signal model is a linear approximation to the large signal behavior.

1. The transistor is biased at given DC operating point (Point \( Q \) above)
2. Voltage changes are made about the operating point.
3. Current changes result from the voltage changes.

If the designer is interested in only the current changes and not the DC value, then the small signal model is a fast and simple way to find the current changes given the voltage changes.
How Good is the Small Signal Model?
It depends on how large are the changes and how nonlinear is the large signal model.

- The parameters of the small signal model will depend on the values of the large signal model.
- The model is a tradeoff in complexity versus accuracy (we will choose simplicity and give up accuracy).
- What does a simulator do? Exactly the same thing when it makes an ac analysis (i.e. frequency response)
- Regardless of the approximate nature of the small signal model, it is the primary model used to predict the signal performance of an analog circuit.

Small-Signal Model for the Saturation Region
The small-signal model is a linearization of the large signal model about a quiescent or operating point.

Consider the large-signal MOSFET in the saturation region \( v_{DS} \approx v_{GS} - V_T \):

\[
 i_D = \frac{W\mu_0 C_Ox}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})
\]

The small-signal model is the linear dependence of \( i_D \) on \( v_{gs} \), \( v_{bs} \), and \( v_{ds} \). Written as,

\[
 i_D \approx g_m v_{gs} + g_{mb} v_{bs} + g_{ds} v_{ds}
\]

where

\[
 g_m = \left. \frac{dI_D}{dv_{GS}} \right|_Q = \beta (v_{GS} - V_T) = \sqrt{2\beta I_D}
\]

\[
 g_{ds} = \left. \frac{dI_D}{dv_{DS}} \right|_Q = \frac{\lambda I_D}{1 + \lambda v_{DS}} \approx \lambda I_D
\]

and

\[
 g_{mb} = \left. \frac{dI_D}{dv_{BS}} \right|_Q = \left( \frac{dI_D}{dv_{GS}} \right) \left( \frac{dv_{GS}}{dv_{BS}} \right) \left|_Q = - \left( \frac{dI_D}{dv_{T}} \right) \left( \frac{dv_{T}}{dv_{BS}} \right) \right|_Q = \frac{g_m \gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} = \eta g_m
\]
Small-Signal Model – Continued

Complete schematic model:

where

\[ g_m = \frac{dI_D}{dV_{GS}} = \beta (V_{GS} - V_T) = \sqrt{2|\beta|} I_D \]

and

\[ g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}} = \lambda I_D \]

Simplified schematic model:

An extremely important assumption:

\[ g_m \approx 10g_{mbs} \approx 100g_{ds} \]

An Alternate Way of Deriving the Small Signal Model

Large-Signal Characteristics:

Ignore channel modulation-

\[ i = I_D = \frac{K'W}{2L} (v_{GS} - V_T)^2 = \frac{\beta}{2} (v_{GS} - V_T)^2 \quad \text{and} \quad V = v_{GS} = v_{DS} = V_T + \sqrt{\frac{2I_D}{\beta}} \]

Small-Signal Characteristics:

The small signal model is a linearization of the large signal model at an operating point.

\[ i_d + I_D = \left( \frac{\beta}{2} (v_{GS} - V_T)^2 + \frac{\beta}{2} v_{gs}^2 + \beta (V_{GS} - V_T)v_{gs} + \frac{\beta}{2} (V_{GS} - V_T)^2 + \frac{\beta}{2} v_{gs}^2 \lambda v_{ds} + \beta (V_{GS} - V_T)v_{gs} \lambda v_{ds} + \frac{\beta}{2} (V_{GS} - V_T)^2 \lambda v_{DS} \right) \]

Assume that \( v_{gs} < V_{GS} - V_T, v_{ds} < V_{DS} \) and \( \lambda \ll 1 \). Therefore we write:

\[ i_d + I_D = \beta (V_{GS} - V_T)v_{gs} + \frac{\beta}{2} (V_{GS} - V_T)^2 \lambda v_{ds} + \frac{\beta}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ i_d = \beta (V_{GS} - V_T)v_{gs} + \frac{\beta}{2} (V_{GS} - V_T)^2 \lambda v_{ds} = g_m v_{gs} + g_{ds} v_{ds} \quad \text{and} \quad I_D = \frac{\beta}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]
Small-Signal Model for the Nonsaturated Region

\[ g_m = \frac{\partial i_D}{\partial v_{GS}} \bigg|_{Q} = \frac{K'W V_{DS}}{L} (1 + \lambda V_{DS}) \approx \left(\frac{K'W}{L}\right) V_{DS} \]

\[ g_{mbs} = \frac{\partial i_D}{\partial v_{BS}} \bigg|_{Q} = \frac{K'W V_{DS}}{2L\sqrt{2\phi_F - V_{BS}}} \]

\[ g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \bigg|_{Q} = \frac{K'W}{L} (V_{GS} - V_T - V_{DS})(1 + \lambda V_{DS}) + \frac{I_D \lambda}{1 + \lambda V_{DS}} \approx \frac{K'W}{L} (V_{GS} - V_T - V_{DS}) \]

Note:
While the small-signal model analysis is independent of the region of operation, the evaluation of the small-signal performance is not.

Small Signal Model for the Subthreshold Region

If \( V_{DS} > 0 \), then

\[ i_D = K_x \frac{W}{L} e^{v_{GS}/nV_t} (1 + \lambda V_{DS}) \]

Small-signal model:

\[ g_m = \frac{di_D}{dv_{GS}} \bigg|_{Q} = \frac{qI_D}{n kT} \]

\[ g_{ds} = \frac{di_D}{dv_{DS}} \bigg|_{Q} \approx \frac{I_D}{V_A} \]
FREQUENCY DEPENDENT SMALL SIGNAL MODEL

Small-Signal Frequency Dependent Model
The depletion capacitors are found by evaluating the large signal capacitors at the DC operating point.

The charge storage capacitors are constant for a specific region of operation.

Gain-bandwidth of the MOSFET ($f_T$)
The short-circuit current gain is measure of the frequency capability of the MOSFET. Small signal model:

\[ i_{out} = g_m v_{gs} - s C_{gd} v_{gs} \quad \text{and} \quad v_{gs} = \frac{i_{in}}{s(C_{gs} + C_{gd})} \]

Therefore,

\[ \frac{i_{out}}{i_{in}} = \frac{g_m s C_{gd}}{s(C_{gs} + C_{gd})} \approx \frac{g_m}{s(C_{gs} + C_{gd})} \]

Assume $V_{SB} = 0$ and the MOSFET is in saturation,

\[ f_T = \frac{1}{2 \pi C_{gs} + C_{gd}} \approx \frac{1}{2 \pi C_{gs}} \]

Recalling that

\[ C_{gs} \approx \frac{2}{3} C_{ox} W L \quad \text{and} \quad g_m = \mu_o C_{ox} W (V_{GS} - V_T) \quad \rightarrow \quad f_T = \frac{3}{4 \pi L^2} (V_{GS} - V_T) \]
NOISE MODELS

MOS Device Noise at Low Frequencies

where

\[ i_n^2 = \left[ \frac{8kTg_m(1+\eta)}{3} + \frac{KF I_D}{g_m^2} \right] \Delta f \] (amperes\(^2\))

\[ \Delta f = \text{bandwidth at a frequency, } f \]

\[ \eta = \frac{g_{mbs}}{g_m} \]

\( k \) = Boltzmann’s constant

\( KF \) = Flicker noise coefficient

\( S \) = Slope factor of the 1/f noise

Reflecting the MOSFET Noise to the Gate

Dividing \( i_n^2 \) by \( g_m^2 \) gives

\[ e_n^2 = \frac{i_n^2}{g_m^2} = \left[ \frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2g_m^2} \right] \Delta f \] (volts\(^2\))

It will be convenient to use \( B = \frac{KF}{2g_m^2} \) for model simplification.

Frequency response of MOSFET noise:

Noise Spectral Density

1/f noise

Thermal noise

\( f_{\text{Corner}} \)

\( \log_{10} f \)

060311-06

CMOS Analog Circuit Design

© P.E. Allen - 2006
**MOSFET Noise Model at High Frequencies**

At high frequencies, the source resistance can no longer be assumed to be small. Therefore, a noise current generator at the input results.

**MOSFET Noise Models:**

-MOSFET Noise Model at High Frequencies – Continued

To find $e_{i_2}^2$ and $i_{i_2}^2$, we will perform the following calculations:

$e_{i_2}^2$:

Short-circuit the input and find $i_{o_2}^2$ of both models and equate to get $e_{i_2}^2$.

\[
\text{Ckt. 1: } i_{o_2}^2 = i_{n_2}^2 \\
\text{Ckt. 2: } i_{o_2}^2 = g_m^2 e_{i_2}^2 + (\omega C_{gd})^2 e_{i_2}^2
\]

\[
e_{i_2}^2 = \frac{i_{n_2}^2}{g_m^2 + (\omega C_{gd})^2}
\]

$i_{i_2}^2$:

Open-circuit the input and find $i_{o_2}^2$ of both models and equate to get $i_{i_2}^2$.

\[
\text{Ckt. 1: } i_{o_2}^2 = i_{n_2}^2 \\
\text{Ckt. 2: } i_{o_2}^2 = \left(\frac{1}{1/C_{ds}} + \frac{1}{1/C_{gs}}\right)^{-1} i_{i_2}^2 + g_m^2 i_{i_2}^2 \\
= \frac{g_m^2}{\omega^2 C_{gs}^2} i_{n_2}^2 \text{ if } C_{gd} < C_{gs} \quad \Rightarrow \quad i_{i_2}^2 = \frac{\omega^2 C_{gs}^2}{g_m^2} i_{n_2}^2
\]
SECTION 3.4 – PASSIVE COMPONENT MODELS

RESISTOR

Resistor Models

1.) Large signal

\[ i = \frac{v}{R} \]

2.) Small signal

\[ v = Ri \]

3.) Noise

\[ e_n^2 = 4kTR \quad \text{or} \quad i_n^2 = 4kTG \]

CAPACITOR

Capacitor Models

One of the parasitic capacitors is the top plate and the other is associated with the bottom plate.

1.) Large signal

2.) Small signal

\[ q = Cv \quad \rightarrow \quad i = C(dv/dt) \]

3.) Do capacitors have noise? See next page.
**Switched Capacitor Circuits - kT/C Noise**

Capacitors and switches generate an inherent thermal noise given by $kT/C$. This noise is verified as follows.

An equivalent circuit for a switched capacitor:

The noise voltage spectral density of switched capacitor above is given as

$$e_{Ron}^2 = 4kTR_{on} \text{ Volts}^2/\text{Hz} = \frac{2kTR_{on}}{\pi} \text{ Volt}^2/\text{Rad./sec.}$$

The rms noise voltage is found by integrating this spectral density from 0 to $\infty$ to give

$$v_{Ron}^2 = \frac{2kTR_{on}}{\pi} \int_{0}^{\infty} \frac{\omega_1^2 d\omega}{\omega_1^2 + \omega^2} = \frac{2kTR_{on}}{\pi} \left( \frac{\pi}{2} \right) = \frac{kT}{C} \text{ Volts(rms)}^2$$

where $\omega_1 = 1/(R_{on}C)$. Note that the switch has an effective noise bandwidth of

$$f_{sw} = \frac{1}{4R_{on}C} \text{ Hz}$$

which is found by dividing the second relationship by the first.

**INDUCTOR**

**Inductor Models**

$R$ = losses of the inductor

$C_p$ = parasitic capacitance to ground

$R_p$ = losses due to eddy currents caused by magnetic flux

1.) Large Signal

2.) Small signal

$$\psi = L i \rightarrow \frac{d\psi}{dt} = v = L \frac{di}{dt}$$

3.) Mutual inductance

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

$$k = \frac{M}{\sqrt{L_1L_2}}$$
INTERCONNECTS

Types of “Wires”

1.) Metal
   Many layers are available in today’s technologies:
   - Lower level metals have more resistance (70 mΩ/sq.)
   - Upper level metal has the less resistance because it is thicker (50 mΩ/sq.)

2.) Polysilicon
   Better resistor than conductor (unpolysicided) (135Ω/sq.)
   Silicided polysilicon has a lower resistance (5Ω/sq.)

3.) Diffusion
   Reasonable for connections if silicided (5Ω/sq.)
   Unsilicided (55Ω/sq.)

4.) Vias
   Vias are vertical metal (tungsten plugs or aluminum)
   - Connect metal layer to metal layer (3.5Ω/via)
   - Connect metal to silicon or polysilicon contact resistance (5Ω/contact)

Ohmic Contact Resistance

The metal to silicon contact generates resistance because of the presence of a potential barrier between the metal and the silicon.

Contact and Via Resistance:

<table>
<thead>
<tr>
<th>Contact System</th>
<th>Contact Resistance (Ω/μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al-Cu-Si to 160Ω/sq. base</td>
<td>750</td>
</tr>
<tr>
<td>Al-Cu-Si to 5Ω/sq. emitter</td>
<td>40</td>
</tr>
<tr>
<td>Al-Cu/Ti-W/PtSi to 160Ω/sq. base</td>
<td>1250</td>
</tr>
<tr>
<td>Al-Cu/Al-Cu (Via)</td>
<td>5</td>
</tr>
<tr>
<td>Al-Cu/Ti-W/Al-Cu (Via)</td>
<td>5</td>
</tr>
</tbody>
</table>
Capacitance of Wires

Self, fringing and coupling capacitances:

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>Typical Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal to diffusion, Self capacitance</td>
<td>33</td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Metal to diffusion, Fringe capacitance, minimum spacing</td>
<td>7</td>
<td>aF/μm</td>
</tr>
<tr>
<td>Metal to diffusion, Fringe capacitance, wide spacing</td>
<td>40</td>
<td>aF/μm</td>
</tr>
<tr>
<td>Metal to metal, Coupling capacitance, minimum spacing</td>
<td>85</td>
<td>aF/μm</td>
</tr>
<tr>
<td>Metal to substrate, Self capacitance</td>
<td>28</td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Metal to substrate, Fringe capacitance, minimum spacing</td>
<td>4</td>
<td>aF/μm</td>
</tr>
<tr>
<td>Metal to substrate, Fringe capacitance, wide spacing</td>
<td>39</td>
<td>aF/μm</td>
</tr>
</tbody>
</table>

Example of Coupling between the Input and Output of an Amplifier

For the NMOS in the layout below, find the location of the RHP zero caused by the capacitive coupling due only to the metal-to-metal coupling capacitance between \( V_{out} \) and \( V_{in} \) metal lines. Assume the transconductance is 775\( \mu \)S and \( C_{gd} = 3\)fF.

Assuming minimum spacing and 40\( \mu \)m of coupling gives \( C_{coupling} = 3.4\)fF. The RHP zero is given by,

\[
RHP\ zero = \frac{g_m}{C_{coupling} + C_{gd}} = \frac{775\mu S}{6.4fF} = 1.21 \times 10^{11} \text{ radians/sec. (19.3 GHz)}
\]
Electromigration

Electromigration occurs if the current density is too large and the pressure of carrier collisions on the metal atoms causes a slow displacement of the metal.

Black’s law:

$$\text{MTF} = \frac{1}{A J^2} \exp\left(\frac{E_a}{kT_j}\right)$$

Where

- $A = \text{rate constant (cm}^4/\text{A}^2/\text{hr})$
- $J = \text{current density (A/cm}^2)$
- $E_a = \text{activation energy in electron volts (0.5eV for Al and 0.7eV for Cu doped Al)}$
- $k = \text{Boltzmann’s constant (8.6x10}^{-5}\ \text{eV/K)}$

Electromigration leads to a maximum current density, $J_{max}$. $J_{max}$ for copper doped aluminum is $5 \times 10^5$ A/cm$^2$ at 85°C.

If $t = 10,000$ Angstroms and $J_{max} = 5 \times 10^5$ A/cm$^2$, then a 10μm wide lead can conduct no more than 50mA at 85°C.

Where is AC Ground on the Chip?

AC grounds on the chip are any area tied to a fixed potential. This includes the substrate and the wells. All parasitic capacitances are in reference to these points.
What is a Ground?

Ground is simply another power supply whose value is supposed to be zero and is used as a reference for all other voltages.

- DC ground is a point in the circuit where the DC voltage is supposed to be zero.
- AC ground is a point in the circuit where the AC voltage is supposed to be zero.

![Diagram of a CMOS Analog Circuit Design](image)

Grounds that are Not Grounds

Because of the resistance of “wires”, current flowing through a wire can cause a voltage drop.

An example of good and bad practice:
**Kelvin Connections**
Avoid unnecessary ohmic drops.

![Ohmic vs Kelvin Connections](image)

In the left-hand connection, an *IR* drop is experienced between X and Y causing the potentials at A and B to be slightly different.

For example, let the current be $100\mu A$ and the metal be $30m\Omega/sq$. Suppose that the distance between X and Y is 100 squares. Therefore, the *IR* drop is

$100\mu A \times 30m\Omega/sq. \times 100sq. = 0.3mV$

---

**MODELING OF SUBSTRATE NOISE**

**How Do Carriers Get Injected into the Substrate?**

1.) Hot carriers (substrate current)
2.) Electrostatic coupling (across depletion regions and other dielectrics)
3.) Electromagnetic coupling (parallel conductors)

**Why is this a Problem?**

With decreasing channel lengths, more circuitry is being integrated on the same substrate. The result is that noisy circuits (circuits with rapid transitions) are beginning to adversely influence sensitive circuits (such as analog circuits).

**Present Solution**

Keep circuit separate by using multiple substrates and put the multiple substrates in the same package.
Hot Carrier Injection in CMOS Technology without an Epitaxial Region

![Diagram of Noisy and Quiet Circuits]

- **Noisy Circuits**: 
  - Digital Ground
  - VDD
  - Vin
  - Vout
  - n+ channel stop (1 Ω-cm)
  - p+ substrate (10 Ω-cm)
  - Intrinsic Doping

- **Quiet Circuits**: 
  - Analog Ground
  - VDD (Analog)
  - Vin
  - Vout
  - RL

**Fig. SI-01**

- **Put substrate connections as close to the noise source as possible**
- **"AC ground"**

---

Hot Carrier Injection in CMOS Technology with an Epitaxial Region

![Diagram of Noisy and Quiet Circuits]

- **Noisy Circuits**: 
  - Digital Ground
  - VDD
  - Vin
  - Vout
  - n+ channel stop (1 Ω-cm)
  - p+ substrate (0.05 Ω-cm)

- **Quiet Circuits**: 
  - Analog Ground
  - VDD (Analog)
  - Vin
  - Vout
  - RL

**Fig. SI-02**

- **Put substrate connections as close to the noise source as possible**
- **"AC ground"**
- **Reduced back-gating due to smaller resistance**
- **p+ epitaxial layer (15 Ω-cm)**
Computer Model for Substrate Interference Using SPICE Primitives

Noise Injection Model:

![Noise Injection Diagram](image1)

Noise Detection Model:

![Noise Detection Diagram](image2)
Other Sources of Substrate Injection

(We do it to ourselves and can’t blame the digital circuits.)

Also, there is coupling from power supplies and clock lines to other adjacent signal lines.

Summary of Substrate Interference

- Methods to reduce substrate noise
  1.) Physical separation
  2.) Guard rings placed close to the sensitive circuits with dedicated package pins.
  3.) Reduce the inductance in power supply and ground leads (best method)
  4.) Connect regions of constant potential (wells and substrate) to metal with as many contacts as possible.

- Noise Insensitive Circuit Design Techniques
  1.) Design for a high power supply rejection ratio (PSRR)
  2.) Use multiple devices spatially distinct and average the signal and noise.
  3.) Use “quiet” digital logic (power supply current remains constant)
  4.) Use differential signal processing techniques.

- Some references
SECTION 3.5 – MATCHING OF COMPONENTS

INTRODUCTION

What is Accuracy and Matching?

The accuracy of a quantity specifies the difference between the actual value of the quantity and the ideal or true value of the quantity.

The mismatch between two quantities is the difference between the actual ratio of the quantities and the desired ratio of the two quantities.

Example:

\[ x_1 = \text{actual value of one quantity} \]
\[ x_2 = \text{actual value of a second quantity} \]
\[ X_1 = \text{desired value of the first quantity} \]
\[ X_2 = \text{desired value of the second quantity} \]

The accuracy of a quantity can be expressed as,

\[ \text{Accuracy} = \frac{x - X}{X} = \frac{\Delta X}{X} \]

The mismatch, \( \delta \), can be expressed as,

\[ \delta = \frac{x_2}{x_1} \frac{X_2}{X_1} - 1 \]

Relationship between Accuracy and Matching

Let:

\[ \Delta X_1 = |x_1 - X_1| \quad \Rightarrow \quad x_1 = X_1 \pm \Delta X_1 \]

and

\[ \Delta X_2 = |x_2 - X_2| \quad \Rightarrow \quad x_2 = X_2 \pm \Delta X_2 \]

Therefore, the mismatch can be expressed as,

\[ \delta = \frac{X_1(x_2 \pm \Delta X_2)}{X_2(x_1 \pm \Delta X_1)} - 1 = \frac{1 \pm \frac{\Delta X_2}{X_1}}{1 \pm \frac{\Delta X_1}{X_2}} - 1 \]

\[ \delta \approx 1 \pm \frac{\Delta X_2}{X_2} \frac{\Delta X_1}{X_1} - 1 \]

Thus, the mismatch is approximately equal to the difference in the accuracies of \( x_1 \) and \( x_2 \) assuming the deviations (\( \Delta X \)) are small with respect to \( X \).
Characterization of the Mismatch

Mean of the mismatch for $N$ samples-

$$m_\delta = \frac{1}{N} \sum_{i=1}^{N} \delta_i$$

Standard deviation of the mismatch for $N$ samples-

$$s_\delta = \sqrt{\frac{1}{N-1} \sum_{i=1}^{N} (\delta_i - m_\delta)^2}$$

$$m_\delta = \frac{253}{40} = 6.325 \quad s_\delta = 2.115$$

Motivation for Matching of Components

The accuracy of analog signal processing is determined by the accuracy of gains and time constants. These accuracies are dependent upon:

Gain $\propto$ Ratios of components or areas

Time constants $\propto$ Products of components or areas

Ratio Accuracy?

$$\text{Actual Ratio} = \frac{X_1 \pm \Delta X_1}{X_2 \pm \Delta X_2} = \frac{X_1}{X_2} \left( 1 \pm \frac{\Delta X_1}{X_1} \right) \left( 1 \pm \frac{\Delta X_2}{X_2} \right) \approx \frac{X_1}{X_2} \left( 1 \pm \frac{\Delta X_1}{X_1} \frac{\Delta X_2}{X_2} \right)$$

If $X_1$ and $X_2$ match ($\Delta X_1/X_1 \approx \Delta X_2/X_2$), then the actual ratio becomes the ideal ratio.

Product Accuracy?

$$\text{Product accuracy} = (X_1 \pm \Delta X_1)(X_2 \pm \Delta X_2) = X_1 X_2 \left( 1 \pm \frac{\Delta X_1}{X_1} \right) \left( 1 \pm \frac{\Delta X_2}{X_2} \right) \approx X_1 X_2 \left( 1 \pm \frac{\Delta X_1}{X_1} \frac{\Delta X_2}{X_2} \right)$$

Unfortunately, the product cannot be accurately maintained in integrated circuits.
Switched Capacitor Circuits

Switched capacitor circuits offer a solution to the product accuracy problem. A switched capacitor replacement of a resistor:

\[
R_1 = \frac{T_c}{C_1} \quad \text{and} \quad C_2
\]

The product of a resistor, \( R_1 \), and a capacitor, \( C_2 \), now become,

\[
R_1 C_2 = \left( \frac{T_c}{C_1} \right) C_2 = \frac{1}{f_c C_1} C_2 = \frac{C_2}{f_c C_1}
\]

The accuracy of the time constant (product) now becomes,

\[
\frac{C_2}{f_c C_1} \left( 1 \pm \frac{\Delta C_2}{C_2} + \frac{\Delta C_1}{C_1} + \frac{\Delta f_c}{f_c} \right)
\]

Assuming the clock frequency is accurate and larger than the signal bandwidth, then time constants in analog signal processing can be accurately matched by ratios of elements.

Types of Mismatches

1.) Those controlled or influenced by electrical design
   - Transistor operation
   - Circuit techniques
   - Correction/calibration techniques

2.) Those controlled or influenced by physical design
   - Random statistical fluctuations (microscopic fluctuations and irregularities)
   - Process bias (geometric variations)
   - Pattern shift (misalignment)
   - Diffusion interactions
   - Stress gradients and package shifts
   - Temperature gradients and thermoelectrics
   - Electrostatic interactions
ELECTRICAL MATCHING

Matching Principle

Assume that two transistors are matched (large signal model parameters are equal). Then if all terminal voltages of one transistor are equal to the terminal voltages of the other transistor, then the terminal currents will be matched.

Note that the terminals may be physically connected together or at the same potential but not physically connected together.

Examples of the Matching Principle

Cascode current mirror:

The key transistors are M1 and M2. The gates and sources are physically connected and the drains are equal due to M3 and M4 gate-source drops. As a result, \( I_{D1} \) will be very close to \( I_{D2} \).

Differential amplifier:

When \( I_{D1} \) and \( I_{D2} \) are equal, the fact that the drains of M1 and M2 are equal should give the smallest value of the input offset voltage, \( V_{io} \).

Note: Since the drain voltages of M3 and M4 in both circuits are not necessarily equal, the gate-source voltages of M3 and M4 are not exactly equal which cause the drain voltages of M1 and M2 to not be exactly equal.
Gate-Source Matching

Not as precise as the previous principle but useful for biasing applications.

A. If the gate-source voltages of two or more FETs are equal and the FETs are matched and operating in the saturation region, then the currents are related by the W/L ratios of the individual FETs. The gate-source voltages may be directly or indirectly connected.

\[
i_{D1} = \frac{K'W_1}{2L_1} (v_{GS1} - V_T)^2 \quad \rightarrow \quad (v_{GS1} - V_T)^2 = \frac{2K'i_{D1}}{(W_1/L_1)}
\]

\[
i_{D2} = \frac{K'W_2}{2L_2} (v_{GS2} - V_T)^2 \quad \rightarrow \quad (v_{GS2} - V_T)^2 = \frac{2K'i_{D2}}{(W_2/L_2)}
\]

If \(v_{GS1} = v_{GS2}\), then \(i_{D1} = \frac{W_2}{L_2} i_{D1} = \frac{W_1}{L_1} i_{D2}\) or \(i_{D1} \equiv \frac{W_1}{W_2} \frac{L_2}{L_1} i_{D2}\)

B. If the drain currents of two or more transistors are equal and the transistors are matched and operating in the saturation region, then the gate-source voltages are related by the W/L ratios (ignoring bulk effects).

If \(i_{D1} = i_{D2}\), then

\[
v_{GS1} = V_T + \sqrt{\frac{W_2}{L_2} (v_{GS2} - V_T)} \quad \text{or} \quad v_{GS1} = v_{GS2} \text{ if } \frac{W_2}{L_2} = \frac{W_1}{L_1}
\]

Process Independent Biasing - MOSFET

The sensitivity of the bias points of all transistors depend on both the variation of the technological parameters and the accuracy of the biasing circuits.

Gate-source voltage decomposition:

The gate-source voltage of the MOSFET can be divided into two parts:

1.) The part necessary to form or enhance the channel, \(V_T\)

2.) The part necessary to cause current to flow, \(V_{GS} - V_T = V_{ON}\), called the overdrive.

This overdrive can be expressed,

\[
V_{ON} = V_{DS}(sat) = \sqrt{\frac{2I_D}{K'(W/L)}}
\]

The dependence of the bias point on the technology, \(V_T\), can be reduced by making \(V_{ON} = V_{DS}(sat) >> V_T\).

This implies that small values of \(W/L\) are preferable. Unfortunately, this causes the transconductance to reduce if the current remains the same.
**Doubly Correlated Sampling**
Illustration of the use of chopper stabilization to remove the undesired signal, $v_u$, from the desired signal, $v_{in}$. In this case, the undesired signal is the gate leakage current.

![Diagram of Doubly Correlated Sampling](image)

- Chopping with 50% duty cycle
- All switches use thick oxide devices to reduce gate leakage
- Gain $\approx g_m(r_{ds2}\|r_{ds4})g_mR_2$

Will examine further in low noise op amps.
Self-Calibration Techniques

The objective of self-calibration is to increase the matching between two or more components (generally passive).

The requirements for self-calibration:
1.) A time interval in which to perform the calibration
2.) A means of adjusting the value of one or more of the components.

Self-calibration can typically improve the matching by a factor of 2-3 bits (4-8).

Example of Capacitor Self-Calibration

Consider the charge amplifier below that should have a gain of unity.

Assume the amplifier has a DC input offset voltage of $V_{io}$. The following shows how to calibrate one (or both) of the capacitors.

In the calibration phase, $v_x$, is:

$$v_x = (V_{REF} - V_{io}) \left( \frac{C_2}{C_1 + C_2} \right) - (V_{REF} - V_{io}) \left( \frac{C_1}{C_1 + C_2} \right) = (V_{REF} - V_{io}) \left( \frac{C_2 - C_1}{C_1 + C_2} \right)$$

The correction circuitry varies $C_1$ or $C_2$ until $v_x = 0$ as observed by $v_{OUT}$. 
Variable Components

The correction circuitry should be controlled by logic circuits so that the correction can be placed into memory to maintain the calibration of the circuit during application.

Implementation for $C_1$ and $C_2$ of the previous example:

$$C_1 \left\{ \frac{1}{2^K}, \frac{1}{2^{K+1}}, \ldots, \frac{1}{2^N} \right\}$$

$$C_2 \left\{ \frac{1}{2^K}, \frac{1}{2^{K+1}}, \ldots, \frac{1}{2^N} \right\}$$

$K$ is selected to achieve the desired tolerance or variation

$N$ is selected to achieve the desired resolution ($N > K$)

Additional circuitry:

Every self-calibration system will need additional logic circuits to sense when the value of $v_x$ changes from positive to negative (or vice versa) and to store the switch settings in memory to maintain the calibration.

Basics of Dynamic Element Matching

Dynamic element matching chooses different, approximately equal-valued elements to represent a more precise value of a component as a function of time.

Goal of dynamic element matching:

Convert the error due to element mismatch from a dc offset into an ac signal of equivalent power which can be removed by the appropriate means (doubly-correlated sampling, highpass filtering of a sigma-delta modulator, etc.)

---


CMOS Analog Circuit Design © P.E. Allen - 2006
**How Dynamic Element Matching Works**

Assume that we have three approximately equal elements with the following currents:

- Element 1 = 0.99 mA
- Element 2 = 1.03 mA
- Element 3 = 0.98 mA

**Ideal current output level**

![Ideal Current (mA)](image)

**Error when dynamic element matching is not used**

![Error when dynamic element matching is not used](image)

**Error when dynamic element matching is used**

![Error when dynamic element matching is used](image)

**Issues of Dynamic Element Matching**

- The selection of the elements must be truly random for the maximum benefit to occur.
- If the number of elements is large this can be an overwhelming task to implement. An approximation to random selection is the butterfly-type randomizer below:

![Three-stage, eight-line butterfly randomizer](image)

- When using the dynamic element technique, one needs to be careful that the averaging activity of the dynamic element matching process does not interfere with other averaging processes that might be occurring simultaneously (i.e. Σ∆ modulators).

**Other references:**


PHYSICAL MATCHING

Review of Physical Matching
We have examined these topics in the previous chapter. To summarize, the sources of physical mismatch are:

- Random statistical fluctuations (microscopic fluctuations and irregularities)
- Process bias (geometric variations)
- Pattern shift (misalignment)
- Diffusion interactions
- Stress gradients and package shifts
- Temperature gradients and thermoelectrics
- Electrostatic interactions

Rules for Resistor Matching†

1.) Construct matched resistors from the same material.
2.) Make matched resistors the same width.
3.) Make matched resistors sufficiently wide.
4.) Where practical, use identical geometries for resistors (replication principle)
5.) Orient resistors in the same direction.
6.) Place matched resistors in close physical proximity.
7.) Interdigitate arrayed resistors.
8.) Place dummy resistors on either end of a resistor array.
9.) Avoid short resistor segments.
10.) Connect matched resistors in order to cancel thermoelectrics.
11.) If possible place matched resistors in a low stress area (minimize piezoresistance).
12.) Place matched resistors well away from power devices.
13.) Place precisely matched resistors on the axes of symmetry of the die.

Rules for Resistor Matching – Continued

14.) Consider the influence of tank modulation for HSR resistors (the voltage modulation of the reverse-biased depletion region changes the sheet resistivity).

15.) Sectioned resistors are superior to serpentine resistors.

16.) Use poly resistors in preference to diffused resistors.

17.) Do not allow the buried layer shadow to intersect matched diffused resistors.

18.) Use electrostatic shielding where necessary.

19.) Do not route unconnected metal over matched resistors.

20.) Avoid excessive power dissipation in matched resistors.

Rules for Capacitor Matching†

1.) Use identical geometries for matched capacitors (replication principle).

2.) Use square or octagonal geometries for precisely matched capacitors.

3.) Make matched capacitors as large as possible.

4.) Place matched capacitors adjacent to one another.

5.) Place matched capacitors over field oxide.

6.) Connect the upper electrode of a matched capacitor to the higher-impedance node.

7.) Place dummy capacitors around the outer edge of the array.

8.) Electrostatically shield matched capacitors.

9.) Cross-couple arrayed matched capacitors.

10.) Account for the influence of the leads connecting to matched capacitors.

11.) Do not run leads over matched capacitors unless they are electrostatically shielded.

12.) Use thick-oxide dielectrics in preference to thin-oxide or composite dielectrics.

13.) If possible, place matched capacitors in areas of low stress gradients.

14.) Place matched capacitors well away from power devices.

15.) Place precisely matched capacitors on the axes of symmetry for the die.

Mismatched Transistors

Assume two transistors have \( v_{DS1} = v_{DS2}, \) \( K'_1 \neq K'_2 \) and \( V_{T1} \neq V_{T2}. \) Therefore we have
\[
\frac{i_O}{I} = \frac{K'_2}{K'_1} \frac{(v_{GS} - V_{T2})^2}{(v_{GS} - V_{T1})^2}
\]

How do you analyze the mismatch? Use plus and minus worst case approach. Define
\[
\Delta K' = K'_2 - K'_1 \quad \text{and} \quad K' = 0.5(K'_2 + K'_1) \quad \Rightarrow \quad K'_1 = K' - 0.5\Delta K' \quad \text{and} \quad K'_2 = K' + 0.5\Delta K'
\]
\[
\Delta V_T = V_{T2} - V_{T1} \quad \text{and} \quad V_T = 0.5(V_{T1} + V_{T2}) \quad \Rightarrow \quad V_{T1} = V_T - 0.5\Delta V_T \quad \text{and} \quad V_{T2} = V_T + 0.5\Delta V_T
\]
Substituting these terms into the above equation gives,
\[
\frac{i_O}{I} = \left(\frac{K' + 0.5\Delta K'}{K' - 0.5\Delta K'}\right) \frac{(v_{GS} - V_T - 0.5\Delta V_T)^2}{(v_{GS} - V_T + 0.5\Delta V_T)^2} = \left(1 + \frac{\Delta K'}{2K'}\right) \frac{1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}}{1 + \frac{\Delta V_T}{2(v_{GS} - V_T)}}
\]
Assuming that the terms added to or subtracted from “1” are smaller than unity gives
\[
\frac{i_O}{I} \approx \left(1 + \frac{\Delta K'}{2K'}\right) \left(1 + \frac{\Delta K'}{2K'}\right) \frac{1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}}{1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}} \approx 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS} - V_T)}
\]
If \( \Delta K'/K' = \pm 5\% \) and \( \Delta V_T/(v_{GS} - V_T) = \pm 10\% \), then \( i_O/I \approx 1 \pm 0.05 \pm (-0.20) = 1 \pm (0.25) \)

Geometric Effects

How does the size and shape of the transistor effect its matching?

Gate Area:
\[
\sigma_{V_{th}} = \frac{C_{Vth}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{Kp} = K' \frac{C_{Kp}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{AW/W} = \frac{C_{AW/W}}{\sqrt{W_{eff}L_{eff}}}
\]
where \( C_{Vth}, C_{Kp} \) and \( C_{AW/W} \) are constants determined by measurement.

Values from a 0.35\( \mu m \) CMOS technology:
\[
\sigma_{V_{th,NMOS}} = \frac{10.6mV \cdot \mu m}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{V_{th,PMOS}} = \frac{8.25mV \cdot \mu m}{\sqrt{W_{eff}L_{eff}}}
\]
and
\[
\sigma_{\frac{\Delta W}{W}}_{NMOS} = \frac{0.0056 \cdot \mu m}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{\frac{\Delta W}{W}}_{PMOS} = \frac{0.0011 \cdot \mu m}{\sqrt{W_{eff}L_{eff}}}
\]
The above results suggest that PMOS devices would be better matched than NMOS devices in this technology.
Rules for Transistor Matching†

1.) Use identical finger geometries.
2.) Use large active areas.
3.) For voltage matching, keep $V_{GS} - V_T$, small (i.e. 0.1V).
4.) For current matching, keep $V_{GS} - V_T$, large (i.e. 0.5V).
5.) Orient the transistors in the same direction.
6.) Place the transistors in close proximity to each other.
7.) Keep the layout of the matched transistors as compact as possible.
8.) Where practical use common centroid geometry layouts.
9.) Place dummy segments on the ends of arrayed transistors.
10.) Avoid using very short or narrow transistors.
11.) Place transistors in areas of low stress gradients.
12.) Do not place contacts on top of active gate area.
13.) Keep junctions of deep diffusions as far away from the active gate area as possible.
14.) Do not route metal across the active gate region.
15.) Place precisely matched transistors on the axes of symmetry of the die.
16.) Do not allow the buried layer shadow to intersect the active gate area.
17.) Connect gate fingers using metal connections.

† Alan Hastings, Art of Analog Layout, 2nd ed, 2006, Pearson Prentice Hall, New Jersey

SECTION 3.6 – COMPUTER MODELS

FET Model Generations

• First Generation – Physically based analytical model including all geometry dependence.
• Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
• Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

Performance Comparison of Models (from Cheng and Hu, MOSFET Modeling & BSIM3 Users Guide)

<table>
<thead>
<tr>
<th>Model</th>
<th>Minimum L (μm)</th>
<th>Minimum Tox (nm)</th>
<th>Model Continuity</th>
<th>iD Accuracy in Strong Inversion</th>
<th>iD Accuracy in Subthreshold</th>
<th>Small signal parameter</th>
<th>Scalability</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS1</td>
<td>5</td>
<td>50</td>
<td>Poor</td>
<td>Poor</td>
<td>Not Modeled</td>
<td>Poor</td>
<td>Poor</td>
</tr>
<tr>
<td>MOS2</td>
<td>2</td>
<td>25</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>MOS3</td>
<td>1</td>
<td>20</td>
<td>Poor</td>
<td>Fair</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
</tr>
<tr>
<td>BSIM1</td>
<td>0.8</td>
<td>15</td>
<td>Fair</td>
<td>Good</td>
<td>Fair</td>
<td>Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>BSIM2</td>
<td>0.35</td>
<td>7.5</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
<td>Fair</td>
</tr>
<tr>
<td>BSIM3v2</td>
<td>0.25</td>
<td>5</td>
<td>Fair</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>BSIM3v3</td>
<td>0.15</td>
<td>4</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
</tbody>
</table>
First Generation Models

Level 1 (MOS1)
- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift).

Level 2 (MOS2)
- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a “developing ground” for better modeling techniques.

Level 3 (MOS3)
- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.

Second Generation Models

BSIM (Berkeley Short-Channel IGFET Model)
- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
-Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28
- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2
- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design
**Third Generation Models**

**BSIM2 – Continued**
- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature

**BSIM3**
- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

**MOS Model 9**
- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

**Other Candidates**
- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design

---

**BSIM2 Model**

Generic composite expression for the model parameters:

\[ X = X_0 + \frac{LX}{L_{\text{eff}}} + \frac{WX}{W_{\text{eff}}} \]

where
- \( X_0 \) = parameter for a given W and L
- \( LX \) (\( WX \)) = first-order dependence of X on L (W)

Modeling features of BSIM2:

**Mobility**
- Mobility reduction by the vertical and the lateral field

**Drain Current**
- Velocity saturation
- Linear region drain current
- Saturation region drain current
- Subthreshold current

\[ i_{DS} = \frac{\mu_o C_{ox} W_{\text{eff}}}{L_{\text{eff}}} \left( \frac{kT}{q} \right) e^{\frac{V_{GS} - V_{t} - V_{off}}{n}} \left[ 1 - e^{qV_{DS}/kT} \right] \]

where
- \( V_{off} = V_{OF} + V_{OFB} \cdot v_{BS} + V_{OFD} \cdot v_{DS} \) and \( n = NO + \frac{NB}{\sqrt{\phi - v_{BS}}} + ND \cdot v_{DS} \)
**BSIM2 Output Conductance Model**

- Drain-Induced Barrier Lowering (DIBL) – Lowering of the potential barrier at the source-bulk junction allowing carriers to traverse the channel at a lower gate bias than would otherwise be expected.
- Substrate Current-Induced Body Effect (SCBE) – The high field near the drain accelerates carriers to high energies resulting in impact ionization which generates a hole-electron pair (hot carrier generation). The opposite carriers are swept into the substrate and have the effect of slightly forward-biasing the source-substrate junction. This reduces the threshold voltage and increases the drain current.

**Charge Model**
- Eliminates the partitioning choice (50%/50% is used)
- BSIM charge model better documented with more options

**BSIM2 Basic Parameter Extraction**
- A number of devices with different W/L are fabricated and measured

- A long, wide device is used as the base to add geometry effects as corrections.
- Procedure:
  1.) Oxide thickness and the differences between the drawn and effective channel dimensions are provided as process input.
  2.) A long, wide device is used to determine some base parameters which are used as the starting point for each individual device extraction in the second phase.
  3.) In the second phase, a set of parameters is extracted independently for each device. This phase represents the fitting of the data for each independent device to the intrinsic equation structure of the model.
  4.) In the third phase, the compiled parameters from the second phase are used to determine the geometry parameters. This represents the imposition of the extrinsic structure onto the model.
BSIM2 Model used in Subthreshold

BSIM Model Parameters used in Subthreshold
VDS 1 0 DC 3.0
M1 1 0 0 CMOSN W=5UM L=2UM
.MODEL CMOSN NMOS LEVEL=4
+VFB=-7.9262E-01 LVFB= 1.2297E-02 WFB=1.0023E-01
+PHI=7.5909E-01 LPHI= 0.0000E+00 WPHI= 0.00000E+00
+K1= 1.0670E+00 LK1= 5.0843E-02 WK1= 6.7697E-02
+K2= 4.2366E-03 LK2= 6.7697E-02 WK2= 6.2741E-02
+ETA= -4.3579E-03 LETA= 9.0518E-03 WETA= 7.3315E-03
+U0= 5.58459E+02 DL= 6.86137E-01 DW= 1.04701E-01
+U0= 5.58459E+02 DL= 6.86137E-01 DW= 1.04701E-01
+U1= 5.38133E-03 LU1= 5.43387E-01 WU1= 8.63357E-02
+X2MZ= 1.45214E+01 LX2MZ= 3.08694E+01 WX2MZ= 4.75033E+01
+X2E= -1.67104E-04 LX2E= -4.7532E-03 WX2E= -2.7484E-03
+X3E= 5.33407E-04 LX3E= -4.69455E-04 WX3E= -8.63357E-02
+X2U0= 2.45655E-03 LX2U0= 1.46188E-02 WX2U0= 2.63555E-02
+X2U1= 3.80979E-04 LX2U1= -1.71488E-03 WX2U1= 2.3520E-02
+MUS= 5.48735E+02 LMUS= 3.28720E+02 WMUS= 1.3536E+02
+X2MS= -6.72261E+00 LX2MS= -3.48094E+01 WX2MS= 9.84809E+01
+X3MS= -2.79427E+00 LX3MS= 6.31555E+01 WX3MS= -1.3536E+02
+X3U1= 1.74888E-03 LX3U1= 6.13936E-02 WX3U1= 3.49351E-03
+TOX= 4.03000E-00 TEMP= 2.70000E+01 VDD= 5.00000E+00
+CGDO= 4.40942E-01 CGSO= 4.40942E-01 CGBO= 6.34142E-01
+XPART= -1.00000E+00
+N0=1.00000E+00 LW=0.00000E+00 WN=0.00000E+00
+NB=0.00000E+00 LNB=0.00000E+00 WNB=0.00000E+00
+ND=0.00000E+00 LND=0.00000E+00 WND=0.00000E+00
+RSH=0 C=6.14150E-04 CJSW=6.17440E-10 JS=0 PB=0.8
+PBSW=0.8 MJ=5.4726 MJMS=0.3597 WDF=0 DELL=0
.DC VDS 0 0.01
.PRINT DC ID(M1)
.PROBE
.END

Results of the BSIM2 Model Simulation in Subthreshold

![Graph showing the relationship between VGS and ID(M1)](image_url)
BSIM3 Model

The short channel effects included in the BSIM3 model are:
- Normal and reverse short-channel and narrow-width effects on the threshold.
- Channel length modulation (CLM).
- Drain induced barrier lowering (DIBL).
- Velocity saturation.
- Mobility degradation due to the vertical electric field.
- Impact ionization.
- Band-to-band tunnelling.
- Velocity overshoot.
- Self-heating.
1.) Channel quantization.
2.) Polysilicon depletion.

CMOS Analog Circuit Design © P.E. Allen - 2006

BSIM3v3 Model Equations for Hand Calculations
In strong inversion, approximate hand equations are:

\[ i_{DS} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \left( 1 + \frac{1}{E_{sat} L_{eff}} \right) \left( v_{GS} - V_{th} - \frac{A_{bulk} V_{DS}}{2} \right) V_{DS} , \quad V_{DS} < V_{DS(sat)} \]

\[ i_{DS} = W_{eff} v_{sat} C_{ox} \left( v_{GS} - V_{th} - A_{bulk} V_{DS(sat)} \right) \left( 1 + \frac{V_{DS} - V_{DS(sat)}}{V_{A}} \right) , \quad V_{DS} > V_{DS(sat)} \]

where

\[ V_{DS(sat)} = \frac{E_{sat} L_{eff} (v_{GS} - V_{th})}{A_{bulk} E_{sat} L_{eff} + (v_{GS} - V_{th})} \]

\[ L_{eff} = L_{drawn} - 2dL \]

\[ W_{eff} = W_{drawn} - 2dW \]

\[ E_{sat} = \text{Electric field where the drift velocity (v) saturates} \]

\[ v_{sat} = \text{saturation velocity of carriers in the channel} \]

\[ \mu = \frac{\mu_{eff}}{1 + (E/E_{sat})} \quad \Rightarrow \quad \mu_{eff} = \frac{2v_{sat}}{E_{sat}} \]

Note: Assume \( A_{bulk} \approx 1 \) and extract \( V_{th} \) and \( V_{A} \).
MOSIS Parametric Test Results

http://www.mosis.org/

RUN: T02D  VENDOR: TSMC
TECHNOLOGY: SCN025  FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 0251P5M.

TRANSISTOR PARAMETERS  W/L  N-CHANNEL  P-CHANNEL  UNITS
MINIMUM  0.36/0.24  0.54  -0.50  volts
SHORT  20.0/0.24  557  -256  uA/um
Vth  0.56  -0.56  volts
Vpt  7.6  -7.2  volts
WIDE  20.0/0.24  6.6  -1.5  pA/um
Id0  20.0/0.24  0.47  -0.60  volts
Vth  5.8  -7.2  volts
Vjbd  -25.0  -1.1  pA
Gamma  0.44  0.61  V 0.5
K’ (Uo*Cox/2)  112.0  -23.0  uA/V^2

0.25μm BSIM3v3.1 NMOS Parameters

.MODEL CMOSN NMOS (  LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 5.7E-9
+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.4273342
+K1 = 0.3922983 K2 = 0.0185825 K3 = 1E-3
+K3B = 2.0947677 W0 = 2.171779E-7 NLX = 1.919758E-7
+DVTOW = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 7.137212E-3 DVT1 = 6.664687E-3 DVT2 = -0.3025397
+U0 = 403.1776038 W0 = -3.60743E-12 UB = 1.323051E-18
+UC = 2.575123E-11 VSAT = 1.616298E5 A0 = 1.4626549
+AGS = 0.3136349 B0 = 3.080869E-8 B1 = -1E-7
+KETA = 5.462411E-3 A1 = 4.653219E-4 A2 = 0.6191129
+RDSW = 345.624986 PRWG = 0.3183394 PRWB = -0.1441065
+WR = 1 WINT = 8.107812E-9 LINT = 3.375532E-9
+XL = 3E-8 XW = 0 DWG = 6.420502E-10
+DWB = 1.042904E-8 VOFF = -0.1083577 NFACTOR = 1.1884386
+CI = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 4.914545E-3 ETAB = 4.215338E-4
+DSUB = 0.0313287 PCLM = 1.2088426 PDIBLC1 = 0.7240447
+PDIBLC2 = 5.120303E-3 PDIBLCB = -0.0443076 DROUT = 0.7752992
+PSCBE1 = 4.451333E8 PSCBE2 = 5E-10 PVAG = 0.2068286
+DELTA = 0.01 MOBMOD = 1 PRT = 0
+UTE = -1.5 KT1 = -0.11 KTL1 = 0
+K2 = 0.22 UA1 = 4.31E-9 UB1 = 1.66E-18
+UC1 = 1.66E-11 AT = 3.3E4 WL = 0
+WLN = 1 WW = 1.212182E-16 WNW = 1.2127
+WL = 0 LL = 0 LNL = 1
+LW = 0 LWN = 1 LWL = 0
+CAPMOD = 2 XPART = 0.4 CGDO = 6.33E-10
+CGSO = 6.33E-10 CGBO = 1E-11 CJ = 1.766171E-3
+PB = 0.9577677 MJ = 0.4579102 CSW = 3.931544E-10
+PBSW = 0.99 MJSW = 0.2722644 CF = 0
+PVTH0 = 2.125456E-3 PRDSW = 24.2435379 PK2 = 4.788904E-4
+WKETA = 1.430792E-3 LKETA = -6.548592E-3 )
### 0.25μm BSIM3v3.1 PMOS Parameters

```plaintext
MODEL CMOSP PMOS (LEVEL = 49
+VERSION = 3.1 TNO = 27 TOX = 5.7E-9
+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.6193382
+K1 = 0.5275326 K2 = 0.0281819 K3 = 0
+K3B = 11.249555 W0 = 1E-6 NLX = 1E-9
+DVTOW = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 3.1920483 DVT1 = 0.4901788 DVT2 = -0.0295257
+U0 = 185.1288894 UA = 3.40616E-9 UB = 3.640498E-20
+UC = -6.35238E-11 VSAT = 1.975064E5 A0 = 0.4156696
+AGS = 0.070036 B0 = 3.11154E-8 B1 = 5E-6
+KETA = 0.0253118 A1 = 2.42104E-4 A2 = 0.6754231
+RDSW = 866.896668 PRWG = 0.0362726 PRWB = -0.293946
+WR = 1 WINT = 6.519911E-9 LINT = 2.210804E-8
+XL = 3E-8 XW = 0 DWG = -2.423118E-8
+DWB = 3.052612E-8 VOFF = -0.1161062 NFACTOR = 1.2546896
+MIX = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.7241245 ETAB = -0.3675267
+DSUB = 1.1734643 PCLM = 1.0837457 PDIBLC1 = 9.608442E-4
+PDIBLC2 = 0.0176785 PDIBLCB = -9.605935E-4 DROUT = 0.0735541
+PSBIE1 = 1.579442E10 PSCBE2 = 6.707105E-9 PVAG = 0.0490261
+DELTA = 0.01 MOBMOD = 1 PRT = 0
+UTE = -1.5 KT1 = -0.11 KTIL = 0
+KT2 = 0.022 UA1 = 4.31E-9 UB1 = -7.61E-18
+UC1 = -5.6E-11 AT = 3.3E4 WL = 0
+WLN = 1 WW = 0 WWN = 1
+WAL = 0 LL = 0 LLN = 1
+LWL = 0 LWN = 1 LWL = 0
+CAPMOD = 2 XPART = 0.4 CGDO = 5.11E-10
+CQSO = 5.11E-10 CGBO = 1E-11 CJ = 1.882953E-3
+PB = 0.99 MJ = 0.4690946 CISW = 3.018356E-10
+PRSW = 0.8137064 MISW = 0.3299497 CF = 0
+PVTH0 = 5.268963E-5 PRDSW = -2.2622317 PK2 = 3.952008E-3
+WKETA = -7.69819E-3 LKETA = -0.0119828 )
```

### Summary of MOSFET Models for Simulation

- Models are much improved for efficient computer simulation
- Output conductance model is greatly improved
- Poor results for narrow channel transistors
- Can have discontinuities at bin boundaries
- Fairly complex model, difficult to understand in detail
SECTION 3.7 – EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

Procedure for extracting short channel models:

1.) Extract the square-law model parameters for a transistor with length at least 10 times $L_{\text{min}}$.

2.) Using the values of $K'$, $V_T$, $\lambda$, and $\gamma$ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

Adjust the values of $K'$, $V_T$, and $\lambda$ as needed.

Illustration of the Extraction Procedure

Choose $L$

Extract $V_{TO}$, $K'$, $\lambda$, $\gamma$ and $\phi$ using the simulator for the simple model

Use the appropriate optimization routine to find $\theta$ and the new values for $V_{TO}$, $K'$, $\lambda$, $\gamma$ and for the model

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$
EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

\[
\begin{align*}
i_D &= K \left( \frac{W}{2L} \right) (v_{GS} - V_T)^2(1 + \lambda v_{DS}) \quad (1) \\
i_D &= K \left( \frac{W}{L} \right) \left[ (v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS}) \quad (2)
\end{align*}
\]

where

\[
V_T = V_{T0} + \gamma \left[ \sqrt{2|\phi|} + v_{SB} - \sqrt{2|\phi|} \right] \quad (3)
\]

Extraction of Model Parameters:

First assume that \(v_{DS}\) is chosen such that the \(\lambda v_{DS}\) term in Eq. (1) is much less than one and \(v_{SB}\) is zero, so that \(V_T = V_{T0}\).

Therefore, Eq. (1) simplifies to

\[
i_D = K' \frac{W_{eff}}{2L_{eff}} (v_{GS} - V_{T0})^2
\]

This equation can be manipulated algebraically to obtain the following

\[
i_D^{1/2} = \left( \frac{K' W_{eff}}{2L_{eff}} \right)^{1/2} v_{GS} = \left( \frac{K' W_{eff}}{2L_{eff}} \right)^{1/2} V_{T0}
\]

which has the form

\[
y = mx + b
\]

This equation is easily recognized as the equation for a straight line with \(m\) as the slope and \(b\) as the \(y\)-intercept. Comparing Eq. (5) to Eq. (6) gives

\[
y = i_D^{1/2}
\]

\[
x = v_{GS}
\]

\[
m = \left( \frac{K' W_{eff}}{2L_{eff}} \right)^{1/2}
\]

and

\[
b = -\left( \frac{K' W_{eff}}{2L_{eff}} \right)^{1/2} V_{T0}
\]
### Illustration of $K'$ and $V_T$ Extraction

![Graph showing extraction of $K'$ and $V_T$](image)

**Comments:**
- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than $L_{\text{min}}$

### Example 3.7-1 – Extraction of $K'$ and $V_T$ Using Linear Regression

Given the following transistor data shown in Table 3.7-1 and linear regression formulas based on the form,

$$y = mx + b$$

and

$$m = \frac{\sum x_i y_i - (\sum x_i \sum y_i)/n}{\sum x_i^2 - (\sum x_i)^2/n}$$

(11)

(12)

determine $V_{T0}$ and $K'W/2L$. The data in Table 3.7-1 also give $I_D^{1/2}$ as a function of $V_{GS}$.

**Table 3.7-1 Data for Example 3.7-1**

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$I_D$ (μA)</th>
<th>$\sqrt{I_D}$ (μA)$^{1/2}$</th>
<th>$V_{SB}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000</td>
<td>0.700</td>
<td>0.837</td>
<td>0.000</td>
</tr>
<tr>
<td>1.200</td>
<td>2.00</td>
<td>1.414</td>
<td>0.000</td>
</tr>
<tr>
<td>1.500</td>
<td>8.00</td>
<td>2.828</td>
<td>0.000</td>
</tr>
<tr>
<td>1.700</td>
<td>13.95</td>
<td>3.735</td>
<td>0.000</td>
</tr>
<tr>
<td>1.900</td>
<td>22.1</td>
<td>4.701</td>
<td>0.000</td>
</tr>
</tbody>
</table>
**Example 3.7-1 – Continued**

**Solution**

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

\[
\text{Slope} = m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{ID_2} - \sqrt{ID_1}}{V_{GS2} - V_{GS1}}
\]

Gives

\[
m_1 = \frac{1.414 - 0.837}{0.2} = 2.885 \\
m_2 = \frac{2.828 - 1.414}{0.3} = 4.713 \\
m_3 = \frac{3.735 - 2.828}{0.2} = 4.535 \\
m_4 = \frac{4.701 - 3.735}{0.2} = 4.830
\]

These results indicate that the first (lowest value of \(V_{GS}\)) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

\[
V_{T0} = 0.898 \text{ V} \quad \text{and} \quad \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} = 21.92 \mu A/V^2
\]

---

**Extraction of the Bulk-Threshold Parameter \(\gamma\)**

Using the same techniques as before, the following equation

\[
V_T = V_{T0} + \gamma \left[ \sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|} \right]
\]

is written in the linear form where

\[
\begin{align*}
\gamma &= V_T \\
x &= \sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|} \\
m &= \gamma \\
b &= V_{T0}
\end{align*}
\]

The term \(2|\phi_F|\) is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for \(2|\phi_F|\).
2.) Extract a value for \(\gamma\).
3.) Calculate \(N_{\text{SUB}}\) using the relationship, \(\gamma = \frac{\sqrt{2|\phi_F|qN_{\text{SUB}}}}{C_{ox}}\)
4.) Calculate \(\phi_F\) using the relationship, \(\phi_F = -\frac{kT}{q} \ln \left( \frac{N_{\text{SUB}}}{n_i} \right)\)
5.) Iterative procedures can be used to achieve the desired accuracy of \(\gamma\) and \(2|\phi_F|\).

Generally, an approximate value for \(2|\phi_F|\) gives adequate results.
**Illustration of the Procedure for Extracting $\gamma$**

A plot of $\sqrt{i_D}$ versus $v_{GS}$ for different values of $v_{SB}$ used to determine $\gamma$ is shown below.

By plotting $V_T$ versus $x$ of Eq. (13) one can measure the slope of the best fit line from which the parameter $\gamma$ can be extracted. In order to do this, $V_T$ must be determined at various values of $v_{SB}$ using the technique previously described.

---

**Illustration of the Procedure for Extracting $\gamma$ - Continued**

Each $V_T$ determined above must be plotted against the $v_{SB}$ term. The result is shown below. The slope $m$, measured from the best fit line, is the parameter $\gamma$. 

---
Example 3.7-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. 3.7-1 and the following transistor data, determine the value of \( \gamma \) using linear regression techniques. Assume that \( 2|\phi_b| \) is 0.6 volts.

<table>
<thead>
<tr>
<th>( V_{SB} ) (V)</th>
<th>( V_{GS} ) (V)</th>
<th>( I_D ) (( \mu )A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.000</td>
<td>1.400</td>
<td>1.431</td>
</tr>
<tr>
<td>1.000</td>
<td>1.600</td>
<td>4.55</td>
</tr>
<tr>
<td>1.000</td>
<td>1.800</td>
<td>9.44</td>
</tr>
<tr>
<td>1.000</td>
<td>2.000</td>
<td>15.95</td>
</tr>
<tr>
<td>2.000</td>
<td>1.700</td>
<td>3.15</td>
</tr>
<tr>
<td>2.000</td>
<td>1.900</td>
<td>7.43</td>
</tr>
<tr>
<td>2.000</td>
<td>2.10</td>
<td>13.41</td>
</tr>
<tr>
<td>2.000</td>
<td>2.30</td>
<td>21.2</td>
</tr>
</tbody>
</table>

Solution

Table 3.7-2 shows data for \( V_{SB} = 1 \) volt and \( V_{SB} = 2 \) volts. A quick check of the data in this table reveals that \( \sqrt{I_D} \) versus \( V_{GS} \) is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. 3.7-1, the following thresholds are determined: \( V_{T_0} = 0.898 \) volts (from Ex. 3.7-1), \( V_T = 1.143 \) volts (@ \( V_{SB} = 1 \) V), and \( V_T = 1.322 \) V (@ \( V_{SB} = 2 \) V). Table 3.7-3 gives the value of \( V_T \) as a function of \( [(2|\phi_b| + V_{SB})^{1/2} - (2|\phi_b|)^{1/2}] \) for the three values of \( V_{SB} \).

Example 3.7-2 - Continued

| \( V_{SB} \) (V) | \( V_T \) (V) | \( [\sqrt{2|\phi_b| + V_{SB}} - \sqrt{2|\phi_b|}] \) (V\(^{1/2}\)) |
|----------------|---------------|---------------------------------------------------|
| 0.000          | 0.898         | 0.000                                             |
| 1.000          | 1.143         | 0.490                                             |
| 2.000          | 1.322         | 0.838                                             |

With these data, linear regression must be performed on the data of \( V_T \) versus \( [(2|\phi_b| + V_{SB})^{0.5} - (2|\phi_b|)^{0.5}] \). The regression parameters of Eq. (12) are

\[
\Sigma x_i y_i = 1.668 \\
\Sigma x_i y_i = 4.466 \\
\Sigma x_i^2 = 0.9423 \\
(\Sigma x_i)^2 = 1.764
\]

These values give \( m = 0.506 = \gamma \).
Extraction of the Channel Length Modulation Parameter, $\lambda$

The channel length modulation parameter $\lambda$ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (1) is rewritten as

$$i_D = i_D' = \lambda' v_{DS} + i_D'$$

which is in the familiar linear form where

$$y = i_D \quad (\text{Eq. (1)})$$

$$x = v_{DS}$$

$$m = \lambda i_D'$$

$$b = i_D' \quad (\text{Eq. (1) with } \lambda = 0)$$

By plotting $i_D$ versus $v_{DS}$, measuring the slope of the data in the saturation region, and dividing that value by the $y$-intercept, $\lambda$ can be determined. The procedure is illustrated in the figure shown.

Example 3.7-3 – Extraction of the Channel Length Modulation Parameter

Given the data of $I_D$ versus $V_{DS}$ in Table 3.7-4, determine the parameter $\lambda$.

Table 3.7-4 Data for Example 3.7-3.

<table>
<thead>
<tr>
<th>$I_D$ (μA)</th>
<th>39.2</th>
<th>68.2</th>
<th>86.8</th>
<th>94.2</th>
<th>95.7</th>
<th>97.2</th>
<th>98.8</th>
<th>100.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$ (V)</td>
<td>0.500</td>
<td>1.000</td>
<td>1.500</td>
<td>2.000</td>
<td>2.50</td>
<td>3.00</td>
<td>3.50</td>
<td>4.00</td>
</tr>
</tbody>
</table>

**Solution**

We note that the data of Table 3.7-4 covers both the saturation and nonsaturation regions of operation. A quick check shows that saturation is reached near $V_{DS} = 2.0 \text{ V}$. To calculate $\lambda$, we shall use the data for $V_{DS}$ greater than or equal to 2.5 V. The parameters of the linear regression are

$$x_i y_i = 1277.85 \quad \sum x_i y_i = 5096.00$$

$$\sum x_i^2 = 43.5 \quad (\sum x_i)^2 = 169$$

These values result in $m = \lambda I_D' = 3.08$ and $b = I_D' = 88$, giving $\lambda = 0.035 \text{ V}^{-1}$.

The slope in the saturation region is typically very small, making it necessary to be careful that two data points taken with low resolution are not subtracted (to obtain the slope) resulting in a number that is of the same order of magnitude as the resolution of the data point measured. If this occurs, then the value obtained will have significant and unacceptable error.
EXTRACTION OF THE SIMPLE MODEL FOR SHORT CHANNEL MOSFETS

Extraction for Short Channel MOSFETS

The model proposed is the following one which is the square-law model modified by the velocity saturation influence.

\[
i_D = \frac{K'}{2} \left[ 1 + \theta(v_{GS} - V_T) \right] \frac{W}{L} [v_{GS} - V_T]^2 (1 + \lambda v_{DS})\]

Using the values of \(K'\), \(V_T\), \(\lambda\), and \(\gamma\) extracted previously, use an appropriate extraction procedure to find the value of \(\theta\) adjusting the values of \(K'\), \(V_T\), and \(\lambda\) as needed.

Comments:

- We will assume that the bulk will be connected to the source or the standard relationship between \(V_T\) and \(V_{BS}\) can be used.
- The saturation voltage is still given by

\[
V_{DS}( \text{sat}) = V_{GS} - V_T
\]

Example of a Genetic Algorithm†

1.) To use this algorithm or any other, use the simulator and an appropriate short-channel model (BSIM3) to generate a set of data for the transconductance \(i_D\) vs. \(v_{GS}\) and output characteristics \(i_D\) vs. \(v_{DS}\) of the transistor with the desired \(W\) and \(L\) values.

2.) The best fit to the data is found using a genetic algorithm. The constraints on the parameters are obtained from experience with prior transistor parameters and are:

\[
10^{E-6} < \beta < 6 \times 10^{E-6}, \quad 1 < \theta < 5, \quad 0 < V_T < 1, \quad \text{and} \quad 0 < \lambda < 0.5
\]

3.) The details of the genetic algorithm are:

Gene structure is \(A = [\beta, \theta, V_T, \text{fitness}]\). A mutation was done by varying all four parameters. A weighted sum of the least square errors of the data curves was used as the error function. The fitness of a gene was chosen as 1/error.

4.) The results for an extraction run of 8000 iterations for an NMOS transistor is shown below.

<table>
<thead>
<tr>
<th>(\beta (A/V^2))</th>
<th>(\theta)</th>
<th>(V_T (V))</th>
<th>(\lambda (V^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>294.1x10^{-6}</td>
<td>1.4564</td>
<td>0.4190</td>
<td>0.1437</td>
</tr>
</tbody>
</table>

5.) The results for a NMOS and PMOS transistor are shown on the following pages.

Extraction Results for an NMOS Transistor with $W = 0.32 \mu m$ and $L = 0.18 \mu m$

Transconductance:

![Graph showing IDS vs. VGS for an NMOS Transistor](image)

Output:

![Graph showing IDS vs. VDS for an NMOS Transistor](image)
Extraction Results for an PMOS Transistor with $W = 0.32 \mu m$ and $L = 0.18 \mu m$

Transconductance:

Output:
SECTION 3.8 - SUMMARY

• Model philosophy for analog IC design
  Use simple models for design and sophisticated models for verification

• Models have several parts
  Large signal static (dc variables)
  Small signal static (midband gains, resistances)
  Small signal dynamic (frequency response, noise)
  Large signal dynamic (slew rate)

• In addition models may include:
  Temperature
  Noise
  Process variations (Monte Carlo methods)

• Computer models
  Must be numerically efficient
  Quickly derived from new technology

• Analog Design “Tricks”
  Stay away from minimum channel length if possible
    - Larger $r_{ds} \rightarrow$ larger gains
    - Better agreement
  Don’t use the computer models for design, rather verification of design