CHAPTER 2 – CMOS TECHNOLOGY

INTRODUCTION

What is Integrated Circuit Technology?

Webster:

Integrated circuit = a combination of interconnected circuit elements inseparably associated on or within a continuous substrate.

Technology = application of science or a body of knowledge to achieve an objective.

∴ Integrated circuit technology is the application of scientific knowledge to build a combination of interconnected circuit elements inseparably associated on or with a continuous substrate.

How Does IC Technology Influence Analog IC Design?

Characteristics of analog IC design:

• Continuous in signal amplitude
• Discrete or continuous in time
• Signal processing primarily depends on ratios of values and time constants
  - Ratios are generally resistance, conductance, or capacitance
  - Time constants are generally products of resistance and capacitance
• Dynamic range is determined by the largest and smallest signals

Influence of IC Technology:

• Accuracy of signal processing depends on the accuracy of the ratios of values
• The dynamic range depends upon the linearity of the circuit elements and the noise
• The value of components is limited by area considerations
• IC technology introduces resistive, capacitive and inductive parasitics that cause deviation from desired behavior
• An analog circuit is subject to the influence of other circuits fabricated in the same substrate
## Classification of Silicon Technology

![Classification of Silicon Technology Diagram]

### Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

<table>
<thead>
<tr>
<th>Comparison Feature</th>
<th>BJT</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff Frequency ($f_T$)</td>
<td>100 GHz</td>
<td>50 GHz (0.25 μm)</td>
</tr>
<tr>
<td>Noise (thermal about the same)</td>
<td>Less 1/f</td>
<td>More 1/f</td>
</tr>
<tr>
<td>DC Range of Operation</td>
<td>9 decades of exponential current versus $v_{BE}$</td>
<td>2-3 decades of square law behavior</td>
</tr>
<tr>
<td>Transconductance</td>
<td>Larger by 10X</td>
<td>Smaller by 10X</td>
</tr>
<tr>
<td>Small Signal Output Resistance</td>
<td>Slightly larger</td>
<td>Smaller for short channel</td>
</tr>
<tr>
<td>Switch Implementation</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Voltage dependent</td>
<td>More options</td>
</tr>
<tr>
<td>Technology Improvement</td>
<td>Slower</td>
<td>Faster</td>
</tr>
</tbody>
</table>

Therefore,

- Almost every comparison favors the BJT, however a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume mixed-mode technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.
Components of a Modern CMOS Technology

Illustration of a modern CMOS process:

In addition to NMOS and PMOS transistors, the technology provides:

1.) A deep $n$-well that can be utilized to reduce substrate noise coupling.
2.) A MOS varactor that can serve in VCOs
3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

CMOS Components – Transistors

$f_T$ as a function of gate-source overdrive, $V_{GS}-V_T\ (0.13\ \mu m)$:

The upper frequency limit is probably around 40 GHz for NMOS with an $f_T$ in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.
SECTION 2.1 – BASIC IC PROCESS TECHNOLOGY

FUNDAMENTAL IC PROCESSING STEPS

Basic Steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Shallow trench isolation
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon Wafer

Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.
**Diffusion**

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

Diffusion is typically done at high temperatures: 800 to 1400°C

---

**Ion Implantation**

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.
**Deposition**

Deposition is the means by which various materials are deposited on the silicon wafer. Examples:

- Silicon nitride ($\text{Si}_3\text{N}_4$)
- Silicon dioxide ($\text{SiO}_2$)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Material that is being deposited using these techniques covers the entire wafer and requires no mask.

---

**Etching**

Etching is the process of selectively removing a layer of material. When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer

Important considerations:

- **Anisotropy** of the etch is defined as,
  \[ A = 1 - \frac{\text{lateral etch rate}}{\text{vertical etch rate}} \]
- **Selectivity** of the etch (film to mask and film to substrate) is defined as,
  \[ S_{\text{film-mask}} = \frac{\text{film etch rate}}{\text{mask etch rate}} \]

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

![Fig. 150-08](image-url)
**Shallow Trench Isolation**

1.) Cover the wafer with pad oxide and silicon nitride.

2.) First etch nitride and pad oxide. Next, an anisotropic etch is made in the silicon to a depth of 0.4 to 0.5 microns.

3.) Grow a thin thermal oxide layer on the trench walls.

4.) A CVD dielectric film is used to fill the trench.

5.) A chemical mechanical polishing (CMP) step is used to polish back the dielectric layer until the nitride is reached. The nitride acts like a CMP stop layer.

6.) Densify the dielectric material at 900°C and strip the nitride and pad oxide.

---

**Epitaxy**

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even oppositely, of the material on which it grown
- It accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

---

*CMOS Analog Circuit Design*
Photolithography

Components
- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist
Areas exposed to UV light are soluble in the developer

Negative photoresist
Areas not exposed to UV light are soluble in the developer

Steps
1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake ($\approx 100°C$)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called printing.

Types of printing include:
- Contact printing
- Proximity printing
- Projection printing
Illustration of Photolithography - Positive Photoresist

TYPICAL DEEP SUBMICRON (DSM) CMOS FABRICATION PROCESS

Major Fabrication Steps for a DSM CMOS Process

1.) \( p \) and \( n \) wells
2.) Shallow trench isolation
3.) Threshold shift
4.) Thin oxide and gate polysilicon
5.) Lightly doped drains and sources
6.) Sidewall spacer
7.) Heavily doped drains and sources
8.) Siliciding (Salicide and Polycide)
9.) Bottom metal, tungsten plugs, and oxide
10.) Higher level metals, tungsten plugs/vias, and oxide
11.) Top level metal, vias and protective oxide
**Step 1 – Starting Material**
The substrate should be highly doped to act like a good conductor.

**Step 2 - *n and p* wells**
These are the areas where the transistors will be fabricated - NMOS in the *p*-well and PMOS in the *n*-well.
Done by implantation followed by a deep diffusion.
Step 3 – Shallow Trench Isolation
The shallow trench isolation (STI) electrically isolates one region/transistor from another.

\[ \text{Shallow Trench Isolation} \]
\[ \text{n-well} \]
\[ \text{p-well} \]
\[ \text{Substrate} \]

Step 4 – Threshold Shift and Anti-Punch Through Implants
The natural thresholds of the NMOS is about 0V and of the PMOS is about –1.2V. An p-implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.

Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.

\[ \text{n+ anti-punch through implant} \]
\[ \text{p+ anti-punch through implant} \]
\[ \text{p threshold implant} \]
\[ \text{p threshold implant} \]
Step 5 – Thin Oxide and Polysilicon Gates
A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.

Step 6 – Lightly Doped Drains and Sources
A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.
Step 7 – Sidewall Spacers
A layer of dielectric is deposited on the surface and removed in such a way as to leave “sidewall spacers” next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.

Step 8 – Implantation of the Heavily Doped Sources and Drains
Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.
**Step 9 – Siliciding**

Siliciding and polyciding is used to reduce interconnect resistivity by placing a low-resistance silicide such as TiSi$_2$, WSi$_2$, TaSi$_2$, etc. on top of the diffusions.

**Step 10 – Intermediate Oxide Layer**

An oxide layer is used to cover the transistors and to planarize the surface.
**Step 11 - First-Level Metal**

Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.

---

**Step 12 – Second-Level Metal**

The previous step is repeated to form the second-level metal.
**Completed Fabrication**

After multiple levels of metal are applied, the fabrication is completed with a thicker top-level metal and a protective layer to hermetically seal the circuit from the environment. Note that metal is used for the upper level metal vias. The chip is electrically connected by removing the protective layer over large bonding pads.

---

**Scanning Electron Microscope of a MOSFET Cross-section**

---
Scanning Electron Microscope Showing Metal Levels and Interconnect

Fig.180-11

DSM CMOS Technology Summary

• Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.

• Basic process steps include:
  1.) Oxide growth  
  2.) Thermal diffusion  
  3.) Ion implantation  
  4.) Deposition  
  5.) Etching  
  6.) Shallow Trench Isolation  
  7.) Epitaxy  
  8.) Siliciding (Salicide and Polycide)  
  9.) Bottom metal, tungsten plugs, and oxide  
  10.) Higher level metals, tungsten plugs/vias, and oxide  
  11.) Top level metal, vias and protective oxide

CMOS Analog Circuit Design

© P.E. Allen - 2006
ULTRA DEEP SUBMICRON (UDSM) CMOS FABRICATION PROCESS

What is UDSM CMOS Technology?

- Vindication of Moore’s Law
  “The minimum feature size decreases by approximately 0.7 every two years.”

- Minimum feature size less than 100 nanometers
- Today’s state of the art:
  - 65 nm drawn length
  - 35 nm transistor gate length
  - 1.2 nm transistor gate oxide
  - 8 layers of copper interconnect

65 Nanometer CMOS Technology

TEM cross-section of a 35 nm NMOS and PMOS transistors.†

NMOS:  
PMOS:

These transistors utilize enhanced channel strains to increase drive capability and to reduce off currents.

UDSM Metal and Interconnects

Physical aspects:

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch (nm)</th>
<th>Thickness (nm)</th>
<th>Aspect Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>220</td>
<td>230</td>
<td>-</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>220</td>
<td>90</td>
<td>-</td>
</tr>
<tr>
<td>Contacted Gate Pitch</td>
<td>220</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Metal 1</td>
<td>210</td>
<td>170</td>
<td>1.6</td>
</tr>
<tr>
<td>Metal 2</td>
<td>210</td>
<td>190</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 3</td>
<td>220</td>
<td>200</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 4</td>
<td>280</td>
<td>250</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 5</td>
<td>330</td>
<td>300</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 6</td>
<td>480</td>
<td>430</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 7</td>
<td>720</td>
<td>650</td>
<td>1.8</td>
</tr>
<tr>
<td>Metal 8</td>
<td>1080</td>
<td>975</td>
<td>1.8</td>
</tr>
</tbody>
</table>

What are the Advantages of UDSM CMOS Technology?

Digital Viewpoint:
- Improved $I_{on}/I_{off}$
- Reduced gate capacitance
- Higher drive current capability
- Reduced interconnect density
- Reduction of active power

Analog Viewpoint:
- More levels of metal
- Higher $f_T$
- Higher capacitance density
- Reduced junction capacitance per $g_m$
What are the Disadvantages of UDSM CMOS Technology (for Analog)?

- Reduction in power supply resulting in reduced headroom
- Gate leakage currents
- Reduced small-signal intrinsic gains
- Increased nonlinearity (IIP3)
- Noise and matching??

Intrinsic gain and IP3 as a function of the gate overdrive for decreasing $V_{DS}$:


What is the Gate Leakage Problem?

Gate current occurs in thin oxide devices due to direct tunneling through the thin oxide. Gate current depends on:

1. The gate-source voltage (and the drain-gate voltage)
   \[ i_{GS} = K_1 v_{GS} \exp(K_2 v_{GS}) \quad \text{and} \quad i_{GD} = K_3 v_{GD} \exp(K_4 v_{GD}) \]

2. Gate area – NMOS leakage $\approx 6nA/\mu m^2$ and PMOS leakage $\approx 3nA/\mu m^2$

Unfortunately, the gate leakage current is nonlinear with respect to the gate-source and gate-drain voltages. A possible model is:

Base current cancellation schemes used for BJTs are difficult to apply to the MOSFET.
**Gate Leakage and \( f_{gate} \)**

The gate leakage can be represented by a conductance, \( g_{gate} \), in parallel with the gate capacitance, \( C_{gate} \). Since these two elements have identical area dependence, they result in a frequency, \( f_{gate} \), that is independent and fairly independent of the drain-source voltage, \( v_{ds} \).

\[
f_{gate} = \frac{g_{gate}}{2\pi C_{gate}} \approx \begin{cases} 1.5 \cdot 10^{16} v_{GS}^2 e^{tox(v_{GS}-13.6)} & \text{(NMOS)} \\ 0.5 \cdot 10^{16} v_{GS}^2 e^{tox(v_{GS}-13.6)} & \text{(PMOS)} \end{cases}
\]

where \( tox \) is in nm and \( v_{GS} \) is in V.

For frequencies above \( f_{gate} \) the MOSFET looks capacitive and below \( f_{gate} \), the MOSFET looks resistive (gate leakage).

---

**UDSM CMOS Technology Summary**

- Increased transconductance and frequency capability
- Low power supply voltages
- Reduced parasitics
- Gate leakage causes challenges for analog applications of UDSM technology
- Other??
SECTION 2.1 – PN JUNCTIONS

How are PN Junctions used in CMOS?

- PN junctions are used to electrically isolate one semiconductor region from another
- PN diodes
- Creation of the thermal voltage for bandgap purposes
- Depletion capacitors – voltage variable capacitors (varactors)

Components of a pn junction:

1. p-doped semiconductor – a semiconductor having atoms containing a lack of electrons (acceptors). The concentration of acceptors is \( N_A \) in atoms per cubic centimeter.
2. n-doped semiconductor – a semiconductor having atoms containing an excess of electrons (donors). The concentration of these atoms is \( N_D \) in atoms per cubic centimeter.

Abrupt PN Junction

1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field, which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:
   \[
   \text{Current due to diffusion} = \text{Current due to electric field}
   \]
**Influence of Doping Level on the Depletion Regions**

Intuitively, one can see that the depletion regions are inversely proportional to the doping level. To achieve equilibrium, equal and opposite fixed charge on both sides of the junction are required. Therefore, the larger the doping the smaller the depletion region on that side of the junction.

The equations that result are:

\[
W_1 = \sqrt{\frac{2\varepsilon(\psi_o - v_D)}{qN_A(1 + \frac{N_A}{N_D})}} \propto \sqrt{\frac{1}{N_A}}
\]

and

\[
W_2 = \sqrt{\frac{2\varepsilon(\psi_o - v_D)}{qN_D(1 + \frac{N_D}{N_A})}} \propto \sqrt{\frac{1}{N_D}}
\]

**Mathematical Characterization of the Abrupt PN Junction**

Assume the pn junction is open-circuited.

Cross-section of an ideal pn junction:

Symbol for the pn junction:

Built-in potential, $\psi_o$:

\[
\psi_o = V_t \ln \left( \frac{N_A N_D}{n_i^2} \right),
\]

where

\[
V_t = \frac{kT}{q}
\]

$n_i^2$ is the intrinsic concentration of silicon.
Reverse-Biased PN Junctions

Depletion region:

\[ x_d = x_p + x_n = W_1 + W_2 \]
\[ x_p = W_1 \propto \sqrt{v_R} \]

and

\[ x_n = W_2 \propto \sqrt{v_R} \]

Breakdown voltage (BV):

If \( v_R > BV \), avalanche multiplication will occur resulting in a high conduction state as illustrated.

Depletion Capacitance

Physical viewpoint of the depletion capacitance:

\[ C_j = \frac{\varepsilon_{si} A}{d} = \frac{\varepsilon_{si} A}{W_1 + W_2} \]

\[ = \frac{\varepsilon_{si} A}{\sqrt{\frac{2 \varepsilon_{si} (\psi_o - v_D)}{q (N_D + N_A)}} \sqrt{\frac{N_D}{N_A} + \sqrt{\frac{N_A}{N_D}}}} \]

\[ = A \sqrt{\frac{\varepsilon_{si} q N_A N_D}{2 (N_A + N_D)}} \frac{1}{\sqrt{\psi_o - v_D}} \]

\[ = \frac{C_{j0}}{\sqrt{1 - \frac{v_D}{\psi_o}}} \]
**Forward-Biased PN Junctions**

When the *pn* junction is forward-biased, the potential barrier is reduced and significant current begins to flow across the junction. This current is given by:

\[
i_D = I_s \exp \left( \frac{v_D}{V_t} - 1 \right) \quad \text{where} \quad I_s = qA \left[ \frac{D_{ppno}}{L_p} + \frac{D_{nnpo}}{L_n} \right] \approx qAD \frac{n_i^2}{N} = KT \exp \left( \frac{-V_{GO}}{V_t} \right)
\]

Graphically, the *i_D* versus *v_D* characteristics are given as:

![Graph of forward-biased PN junction current vs. voltage](image)

**Graded PN Junctions**

In practice, the *pn* junction is graded rather than abrupt.

The previous expressions become:

Depletion region widths:

\[
W_1 = \frac{2\varepsilon_s qN A D}{\psi_o - v_D} m \\
W_2 = \frac{2\varepsilon_s qN A D}{q N D (N A + N D)} m
\]

Depletion capacitance:

\[
C_j = A \left( \frac{\varepsilon_s q N A D}{2(N A + N D)} \right)^m \frac{1}{(\psi_o - v_D)^m} = \frac{C_{j0}}{\left( 1 - \frac{v_D}{\psi_o} \right)^m}
\]

where \(0.33 \leq m \leq 0.5\).
Metal-Semiconductor Junctions

Ohmic Junctions: A pn junction formed by a highly doped semiconductor and metal.

Energy band diagram

\[ E_F, E_V \]

IV Characteristics

Schottky Junctions: A pn junction formed by a lightly doped semiconductor and metal.

Energy band diagram

\[ E_F, E_V \]

IV Characteristics

SECTION 2.3 – MOS TRANSISTOR

PHYSICAL ASPECTS OF MOS TRANSISTORS

Physical Structure of MOS Transistors in an n-well Technology

Width (W) of the MOSFET = Width of the source/drain diffusion

Length (L) of the MOSFET = Width of the polysilicon gate between the S/D diffusions

Note that the MOSFET is isolated from the well/substrate by reverse biasing the resulting \( pn \) junction
**Enhancement MOSFETs**

The channel between the source and drain of an enhancement MOSFET is formed when the proper potential is applied to the gate of the MOSFET. This potential inverts the material immediately below the gate to the same type of impurity as the source and drain forming the channel.

How is the threshold voltage determined?

\[
V_T = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} = V_{T0} + \gamma(\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|})
\]

where

\[
Q_b \approx \sqrt{2qN_A\varepsilon_{si}(-2\phi_F + v_{SB})}
\]

\(Q_{SS}\) is the undesired surface-state charge

\[
V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}}
\]

and

\[
\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}
\]

**Depletion Mode MOSFET**

The channel is diffused into the substrate so that a channel exists between the source and drain with no external gate potential.

The threshold voltage for a depletion mode NMOS transistor will be negative (a negative gate potential is necessary to attract enough holes underneath the gate to cause this region to invert to p-type material).
**Weak Inversion Operation**

Weak inversion operation occurs when the applied gate voltage is below $V_T$ and occurs when the surface of the substrate beneath the gate is weakly inverted.

Regions of operation according to the surface potential, $\phi_S$:
- $\phi_S < \phi_F$: Substrate not inverted
- $\phi_F < \phi_S < 2\phi_F$: Channel is weakly inverted (diffusion current)
- $2\phi_F < \phi_S$: Strong inversion (drift current)

Drift current versus diffusion current in a MOSFET:

**LAYOUT OF MOS TRANSISTORS**

**Layout of a Single MOS transistor:**

Comments:
- Make sure to contact the source and drain with multiple contacts to evenly distribute the current flow under the gate.
- Minimize the area of the source and drain to reduce bulk-source/drain capacitance.
**Geometric Effects**

Orientation:

Devices oriented in the same direction match more precisely than those oriented in other directions.

![Good Matching](041027-02)

![Poorer Matching](041027-02)

**Diffusion and Etch Effects**

- Poly etch rate variation – use dummy elements to prevent etch rate differences.

- Do not put contacts on top of the gate for matched transistors.

- Be careful of diffusion interactions for diffusions near the channel of the MOSFET
**Thermal and Stress Effects**

- Oxide gradients – use common centroid geometry layout
- Stress gradients – use proper location and common centroid geometry layout
- Thermal gradients – keep transistors well away from power devices and use common centroid geometry layout with interdigitated transistors

Examples of Common Centroid Interdigitated transistor layout:

```
ABBA
DA SA/SB DB SA/SB DA
GA GB GB GA
DB SB/SADB DA
```

**MOS Transistor Layout**

*Photolithographic invariance* (PLI) are transistors that exhibit identical orientation. PLI comes from optical interactions between the UV light and the masks.

Examples of the layout of matched MOS transistors:

1.) Examples of mirror symmetry and photolithographic invariance.
MOS Transistor Layout - Continued

2.) Two transistors sharing a common source and laid out to achieve both photolithographic invariance and common centroid.

MOS Transistor Layout - Continued

3.) Compact layout of the previous example.
SECTION 2.4 – CAPACITORS

INTRODUCTION

Types of Capacitors for CMOS Technology

1.) PN junction (depletion) capacitors

2.) MOSFET gate capacitors

3.) Conductor-insulator-conductor capacitors

Characterization of Capacitors

What characterizes a capacitor?

1.) Dissipation (quality factor) of a capacitor is

\[ Q = \omega C R_p = \frac{\omega C}{R_s} \]

where \( R_p \) is the equivalent resistance in parallel with the capacitor, \( C \), and \( R_s \) is the electrical series resistance (ESR) of the capacitor, \( C \).

2.) Parasitic capacitors to ground from each node of the capacitor.

3.) The density of the capacitor in Farads/area.

4.) The absolute and relative accuracies of the capacitor.

5.) The \( C_{\text{max}}/C_{\text{min}} \) ratio which is the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor (varactor).

6.) The variation of a variable capacitance with the control voltage.

7.) Linearity, \( q = C_v \).
**PN JUNCTION CAPACITORS**

**PN Junction Capacitors in a Well**
Generally made by diffusion into the well.

![Diagram of PN junction capacitor](image)

**Layout:**
Minimize the distance between the $p^+$ and $n^+$ diffusions.

Two different versions have been tested.
1.) Large islands – $9 \mu m$ on a side
2.) Small islands – $1.2 \mu m$ on a side

**PN-Junction Capacitors – Continued**
The anode should be the floating node and the cathode must be connected to ac ground.

**Experimental data ($Q$ at 2GHz, 0.5$\mu m$ CMOS):**

Electrons as majority carriers lead to higher $Q$ because of their higher mobility.

The resistance, $R_{wj}$, is reduced in small islands compared with large islands $\Rightarrow$ higher

---


*CMOS Analog Circuit Design*
**MOSFET Gate Capacitors**

**MOSFET Gate Capacitor Structure**

The MOSFET gate capacitors have the gate as one terminal of the capacitor and some combination of the source, drain, and bulk as the other terminal.

In the model of the MOSFET gate capacitor shown below, the gate capacitance is really two capacitors in series depending on the condition of the channel.

\[
C_{\text{gate}} = \frac{1}{C_{ox}} + \frac{1}{C_{j}}
\]

**MOSFET Gate Capacitor with D = S = B**

In this configuration, the MOSFET gate capacitor has 5 regions of operation. For the first four regions, the gate capacitance is the series combination of \( C_{ox} \) and \( C_{j} \).

\[
C_{\text{gate}} = \frac{1}{C_{ox}} + \frac{1}{C_{j}}
\]

1.) Channel is not formed (accumulation mode), \( C_{\text{gate}} = C_{ox} \)

2.) The channel is in depletion mode (the channel resistance is large and \( C_{j} \approx C_{ox} \)),

\[
C_{\text{gate}} \approx 0.5C_{ox} \approx 0.5C_{j}
\]

3.) The channel is weak inversion (channel resistance is large and \( C_{j} < C_{ox} \)),

\[
C_{\text{gate}} \approx C_{j}
\]

4.) The channel is in moderate inversion (channel resistance is decreasing and \( C_{j} < C_{ox} \)),

\[
C_{j} < C_{\text{gate}} < C_{ox}
\]

5.) The channel is in strong inversion (\( C_{ox} \) is in parallel with \( C_{j} \) and \( C_{j} < C_{ox} \)),

\[
C_{\text{gate}} \approx C_{ox}
\]

(The bulk resistance will influence the above when \( C_{\text{gate}} \approx C_{j} \))
Illustration of the MOSFET Gate Capacitor as a function of $V_{GS}$ with $D=S=B$

Conditions:
- $D = S = B$
- Operates from accumulation to inversion
- Nonmonotonic
- Nonlinear

MOSFET Gate Capacitor as a function of $V_{GS}$ with Bulk Fixed (Inversion Mode)

Conditions:
- $D = S$, $B = V_{SS}$
- Accumulation region removed by connecting bulk to $V_{DD}$
- Nonlinear
- Channel resistance:
  \[ R_{on} = \frac{L}{12KP'(V_{BG} - |V_T|)} \]
- LDD transistors will give lower $Q$ because of the increased series resistance
**Inversion Mode NMOS Capacitor**

Best results are obtained when the drain-source are on ac ground.

Experimental Results ($Q$ at 2GHz, 0.5μm CMOS)†:

\[
\begin{align*}
V_G &= 1.8V: & C_{\text{max}}/C_{\text{min}} \text{ ratio} &= 2.15 (1.91), & Q_{\text{max}} &= 34.3 (5.4), & Q_{\text{min}} &= 25.8 (4.9) \\

\end{align*}
\]


---

**Accumulation Mode NMOS Gate Capacitor**

Conditions:
- Remove p+ drain and source and put n+ bulk contacts instead.
- Implements a variable capacitor with a larger transition region between the maximum and minimum values.
- Reasonably linear capacitor for values of $V_{GB} > 0$,
Accumulation Mode Capacitor – Continued

Best results are obtained when the drain-source are on ac ground.

Experimental Results ($Q$ at 2GHz, 0.5μm CMOS):

$$V_G = 0.6V: \frac{C_{max}}{C_{min}} \text{ ratio } = 1.69 \ (1.61), \ Q_{max} = 38.3 \ (15.0), \ \text{and } Q_{min} = 33.2\ (13.6)$$


CONDUCTOR-INSULATOR-CONDUCTOR CAPACITORS

Polysilicon-Oxide-Polysilicon (Poly-Poly) Capacitors

LOCOS Technology:
A very linear capacitor with minimum bottom plate parasitic.

DSM Technology:
A very linear capacitor with larger bottom plate parasitic.
**Metal-Insulator-Metal (MiM) Capacitors**

In some processes, there is a thin dielectric between a metal layer and a special metal layer called “capacitor top metal”. Typically the capacitance is around 1fF/μm² and is at the level below top metal.

Good matching is possible with low parasitics.

---

**Metal-Insulator-Metal Capacitors – Lateral and Vertical Flux**

Capacitance between conductors on the same level and use lateral flux.

These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with a near-infinite perimeter. The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.
More Detail on Horizontal Metal Capacitors†
Some of the possible metal capacitor structures include:
1.) Horizontal parallel plate

![Horizontal parallel plate (HPP)](030909-01)

2.) Parallel wires (PW):

![Parallel wires (PW)](030909-02)

3.) Vertical parallel plates (VPP):

![Vertical parallel plates (VPP)](030909-03)

4.) Vertical bars (VB):

![Vertical bars (VB)](030909-04)

---


CMOS Analog Circuit Design © P.E. Allen - 2006
**Horizontal Metal Capacitors - Continued**

Experimental results for a CMOS process with 3 layers of metal, $L_{\text{min}}=0.5 \mu m$, $t_{\text{ox}}=0.95 \mu m$ and $t_{\text{metal}}=0.63 \mu m$ for the bottom 2 layers of metal.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Cap. Density (aF/$\mu m^2$)</th>
<th>$C_{\text{aver.}}$ (pF)</th>
<th>Std. Dev. (fF)</th>
<th>$\sigma_{C_{\text{aver.}}}$</th>
<th>$f_{\text{res.}}$ (GHz)</th>
<th>$Q @ 1$ GHz</th>
<th>$R_s$ (Ω)</th>
<th>Breakdown (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPP</td>
<td>158.3</td>
<td>18.99</td>
<td>103</td>
<td>0.0054</td>
<td>3.65</td>
<td>14.5</td>
<td>0.57</td>
<td>355</td>
</tr>
<tr>
<td>PW</td>
<td>101.5</td>
<td>33.5</td>
<td>315</td>
<td>0.0094</td>
<td>1.1</td>
<td>8.6</td>
<td>0.55</td>
<td>380</td>
</tr>
<tr>
<td>HPP</td>
<td>35.8</td>
<td>6.94</td>
<td>427</td>
<td>0.0615</td>
<td>6.0</td>
<td>21</td>
<td>1.1</td>
<td>690</td>
</tr>
</tbody>
</table>

Experimental results for a digital CMOS process with 7 layers of metal, $L_{\text{min}}=0.24 \mu m$, $t_{\text{ox}}=0.7 \mu m$ and $t_{\text{metal}}=0.53 \mu m$ for the bottom 5 layers of metal. All capacitors = 1pF.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Cap. Density (aF/$\mu m^2$)</th>
<th>$C_{\text{aver.}}$ (pF)</th>
<th>Area ($\mu m^2$)</th>
<th>Cap. Enhancement</th>
<th>Std. Dev. (fF)</th>
<th>$\sigma_{C_{\text{aver.}}}$</th>
<th>$f_{\text{res.}}$ (GHz)</th>
<th>$Q @ 1$ GHz</th>
<th>Breakdown (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPP</td>
<td>1512.2</td>
<td>1.01</td>
<td>670</td>
<td>7.4</td>
<td>5.06</td>
<td>0.0050</td>
<td>&gt;40</td>
<td>83.2</td>
<td>128</td>
</tr>
<tr>
<td>VB</td>
<td>1281.3</td>
<td>1.07</td>
<td>839.7</td>
<td>6.3</td>
<td>14.19</td>
<td>0.0132</td>
<td>37.1</td>
<td>48.7</td>
<td>124</td>
</tr>
<tr>
<td>HPP</td>
<td>203.6</td>
<td>1.09</td>
<td>5378</td>
<td>1.0</td>
<td>26.11</td>
<td>0.0239</td>
<td>21</td>
<td>63.8</td>
<td>500</td>
</tr>
<tr>
<td>MIM</td>
<td>1100</td>
<td>1.05</td>
<td>960.9</td>
<td>5.4</td>
<td>-</td>
<td>-</td>
<td>11</td>
<td>95</td>
<td>-</td>
</tr>
</tbody>
</table>

*CMOS Analog Circuit Design © P.E. Allen - 2006*

**Horizontal Metal Capacitors - Continued**

Histogram of the capacitance distribution for the above case (1 pF):

Experimental results for a digital CMOS process with 7 layers of metal, $L_{\text{min}}=0.24 \mu m$, $t_{\text{ox}}=0.7 \mu m$ and $t_{\text{metal}}=0.53 \mu m$ for the bottom 5 layers of metal (all capacitors = 10pF):

<table>
<thead>
<tr>
<th>Structure</th>
<th>Cap. Density (aF/$\mu m^2$)</th>
<th>$C_{\text{aver.}}$ (pF)</th>
<th>Area ($\mu m^2$)</th>
<th>Cap. Enhancement</th>
<th>Std. Dev. (fF)</th>
<th>$\sigma_{C_{\text{aver.}}}$</th>
<th>$f_{\text{res.}}$ (GHz)</th>
<th>$Q @ 1$ GHz</th>
<th>Breakdown (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPP</td>
<td>1480.0</td>
<td>11.46</td>
<td>7749</td>
<td>8.0</td>
<td>73.43</td>
<td>0.0064</td>
<td>11.3</td>
<td>26.6</td>
<td>125</td>
</tr>
<tr>
<td>VB</td>
<td>1223.2</td>
<td>10.60</td>
<td>8666</td>
<td>6.6</td>
<td>73.21</td>
<td>0.0069</td>
<td>11.1</td>
<td>17.8</td>
<td>121</td>
</tr>
<tr>
<td>HPP</td>
<td>183.6</td>
<td>10.21</td>
<td>55615</td>
<td>1.0</td>
<td>182.1</td>
<td>0.0178</td>
<td>6.17</td>
<td>23.5</td>
<td>495</td>
</tr>
<tr>
<td>MIM</td>
<td>1100</td>
<td>10.13</td>
<td>9216</td>
<td>6.0</td>
<td>-</td>
<td>-</td>
<td>4.05</td>
<td>25.6</td>
<td>-</td>
</tr>
</tbody>
</table>

*CMOS Analog Circuit Design © P.E. Allen - 2006*
DEVIATION FROM IDEAL BEHAVIOR IN CAPACITORS

Capacitor Errors
1.) Dielectric gradients
2.) Edge effects
3.) Process biases
4.) Parasitics
5.) Voltage dependence
6.) Temperature dependence

Capacitor Errors - Oxide Gradients
Error due to a variation in dielectric thickness across the wafer.
Common centroid layout - only good for one-dimensional errors:

An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.

Improved matching of three components, A, B, and C:
**Capacitor Errors - Edge Effects**

There will always be a randomness on the definition of the edge. However, etching can be influenced by the presence of adjacent structures. For example,

Matching of A and B are disturbed by the presence of C.

Improved matching achieve by matching the surroundings of A and B.

**Process Bias on Capacitors**

Consider the following two capacitors:

If $L_1 = L_2 = 2 \mu m$, $W_2 = 2W_1 = 2 \mu m$ and $\Delta x = 0.1 \mu m$, the ratio of $C_2$ to $C_1$ can be written as,

$$\frac{C_2}{C_1} = \frac{(2-2)(4-2)}{(2-2)(2-2)} = \frac{3.8}{1.8} = 2.11 \rightarrow 5.6\% \text{ error in matching}$$

How can this matching error be reduced?

The capacitor ratios in general can be expressed as,

$$\frac{C_2}{C_1} = \frac{(L_2-2\Delta x)(W_2-2\Delta x)}{(L_1-2\Delta x)(W_1-2\Delta x)} = \frac{W_2}{W_1} \left(1 - \frac{2\Delta x}{W_2} \right) \approx \frac{W_2}{W_1} \left(1 - \frac{2\Delta x}{W_2} + \frac{2\Delta x}{W_1} \right)$$

Therefore, if $W_2 = W_1$, the matching error should be minimized. The best matching results between two components are achieved when their geometries are identical.
**Replication Principle**

Based on the previous result, a way to minimize the matching error between two or more geometries is to insure that the matched components have the same area to periphery ratio. Therefore, the replication principle requires that all geometries have the same area-periphery ratio.

Correct way to match the previous capacitors (the two $C_2$ capacitors are connected together):

If $L_1 = L_2 = 2 \mu m$, $W_2 = 2W_1 = 2 \mu m$ and $\Delta x = 0.1 \mu m$, the ratio of $C_2$ to $C_1$ can be written as,

$$\frac{C_2}{C_1} = \frac{2(2\cdot2)(2\cdot2)}{(2\cdot2)(2\cdot2)} = \frac{2\cdot1.8}{1.8} = 2 \rightarrow 0\% \text{ error in matching}$$

The replication principle works for any geometry and includes transistors, resistors as well as capacitors.

---

**Capacitor Errors - Relative Accuracy**

Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,
Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

![Diagram showing top and bottom plate parasitics](image)

Top plate parasitic is 0.01 to 0.001 of $C_{\text{desired}}$
Bottom plate parasitic is 0.05 to 0.2 $C_{\text{desired}}$

---

Layout Considerations on Capacitor Accuracy

Decreasing Sensitivity to Edge Variation:

- Sensitive to alignment errors in the upper and lower plates and loss of capacitance flux (smaller capacitance).
- Insensitive to alignment errors and the flux reaching the bottom plate is larger resulting in large capacitance.

A structure that minimizes the ratio of perimeter to area (circle is best).
Accurate Matching of Capacitors

Accurate matching of capacitors depends on the following influence:

1.) Mismatched perimeter ratios
2.) Proximity effects in unit capacitor photolithography
3.) Mismatched long-range fringe capacitance
4.) Mismatched interconnect capacitance
5.) Parasitic interconnect capacitance

Long-range fringe capacitance:

![Diagram of long-range fringe fields]

Obviously there will be a tradeoff between matching and speed.

---

Shielding Capacitors

The key to shielding is to determine and control the electric fields. Consider the following noisy conductor and its influence on the substrate:

![Diagram of noisy conductor and substrate]

Increased Parasitic Capacitance

Use of bootstrapping to reduce capacitor bottom plate parasitic:

![Diagram of bootstrapping effect]

---


CMOS Analog Circuit Design © P.E. Allen - 2006
Definition of Temperature and Voltage Coefficients

In general a variable \( y \) which is a function of \( x \), \( y = f(x) \), can be expressed as a Taylor series,

\[
y(x = x_0) \approx y(x_0) + a_1(x- x_0) + a_2(x- x_0)^2 + a_3(x- x_0)^3 + \cdots
\]

where the coefficients, \( a_i \), are defined as,

\[
a_1 = \left. \frac{df(x)}{dx} \right|_{x=x_0} , \quad a_2 = \left. \frac{d^2f(x)}{dx^2} \right|_{x=x_0} , \ldots
\]

The coefficients, \( a_i \), are called the first-order, second-order, … temperature or voltage coefficients depending on whether \( x \) is temperature or voltage.

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called fractional temperature coefficient, \( TCF \), which is defined as,

\[
TCF(T=T_0) = \left. \frac{1}{f(T=T_0)} \frac{df(T)}{dT} \right|_{T=T_0} \text{ parts per million/°C (ppm/°C)}
\]

or more simply,

\[
TCF = \left. \frac{1}{f(T)} \frac{df(T)}{dT} \right| \text{ parts per million/°C (ppm/°C)}
\]

A similar definition holds for fractional voltage coefficient.

Capacitor Errors - Temperature and Voltage Dependence

MOSFET Gate Capacitors:
- Absolute accuracy \( \approx \pm 10\% \)
- Relative accuracy \( \approx \pm 0.2\% \)
- Temperature coefficient \( \approx +25 \text{ ppm}/\text{°C} \)
- Voltage coefficient \( \approx -50 \text{ppm}/\text{V} \)

Polysilicon-Oxide-Polysilicon Capacitors:
- Absolute accuracy \( \approx \pm 10\% \)
- Relative accuracy \( \approx \pm 0.2\% \)
- Temperature coefficient \( \approx +25 \text{ ppm}/\text{°C} \)
- Voltage coefficient \( \approx -20 \text{ppm}/\text{V} \)

Metal-Dielectric-Metal Capacitors:
- Absolute accuracy \( \approx \pm 10\% \)
- Relative accuracy \( \approx \pm 0.6\% \)
- Temperature coefficient \( \approx +?? \text{ ppm}/\text{°C} \)
- Voltage coefficient \( \approx -?? \text{ppm}/\text{V} \)

Accuracies depend upon the size of the capacitors.
**Future Technology Impact on Capacitors**

What will be the impact of scaling down in CMOS technology?

- The capacitance can be divided into gate capacitance and overlap capacitance.
  
  Gate capacitance varies with external voltage changes

  Overlap capacitances are constant with respect to external voltage changes

  As the channel length decreases, the gate capacitance becomes less of the total capacitance and consequently the $C_{\text{max}}/C_{\text{min}}$ will decrease. However, the $Q$ of the capacitor will increase because the physical dimensions are getting smaller.

- For UDSM, the gate leakage current will eliminate gate capacitors from being useful.

**Best capacitor for future scaled CMOS?**

Polysilicon-polysilicon or metal-metal (too much leakage current in gate capacitors)

**Best varactor for future scaled CMOS?**

The standard mode CMOS depletion capacitor because $C_{\text{max}}/C_{\text{min}}$ is larger than that for the accumulation mode and $Q$ should be sufficient. The $pn$ junction will be more useful for UDSM.

---

**SECTION 2.5 – RESISTORS**

**Types of Resistors Compatible with CMOS Technology**

1.) Diffused and/or implanted resistors.

2.) Well resistors.

3.) Polysilicon resistors.

4.) Metal resistors.
Characterization of Resistors

1.) Value

$$R = \frac{\rho L}{A}$$

AC and DC resistance

2.) Linearity

Does $$V = IR$$?
Velocity saturation of carriers

3.) Power

$$P = VI = I^2R$$

4.) Current

Electromigration

5.) Parasitics

MOS Resistors - Source/Drain Resistor

Diffusion:

- 10-100 ohms/square
- Absolute accuracy = ±35%
- Relative accuracy=2% (5μm), 0.2% (50μm)
- Temperature coefficient = +1500 ppm/°C
- Voltage coefficient = 200 ppm/V

Ion Implanted:

- 500-2000 ohms/square
- Absolute accuracy = ±15%
- Relative accuracy=2% (5μm), 0.15% (50μm)
- Temperature coefficient = +400 ppm/°C
- Voltage coefficient = 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.
**Polysilicon Resistor**

30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±3 0%
Relative accuracy = 2% (5 μm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

Comments:
- Used for fuzes and laser trimming
- Good general resistor with low parasitics

**N-well Resistor**

1000-5000 ohms/square
Absolute accuracy = ±40%
Relative accuracy ≈ 5%
Temperature coefficient = 4000 ppm/°C
Voltage coefficient is large ≈ 8000 ppm/V

Comments:
- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
- Could put a $p^+$ diffusion into the well to form a pinched resistor
**Metal as a Resistor**

**Illustration:**

Resistance from A to B = Resistance of segments $L_1$, $L_2$, $L_3$, $L_4$, and $L_5$ with some correction subtracted because of corners.

Sheet resistance:

- 50-70 m$\Omega$/sq $\pm$ 30% for lower or middle levels of metal
- 30-40 m$\Omega$/sq $\pm$ 15% for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from 5$\Omega$ to 10$\Omega$.

Tempco $\approx +4000$ ppm/$^\circ$C

---

**Thin Film Resistors**

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:

Performance:

- Sheet resistivity is approximately 5-10 ohms/square
- Temperature coefficients of less than 100 ppm/$^\circ$C
- Absolute tolerance of better than $\pm 0.1\%$ using laser trimming
- Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.
Resistor Layout Techniques

**LOCOS Technology**

Metal

Substrate

Active area (diffusion)

**DSM Technology**

Tungsten Plug

Intermediate Oxide

Substrate

Active area (diffusion)

Contact

Active area or Polysilicon

W

Cut

L

Metal 1

Diffusion or polysilicon resistor

Active area (diffusion)

Well diffusion

Active area (diffusion)

Extending the Length of Resistors

**Snaked Resistors:**

Corner corrections:

0.5

1.45

1.25

Fig. 2.6-16B
Extending the Length of Resistors

Series Resistors:

Resistor Ending Influence:

Process Bias Influence on Resistors

Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.

Process biases introduce systematic errors.

Consider the effect of over-etching-

Assume that etching introduces a process bias of 0.1 μm. Two resistors designed to have a ratio of 2:1 have equal lengths but the widths are different by a factor of two.

The actual matching ratio due to the etching bias is,

\[
\frac{R_2}{R_1} = \frac{W_1}{W_2} = \frac{4 - 0.2}{2 - 0.2} = \frac{3.8}{1.8} = 2.11 \quad \rightarrow \quad 5.6\% \text{ error in matching}
\]

Use the replication principle to eliminate this error.
**Etch Rate Variations – Polysilicon Resistors**

The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant. This is illustrated below:

The objective is to make $A = B = C$. In the left-hand case, $B$ is larger due to the slower etch rates on both sides of $B$. In the right-hand case, the dummy strips have caused the etch rates on both sides of $A$, $B$ and $C$ to be identical leading to better matching. It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.

**Diffusion Interaction – Diffused Resistors**

Problem:
Consider three adjacent $p^+$ diffusions into a $n$ epitaxial region,

If $A$, $B$, and $C$ are resistors that are to be matched, we see that the effective concentration of $B$ is larger than $A$ or $C$ because of diffusion interaction. This would cause the $B$ resistor to be smaller even though the geometry is identical.

Solution: Place identical dummy resistors to the left of $A$ and right of $C$. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.
**Thermoelectric Effects**

The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures. The potential developed is given as,

\[ V_T = S \cdot \Delta T \]

where,

- \( S \) = Seebeck coefficient (≈ 0.4mV/°C)
- \( \Delta T \) = temperature difference between the two metals

Thus, a temperature difference between the contacts to a resistor and the resistor of 1°C can generate a voltage of 0.4mV causing problems in certain circuits (bandgap).

Two possible resistor layouts with regard to the thermoelectric effect:

![Thermoelectric potentials add](image)

![Thermoelectric potentials cancel](image)

---

**High Sheet Resistivity Resistor Layout**

High sheet resistivity resistors must use p+ or n+ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.

![Sensitive to thermoelectric effects](image)

![Sensitive to misalignment](image)

![Resistor layout that minimizes thermoelectric effect and misalignment](image)
**Future Technology Impact on Resistors**

What will be the impact of scaling down in CMOS technology?

- If the size of the resistor remains the same, there will be little impact.
- If the size scales with the technology, the contacts and connections to the resistors will have more influence on the resistor.


---

**MOS Passive RC Component Performance Summary**

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Range of Values</th>
<th>Absolute Accuracy</th>
<th>Relative Accuracy</th>
<th>Temperature Coefficient</th>
<th>Voltage Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET gate Cap.</td>
<td>6-7 fF/μm²</td>
<td>10%</td>
<td>0.1%</td>
<td>20ppm/°C</td>
<td>±20ppm/V</td>
</tr>
<tr>
<td>Poly-Poly Capacitor</td>
<td>0.3-0.4 fF/μm²</td>
<td>20%</td>
<td>0.1%</td>
<td>25ppm/°C</td>
<td>±50ppm/V</td>
</tr>
<tr>
<td>Metal-Metal Capacitor</td>
<td>0.1-1fF/μm²</td>
<td>10%</td>
<td>0.6%</td>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>Diffused Resistor</td>
<td>10-100 Ω/sq.</td>
<td>35%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>200ppm/V</td>
</tr>
<tr>
<td>Ion Implanted Resistor</td>
<td>0.5-2 kΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>400ppm/°C</td>
<td>800ppm/V</td>
</tr>
<tr>
<td>Poly Resistor</td>
<td>30-200 Ω/sq.</td>
<td>30%</td>
<td>2%</td>
<td>1500ppm/°C</td>
<td>100ppm/V</td>
</tr>
<tr>
<td>n-well Resistor</td>
<td>1-10 kΩ/sq.</td>
<td>40%</td>
<td>5%</td>
<td>8000ppm/°C</td>
<td>10kppm/V</td>
</tr>
<tr>
<td>Top Metal Resistor</td>
<td>30 mΩ/sq.</td>
<td>15%</td>
<td>2%</td>
<td>4000ppm/°C</td>
<td>?</td>
</tr>
<tr>
<td>Lower Metal Resistor</td>
<td>70 mΩ/sq.</td>
<td>28%</td>
<td>3%</td>
<td>4000ppm/°C</td>
<td>?</td>
</tr>
</tbody>
</table>
### SECTION 2.6 – INDUCTORS

#### Characterization of Inductors

1.) Value of the inductor

Spiral inductor†:

\[ L \approx \mu_0 n^2 r = 4\pi \times 10^{-7} n^2 r \approx 1.2 \times 10^{-6} n^2 r \]

2.) Quality factor, \( Q = \frac{\omega L}{R} \)

3.) Self-resonant frequency: \( f_{\text{self}} = \frac{1}{\sqrt{LC}} \)

---


---

#### IC Inductors

What is the range of values for on-chip inductors?

![Inductor area too large](image)

Consider an inductor used to resonate with 5pF at 1000MHz.

\[ L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5 \times 10^{-12}} = 5\text{nH} \]

Note: Off-chip connections will result in inductance as well.
Candidates for inductors in CMOS technology are:
1.) Bond wires
2.) Spiral inductors
3.) Multi-level spiral
4.) Solenoid

Bond wire Inductors:

- Function of the pad distance $d$ and the bond angle $\beta$
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 $\Omega$/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors in CMOS Technology

Typically: $3 < N_{\text{turns}} < 5$ and $S = S_{\text{min}}$ for the given current
Select the OD, $N_{\text{turns}}$, and $W$ so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:
- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon
Planar Spiral Inductors on a Lossy Substrate

- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- Accurate analysis of a spiral inductor requires complex electromagnetic simulation
- Optimize the values of $W$, $S$, and $N$ to get the desired $L$, a high $Q$, and a high self-resonant frequency
- Typical values are $L = 1$-$8\text{nH}$ and $Q = 3$-$6$ at $2\text{GHz}$

Inductor Modeling

Model:

$$L \approx \frac{37.5\mu_0 N^2 a^2}{11D-14a}$$

$$R_s \approx \frac{L}{W\alpha(1-e^{-t/\delta})}$$

$$C_p = NW^2 L \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{ox} = W\cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$R_1 \approx \frac{WLC_{sub}}{2}$$

$$C_1 \approx \frac{2}{WLC_{sub}}$$

where

- $\mu_0 = 4\pi \times 10^{-7}$ H/m (vacuum permeability)
- $\sigma$ = conductivity of the metal
- $a$ = distance from the center of the inductor to the middle of the windings
- $L$ = total length of the spiral
- $t$ = thickness of the metal
- $\delta$ = skin depth given by $\delta = \sqrt{2/\mu_0 \sigma}$
- $G_{sub} (C_{sub})$ is a process-dependent parameter
Inductor Modeling – Continued

Definition of the previous components:
- \( R_s \) is the low frequency resistive loss of a metal and the skin effect
- \( C_p \) arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn-to-turn is also included.
- \( C_{ox} \) is the capacitance between the spiral and the substrate
- \( R_1 \) is the substrate loss due to eddy currents
- \( C_1 \) is capacitance of the substrate

Design specifications:
- \( L \) = desired inductance value
- \( Q \) = quality factor
- \( f_{SR} \) = self-resonant frequency. The resonant frequency of the LC tank represents the upper useful frequency limit of the inductor. Inductor operation frequency should be lower than \( f_{SR} \), \( f < f_{SR} \).

ASITIC: A software tool for analysis and simulation of CMOS spiral inductors and transformers.
- [http://formosa.eecs.berkeley.edu/~niknejad/asitic.html](http://formosa.eecs.berkeley.edu/~niknejad/asitic.html)

Guidelines for Designing CMOS Spiral Inductors†

- **D** – Outer diameter:
  - As \( D \) increases, \( Q \) increases but the self-resonant frequency decreases
  - A good design generally has \( D < 200 \mu m \)

- **W** – Metal width:
  - Metal width should be as wide as possible
  - As \( W \) increases, \( Q \) increases and \( R_s \) decreases
  - However, as \( W \) becomes large, the skin effects are more significant, increasing \( R_s \)
  - A good value of \( W \) is \( 10 \mu m < W < 20 \mu m \)

- **S** – Spacing between turns:
  - The spacing should be as small as possible
  - As \( S \) and \( L \) increase, the mutual inductance, \( M \), decreases
  - Use minimum metal spacing allowed in the technology but make sure the interwinding capacitance between turns is not significant

- **N** – Number of turns:
  - Use a value that gives a layout convenient to work with other parts of the circuit

Design Example

A 2GHz LC tank is to be designed as a part of LC oscillator. The $C$ value is given as 3pF.

(a) Find value of $L$. (b) Design a spiral inductor with $L$ value ($\pm 5\%$ range) from (a) using ASITIC. Optimize design parameters, $W$, $S$, $D$ and $N$ to get a high $Q$ ($Q_{\text{min}} = 5$). Show $L$, $Q$, $f_{SR}$ value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model.

Solution

(a) LC tank oscillation frequency is given as 2GHz.

$$\omega_{\text{osc}} = \frac{1}{\sqrt{LC}}, \quad L = \frac{1}{\omega_{\text{osc}}^2 C} = \frac{1}{(2\pi \cdot 2 \times 10^9)^2 \cdot (3 \times 10^{-12})} = 2.11 \times 10^{-9}$$

$\therefore$ $L = 2.11\text{nH}$ is desired.

(b) $L = 2.11\text{nH}(\pm 5\%)$ is used as input parameter. Several design parameters are tried to get high $Q$ and $f_{SR}$ values. Final design has

- Parameters: $W = 19\mu\text{m}$, $S = 1\mu\text{m}$, $D = 200\mu\text{m}$, $N = 3.5$
- Resulting inductor: $L = 2.06\text{nH}$, $Q = 7.11$, $f_{SR} = 9.99\text{GHz} @ 2\text{GHz}$

This design is acceptable as $Q > Q_{\text{min}}$ and $f < f_{SR}$.

Design Example-Continued

(c.) ASITIC generates a layout automatically. It can be saved and imported to use in other tools such as Cadence, ADS and Sonnet.

(d) Analysis in ASITIC gives the following $\pi$ model.

The $\pi$ model is usually not symmetrical and this can be used for differential configuration where none of the two ports are ac-grounded.
**Reduction of Capacitance to Ground**

Comments concerning implementation:

1. Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field
2. Avoid contact resistance wherever possible to keep the series resistance low.
3. Use the metal with the lowest resistance and farthest away from the substrate.
4. Parallel metal strips if other metal levels are available to reduce the resistance.

Example →

---

**Multi-Level Spiral Inductors**

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.

\[ Q = 5-6, f_{SR} = 30-40\text{GHz} \]
\[ Q = 10-11, f_{SR} = 15-30\text{GHz} \]

Good for high \( L \) in small area.

---

\(^1\) The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.
Inductors - Continued

Self-resonance as a function of inductance.  Outer dimension of inductors.

Transformers

Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

Method of reducing the inter-winding capacitances.

Measured 1:2 transformer voltage gains:
Transformers – Continued

A 1:4 transformer:

Structure - Measured voltage gain -

\[ \text{(} C_L = 0, 50\text{fF}, 100\text{fF}, 500\text{fF} \text{ and } 1\text{pF.} \]
\[ C_L \text{ is the capacitive loading on the secondary.)} \]

Summary of Inductors

Scaling? To reduce the size of the inductor would require increasing the flux density which is determined by the material the flux flows through. Since this material will not change much with scaling, the inductor size will remain constant.

Increase in the number of metal layers will offer more flexibility for inductor and transformer implementation.

Performance:

• Inductors
  - Limited to nanohenrys
  - Very low \( Q \) (3-5)
  - Not variable

• Transformers
  - Reasonably easy to build and work well using stacked inductors

• Matching
  - Not much data exists publicly – probably not good
SECTION 2.7 – FURTHER CONSIDERATIONS OF CMOS TECHNOLOGY

PARASITIC BIPOLAR TRANSISTORS

A Lateral Bipolar Transistor

*n*-well CMOS technology:
• It is desirable to have the lateral collector current much larger than the vertical collector current.
• Lateral BJT generally has good matching.
• The lateral BJT can be used as a photodetector with reasonably good efficiency.

A Field-Aided Lateral BJT

Use minimum channel length to enhance beta:
$$\beta_F \approx 50 \text{ to } 100 \text{ depending on the process}$$
HIGH VOLTAGE CMOS TRANSISTORS

Extended Voltage MOSFETs

The electric field from the source to drain in the channel is shown below.

The voltage drop from drain to source is,

$$V_{DS} = V_p + V_d = 0.5(E_{max}x_p + E_{max}x_d) = 0.5E_{max}(x_p + x_d)$$

$E_{max}$ and $x_p$ are limited by hot carrier generation and channel length modulation requirements whereas these limitations do not exist for $x_d$.

Therefore, to get extended voltage transistors, make $x_d$ larger.

Methods of Increasing the Drain Depletion Region

Lightly-Doped Drains (LDD):

- The lateral dimension of the lightly doped area is not large enough to stand higher voltages.
- The oxide at the drain end is too thin to stand higher voltages

Double Diffused Drains (DDD):

Uses the difference in diffusivity between arsenic and phosphorus.

- Same problems as for the LDD structure
**Lateral DMOS (LDMOS) Using CMOS Technology**

The LDMOS structure is designed to provide sufficient lateral dimension and to prevent oxide breakdown by the higher drain voltages.

- Structure is symmetrical about the source/bulk contact
- Channel is formed in the p region under the gates
- Drain voltage can be 20-30V

---

**LATCHUP IN CMOS TECHNOLOGY**

**What is Latchup?**

Latchup is the regenerative process that can occur in a *pn*pn* structure (SCR-silicon controlled rectifier) formed by a parasitic *npn* and a parasitic *pnp* transistor.

Important concepts:
- To avoid latchup, $v_{P_{PNP}} \leq V_S$
- Once the *pn*pn* structure has latched up, the large current required by the above $i$-$v$ characteristics must be provided externally to sustain latchup
- To remove latchup, the current must be reduced below the holding current
**Latchup Triggering**

Latchup of the SCR can be triggered by two different mechanisms.

1.) Allowing $v_{P_{NP}}$ to exceed the sustaining voltage, $V_S$.

2.) Injection of current by a triggering device (gate triggered)

Note: The gates mentioned above are SCR junction gates, not MOSFET gates.

---

**How does Latchup Occur in an IC?**

Consider an output driver in CMOS technology:

Assume that the output is connected to a pad.
Parasitic Bipolar Transistors for the n-well CMOS Inverter

Parasitic components:
- Lateral BJTs LT1 and LT2
- Vertical BJTs VT1 and VT2
- Bulk substrate resistances $R_{s1}$, $R_{s2}$, $R_{s3}$, and $R_{s4}$
- Bulk well resistances $R_{w1}$, $R_{w2}$, $R_{w3}$, and $R_{w4}$

Current Source Injection

Apply a voltage compliant current source to the output pad ($v_{OUT} > V_{DD}$).
Current Sink Injection

Apply a voltage compliant current sink to the output pad ($v_{OUT} < 0$).

Latchup from a Transmission Gate

The classical push-pull output stage is only one of the many configurations that can lead to latchup. Here is another configuration:

The two bold solid bipolar transistors in the transmission gate act as injectors to the $nnpn$- parasitic bipolars of the clock driver and cause these transistors to latchup. The injector sites are the diffusions connected to the pad.
**Preventing Latch-Up**

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of $R_N$ and $R_P$. This requires more current before latch-up can occur.

3.) Surround the transistors with guard rings. Guard rings reduce transistor betas and divert collector current from the base of SCR transistors.

![Figure 190-10](image)

**What are Guard Rings?**

Guard rings are used to collector carriers flowing in the silicon. They can be designed to collect either majority or minority carriers.

**Guard rings in n-material:**

- **$n^+$ guard ring**
  - Collects majority carriers
  - Increased doping level

- **$p^+$ guard ring**
  - Collects minority carriers
  - Decreased bulk resistance

**Guard rings in p-material:**

- **$p^+$ guard ring**
  - Collects majority carriers

- **$n^+$ guard ring**
  - Collects minority carriers

Also, the increased doping level of the $n^+$ ($p^+$) guard ring in $n$ ($p$) material decreases the resistance in the area of the guard ring.

![Figure 051201-01](image)
**Example of Reducing the Sensitivity to Latchup**

Start with an inverter with no attempt to minimize latchup and minimum spacing between the NMOS and PMOS transistors.

![Diagram of a basic inverter circuit with labels for Vin, Vout, VDD, Rs, and Rw.]

Note minimum separation

**Example of Reducing the Sensitivity to Latchup by using Guard Rings**

Next, place guard rings around the NMOS and PMOS transistors (both I/O and logic) to collect most of the parasitic NPN and PNP currents locally and prevent turn-on of adjacent devices.

![Diagram of a circuit with guard rings around the transistors.]

- The guard rings also help to reduce the effective well and substrate resistance.
- The guard rings reduce the lateral beta

Key: The guard rings should act like collectors
**Example of Reducing the Sensitivity to Latchup by using Butted Contacts**

Finally, use butted source contacts to further reduce the well resistance and reduce the substrate resistance.

![Diagram showing gate oxide, poly, nitride, salicide, and metal layers with labels for voltage levels and guard rings.]

**Guidelines for Guard Rings**

- Guard rings should be low resistance paths.
- Guard rings should utilize continuous diffusion areas.
- More than one transistor of the same type can be placed inside the same well inside the same guard ring as long as the design rules for spacing are followed.
- Only 2 guard rings are required between adjacent PMOS and NMOS transistors.
- The well taps and/or the guard ring should be laid out as close to the MOSFET source as possible.
- I/O output NMOSFET should use butted composite for source to bulk connections when the source is electrically connected to the p-well tap. If separate well tap and source connections are required due to substrate noise injection problems, minimize the source-well tap spacing. This will minimize latch up and early snapback of the output MOSFETs with the drain diffusion tied directly (in metal) to the bond pad.
ESD IN CMOS TECHNOLOGY

What is Electrostatic Discharge?
Triboelectric charging happens when 2 materials come in contact and then are separated.

An ESD event occurs when the stored charge is discharged.

ESD and Integrated Circuits
• ICs consist of components that are very sensitive to excess current and voltage above the nominal power supply.
• Any path to the outside world is susceptible to ESD
• ESD damage can occur at any point in the IC assembly and packaging, the packaged part handling or the system assembly process.
• Note that power is normally not on during an ESD event
**ESD Models and Standards**

- Standard tests give an indication of the ICs robustness to withstand ESD stress.
- Increased robustness:
  - Reduces field failures due to ESD
  - Demanded by customers
- Simple ESD model:
  - $V_{SE} = \text{Charging Voltage}$
  - Key parameters of the model:
    - Maximum current flow
    - Time constant or how fast the ESD discharges
    - Risetime of the pulse

\[ \text{Current} \]
\[ \tau \approx R_{Lim}C \]

**ESD Models**

- Human body model (HBM): Representative of an ESD event between a human and an electronic component.

- Machine model (MM): Simulates the ESD event when a charged “machine” discharges through a component.

- Charge device model (CDM): Simulates the ESD event when the component is charged and then discharges through a pin. The substrate of the chip becomes charged and discharges through a pin.
**ESD Influence on Components**

An ESD event typically creates very high values of current (1-10A) for very short periods of time (150 ns) with very rapid rise times (1ns).

Therefore, components experience extremely high values of current with very little power dissipation or thermal effects.

Resistors – become nonlinear at high currents and will breakdown

Capacitors – become shorts and can breakdown from overvoltage (pad to substrate)

Diodes – current no longer flows uniformly (the connections to the diodes represent the ohmic resistance limit)

Transistors – ESD event is only a two terminal event, the third terminal is influenced by parasitics and many parameters out of control

- MOSFETs – the parasitic bipolar experiences snapback under an ESD event
- BJTs – will experience snapback under ESD event

---

**Objective of ESD Protection**

- There must be a safe low impedance path between every combination of pins to sink the ESD current (i.e. 1.5A for 2kV HBM)
- The ESD device should clamp the voltage below the breakdown voltage of the internal circuitry
- The metal busses must be designed to survive 1.5A (fast transient) without building up excessive voltage drop
- ESD current must be steered away from sensitive circuits

- ESD protection will require area on the chip (busses and timing components)
**ESD Protection Architecture**

Local clamps – Designed to pass ESD current without loading the internal (core) circuits
ESD power rail clamps – Designed to pass large amount of current with a small voltage drop

**ESD Events:**
- Pad-to-rail (uses local clamps only)
- Pad-to-pad (uses either local or local and ESD power rail clamps)

**ESD Breakdown Clamp Example**

A normal MOSFET that uses the parasitic lateral BJT to achieve a snapback clamp. Normally, the MOSFET has the gate shorted to the source so that drain current is zero.

**Issues:**
- If the drain voltage becomes too large, the gate oxide may breakdown
- If the transistor has multiple fingers, the layout should ensure that the current is distributed evenly.
Non-Breakdown Clamp Example

Merrill Clamp:

Operation:
- Normally, the input to the driver is high, the output low and the NMOS clamp off.
- For a positive ESD event, the voltage increases across $R$ causing the inverter to turn on the NMOS clamp providing a low impedance path between the rails.
- Cannot be used for pads that go above power supply or are active when powered up.
- For power supply turn-on, the circuit should not trigger ($C$ holds the clamp off during turn-on).

Also, forward biased diodes serve as non-breakdown clamps.

IV Characteristics of Good ESD Protection

Goal: Sink the ESD current and clamp the voltage.
Comparison Between the Merrill Clamp and the Snapback Clamp

Increasing the Merrill clamp MOS width will reduce the clamp voltage.

Note that the Merrill clamp does not normally exceed the absolute maximum voltage. Merrill clamps should be used with EPROMs to avoid reprogramming during an ESD event.

ESD Practice

General Guidelines:

• Understand the current flow requirements for an ESD event
• Make sure the current flows where desired and is uniformly distributed
• Series resistance is used to limit the current in the protected devices
• Minimize the resistance in protecting devices
• Use distributed (smaller) active clamps to minimize the effect of bus resistance
• Understand the influence of packaging on ESD
• Use guard rings to prevent latchup

Check list:

• Check the ESD path between every pair of pads
• Check for ESD protection between the pad and internal circuitry
• Check for low bus resistance
  - Current: Minimum metal for ESD $\approx 40 \times$ Electromigration limit
  - Voltage: 1.5A in a metal bus of 0.03Ω/square of 1000μm long and 30μm wide gives a voltage drop of 1.5V
• Check for sufficient contacts and vias in the ESD path (uniform current distribution)
SECTION 2.8 – SUMMARY

Review

• Importance of technology on circuit design – technology establishes the boundaries and constraints for the circuit design
• Basic IC processes – defines the physical aspects of components and the nonideal behavior
• \textit{pn} junctions – fundamental component of integrated circuits
• Transistors – physical aspects that define performance and parasitics
• Passive components – resistors, capacitors and inductors define gains and time constants of circuit performance
• Parasitic components used as components (BJT)
• Latchup and ESD considerations

Key Focus

The design of analog integrated circuits is a co-design process between electrical and physical. Better understanding of the technology will allow the circuit objectives of a design to be better achieved.