

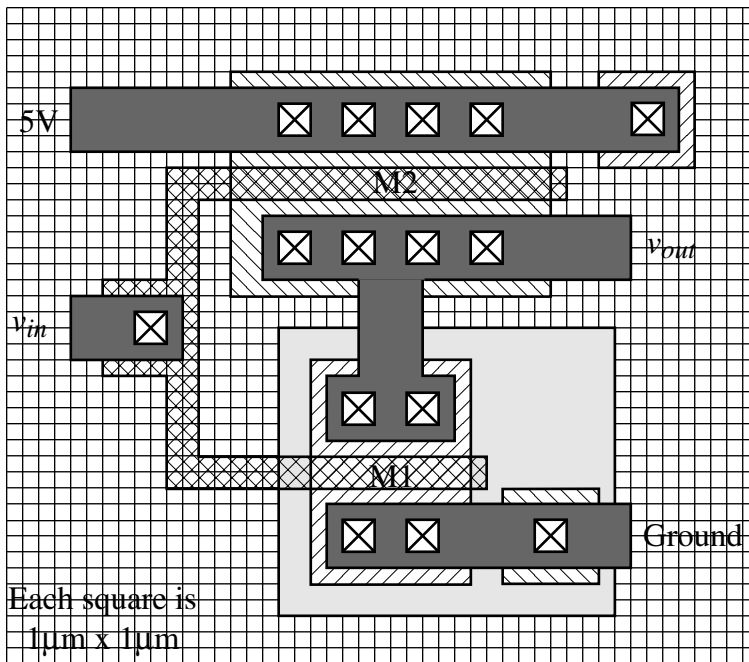
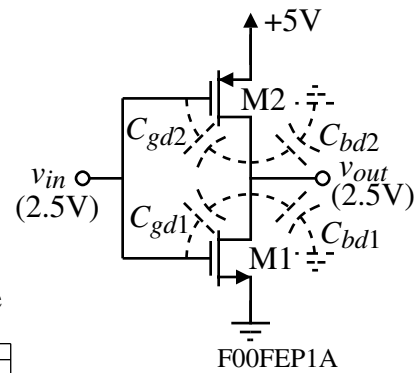
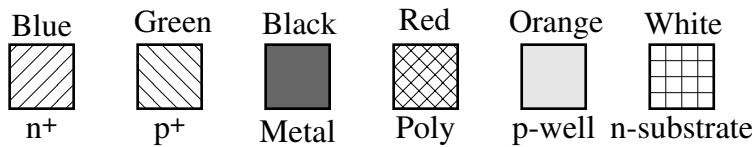
Problems – Day 1

1.) A CMOS amplifier is shown along with the top view of the circuit layout assuming a p-well CMOS technology. (a.) Find the values of the capacitors shown in the circuit if

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m ²
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Based on an oxide thickness of 140 \AA or $C_{ox}=24.7 \times 10^{-4} \text{ F/m}^2$.

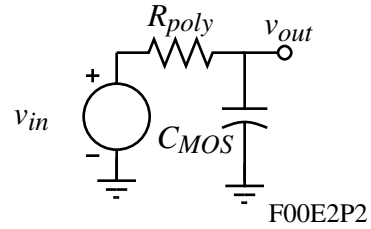
(b.) Find the approximate resistance from the sources of M1 and M2 to ground and +5V if the n⁺ diffusion is $35\Omega/\text{sq.}$, the p⁺ diffusion is $80\Omega/\text{sq.}$, and the contact resistance is 4Ω .



F00FEP1B

Answers: $C_{gd1} = 2.2\text{fF}$, $C_{gd2} = 4.4\text{fF}$, $C_{bd1} = 29.84\text{fF}$, $C_{bd2} = 42.12\text{fF}$, and $R_{S1} \approx R_{S2} \approx 9\Omega$

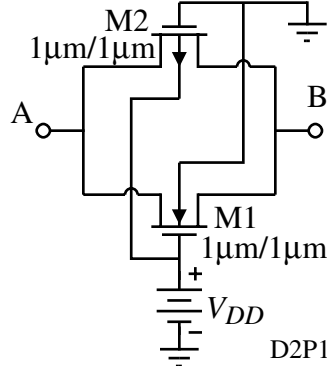
2.) A simple first-order filter shown is to be built with a polysilicon resistor and a MOS capacitor. The polysilicon resistor has a sheet resistance of $50\Omega/\text{sq.} \pm 30\%$ and is $5\mu\text{m}$ wide. The MOS capacitor is $2\text{fF}/\mu\text{m}^2 \pm 10\%$. The -3dB frequency of the lowpass filter is 1MHz. (a.) Choose the size of the resistor (the number of squares, N) to minimize the total area of the filter including both the resistor and the capacitor. Find the area of the resistor and the capacitor in μm^2 . (b.) Using the worst-case tolerance of the resistor and capacitor, find the maximum and minimum -3dB frequencies.



Answers: $A_R = 252 \times 25 \mu\text{m}^2 = 6308 \mu\text{m}^2$ and $A_C = 6308 \mu\text{m}^2$, $R_{poly} = 12.6 \text{k}\Omega$, $C_{MOS} = 12.6 \text{pF}$ and the max. -3dB frequency is 1.6MHz and the min. -3dB frequency is 0.7MHz.

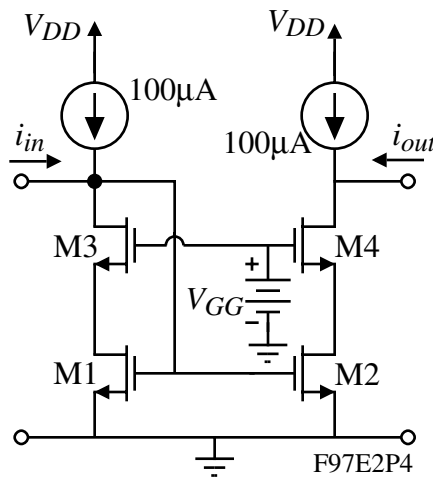
Problems – Day 2

1.) A transmission gate is shown. If $V_{DD} = 2V$, what is the highest possible large signal ON resistance of the transmission gate. Ignore the bulk effects and assume that $v_{DS} \approx 0V$.



Answers: $R_{ON(max)} = 33.3k\Omega$ at $V_{AB} = 1.3V$

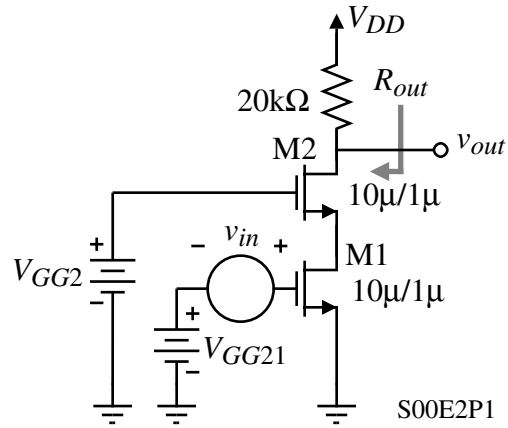
2.) (a.) If all W/Ls are 100, find the value of V_{GG} that will give a minimum value of V_{MIN} .
 (b.) Find the small signal values of R_{in} , R_{out} , and i_{out}/i_{in} .



Answers: $R_{out} \approx g_{m4}r_{ds4}r_{ds2}$, $R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds1} + r_{ds3} + r_{g_{m3}}r_{ds3}}{1 + g_{m1}g_{m3}r_{ds1}r_{ds3} + g_{m1}r_{ds1}} \approx \frac{1}{g_{m1}}$, $i_{out}/i_{in} \approx 1$
 $R_{in} \approx \frac{1}{g_{m1}} = \frac{1}{1.48mS} = 674\Omega$ $R_{out} \approx 250k\Omega(1.48mS)250k\Omega = 92.5M\Omega$ and $\frac{i_{out}}{i_{in}} = 1$

Problems - Day 3

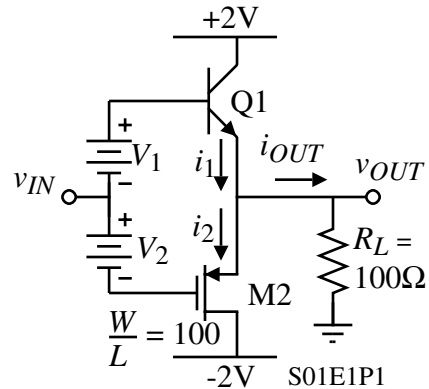
1.) A MOS cascode amplifier is shown below. Assume all transistors are saturated and the $K_N' = 110\mu\text{A}/\text{V}^2$, $V_T = 0.7\text{V}$, and $\lambda_N = 0.04\text{V}^{-1}$. The value of V_{GG1} gives a dc bias current in both transistors of $100\mu\text{A}$. (a.) Find the value of V_{GG2} which gives a minimum output voltage (same as $V_{MIN}(\text{out})$ for current sinks). What is the value of minimum output voltage? (b.) Find the small-signal output resistance, R_{out} . (c.) Find the small-signal voltage gain, v_{out}/v_{in} .



Answers: $V_{GG2} = 2V_{ON} + V_T = 1.553\text{V}$, $V_{MIN} = 2V_{ON} = 2 \cdot 0.4264 = 0.8528\text{V}$,

$$R_{out} = 20\text{k}\Omega \parallel 29.3\text{M}\Omega \approx 20\text{k}\Omega \text{ and } \frac{v_{out}}{v_{in}} = -g_m R_{out} = -(469\mu\text{S})(0.02\text{M}\Omega) = -9.38\text{V}/\text{V}$$

2.) A push-pull follower is shown which uses an NPN BJT and a p-channel MOSFET. In this problem, ignore the bulk effect, the channel length modulation, and the Early voltage. The parameters for the NPN BJT are $\beta_F = 100$, $I_s = 10\text{fA}$ and $V_t = 25.9\text{mV}$. The model parameters for the PMOS are $K_P' = 50\mu\text{A}/\text{V}^2$ and $V_{TP} = -0.7\text{V}$. (a.) Find the value of the dc batteries, V_1 and V_2 , which will cause $100\mu\text{A}$ to flow in Q1 and M2 when the dc value of $v_{IN} = 0\text{VDC}$. (b.) Find the small-signal input resistance, output resistance (not including R_L) and voltage gain when the dc value of $v_{IN} = 0\text{VDC}$.

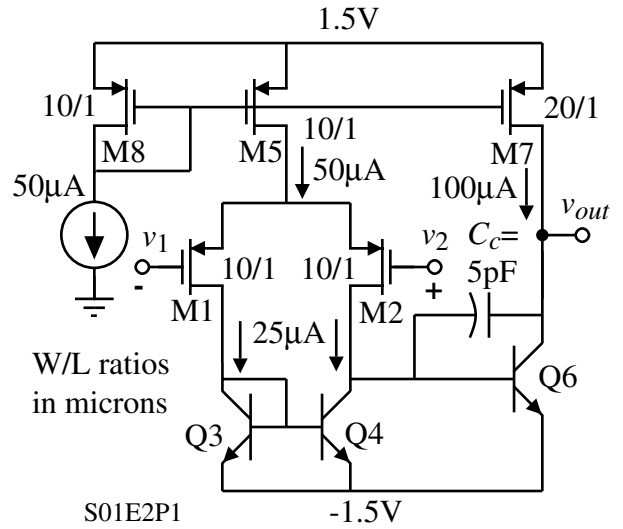


Answers: $V_1 = 0.5964\text{V}$, $V_2 = 0.9\text{V}$, $R_{in} = 38.875\text{k}\Omega$, $R_{out} = 205.8\Omega$ and

$$\frac{v_{out}}{v_{in}} = 0.3271\text{V}/\text{V}$$

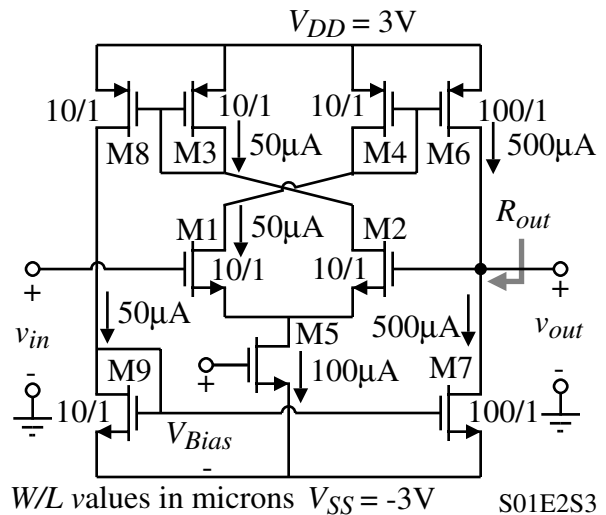
Problems - Day 4

1.) A two-stage, BiCMOS op amp is shown. For the PMOS transistors, the model parameters are $K_P' = 50\mu\text{A}/\text{V}^2$, $V_{TP} = -0.7\text{V}$ and $\lambda_P = 0.05\text{V}^{-1}$. For the NPN BJTs, the model parameters are $\beta_F = 100$, $V_{CE}(\text{sat}) = 0.2\text{V}$, $V_A = 25\text{V}$, $V_t = 26\text{mV}$, $I_s = 10\text{fA}$ and $n=1$. (a.) Identify which input is positive and which input is negative. (b.) Find the numerical values of differential voltage gain magnitude, $|A_v(0)|$, GB (in Hertz), the slew rate, SR , and the location of the RHP zero. (c.) Find the numerical value of the maximum and minimum input common mode voltages.



Answers: $|A_v(0)| = 1,659.6\text{V}/\text{V}$, $GB = 5.03265\text{MHz}$, $SR = 10\text{V}/\mu\text{s}$, $\text{RHP} = 122\text{MHz}$, $v_{icm}^+ = 0.0367\text{V}$, and $v_{icm}^- = -1.6374\text{V}$

2.) A CMOS circuit used as an output buffer for an OTA is shown. Find the value of the small signal output resistance, R_{out} , and from this value estimate the -3dB bandwidth if a 50pF capacitor is attached to the output. What is the maximum and minimum output voltage if a 1kΩ resistor is attached to the output? What is the quiescent power dissipation of this circuit? Use the following model parameters: $K_N' = 110\mu\text{A}/\text{V}^2$, $K_P' = 50\mu\text{A}/\text{V}^2$, $V_{TN} = -V_{TP} = 0.7\text{V}$, $\lambda_N = 0.04\text{V}^{-1}$ and $\lambda_P = 0.05\text{V}^{-1}$.

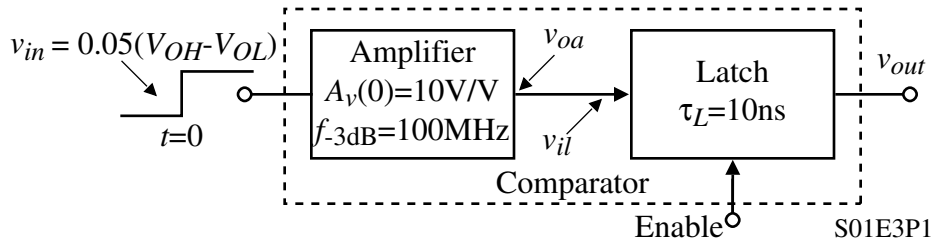


Answers:

W1=W2	W3=W4=W6 =W7=W8	W9=W10 =W11	W5	$I_5(\mu\text{A})$	A_{vd}	V_{BP}	V_{BN}	P_{diss}
89.75	40	18.2	11.07	250µA	17,338V/V	3.3V	1.7V	2.5mW

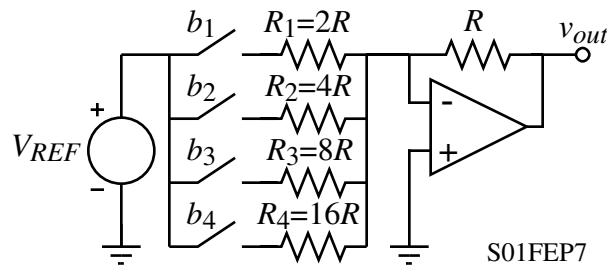
Problems - Day 5

1.) A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has a voltage gain of $10V/V$ and $f_{-3dB} = 100MHz$ and the latch has a time constant of $10ns$. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL} . When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH}-V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may be useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2v_{il}}\right)$ where v_{il} is the latch input (ΔV_i of the text).



Answer: $t_p = 4.637ns$.

2.) A 4-bit, binary-weighted, resistor DAC is shown. (a.) Assume that $GB = \infty$ and find the minimum differential gain, $A_{vd}(0)$, required for the DAC to have an INL of $\pm 0.5LSB$. (b.) If the differential gain is very large, find the conversion time of this DAC if $GB = 1MHz$.



Answer: (a) $A \geq 56.2V/V$ (b) $T = 1.0488\mu s$