CHAPTER 3 - CMOS MODELS

Chapter Outline

3.1 MOS Structure and Operation
3.2 Large signal MOS models suitable for hand calculations
3.3 Extensions of the large signal MOS model
3.4 Capacitances of the MOSFET
3.5 Small Signal MOS models
3.6 Temperature and noise models for MOS transistors
3.7 BJT models
3.8 SPICE level 2 model
3.9 Models for simulation of MOS circuits
3.10 Extraction of a large signal model for hand calculations from the BSIM3 model
3.11 Summary

Perspective

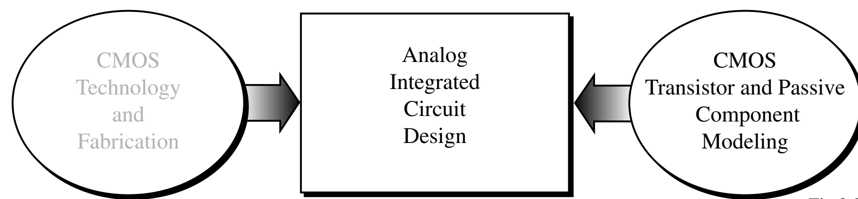


Fig.3.0-1

Philosophy for Models Suitable for Analog Design

The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

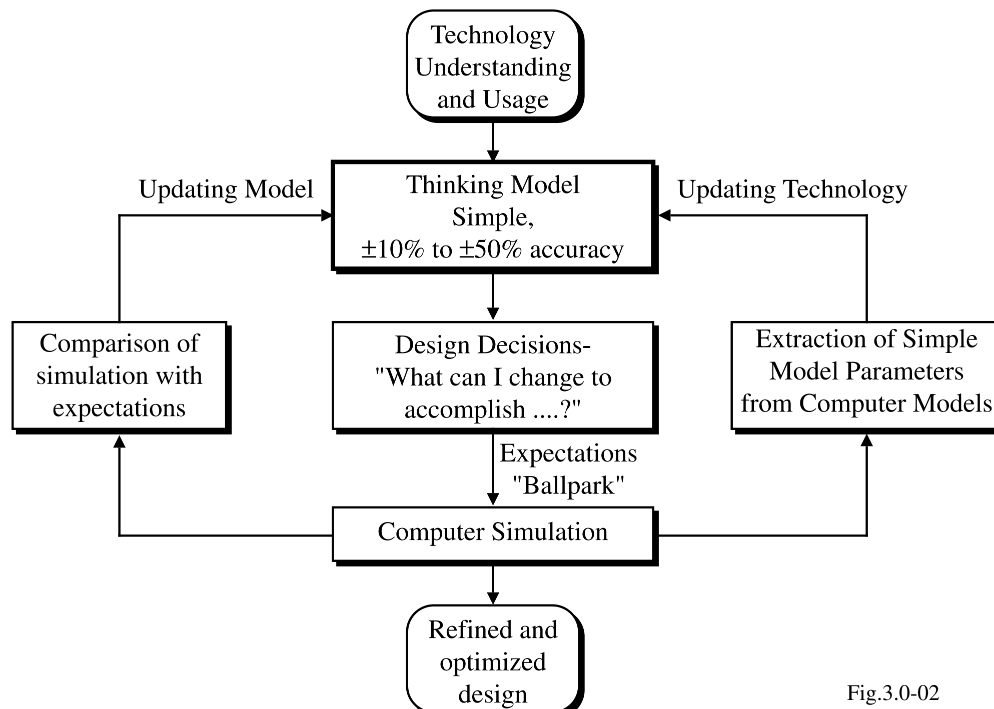


Fig.3.0-02

This chapter is devoted to the simple model suitable for design *not* using simulation.

Categorization of Electrical Models

		Time Dependence	
		Time Independent	Time Dependent
Linearity	Linear	Small-signal, midband R_{in}, A_v, R_{out} (.TF)	Small-signal frequency response-poles and zeros (.AC)
	Nonlinear	DC operating point $i_D = f(v_D,v_G,v_S,v_B)$ (.OP)	Large-signal transient response - Slew rate (.TRAN)

Based on the simulation capabilities of SPICE.

3.1 - MOS STRUCTURE AND OPERATION

Metal-Oxide-Semiconductor Structure

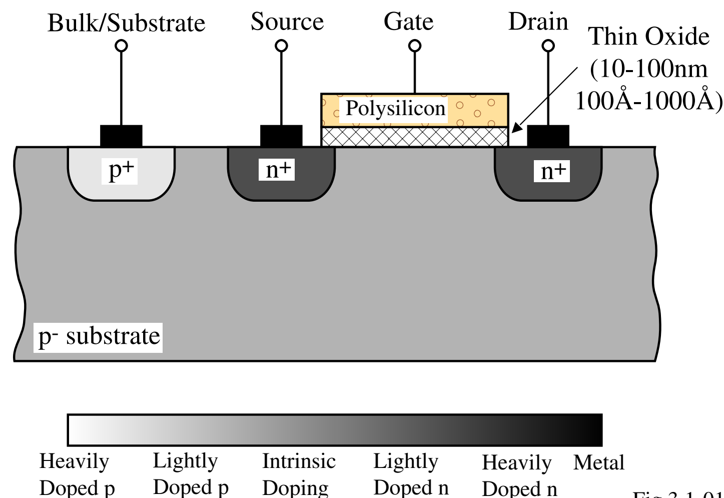


Fig.3.1-01

Terminals:

- Bulk - Used to make an ohmic contact to the substrate
- Gate - The gate voltage is applied in such a manner as to invert the doping of the material directly beneath the gate to form a channel between the source and drain.
- Source - Source of the carriers flowing in the channel
- Drain - Collects the carriers flowing in the channel

Formation of the Channel for an Enhancement MOS Transistor

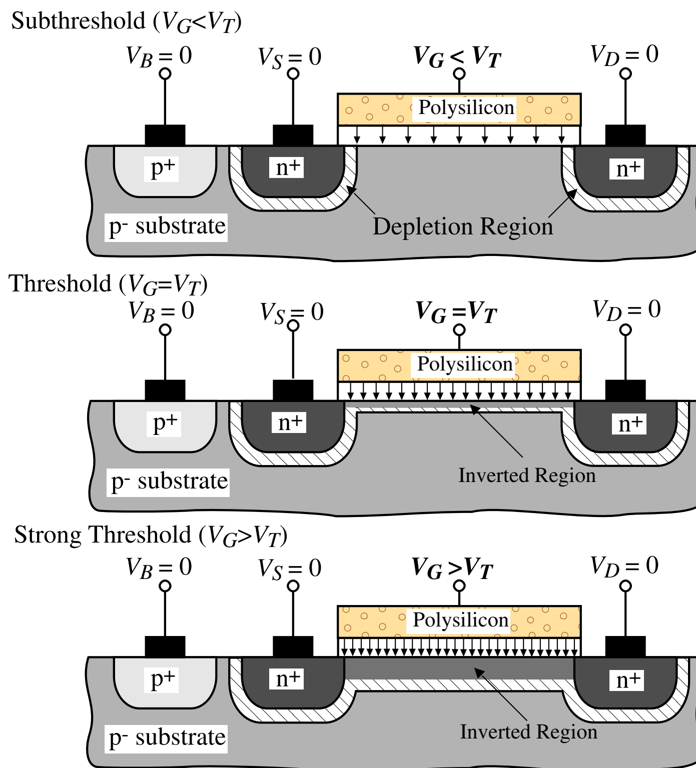


Fig.3.1-02

Transconductance Characteristics of an Enhancement NMOS FET when V_{DS} = 0.1V

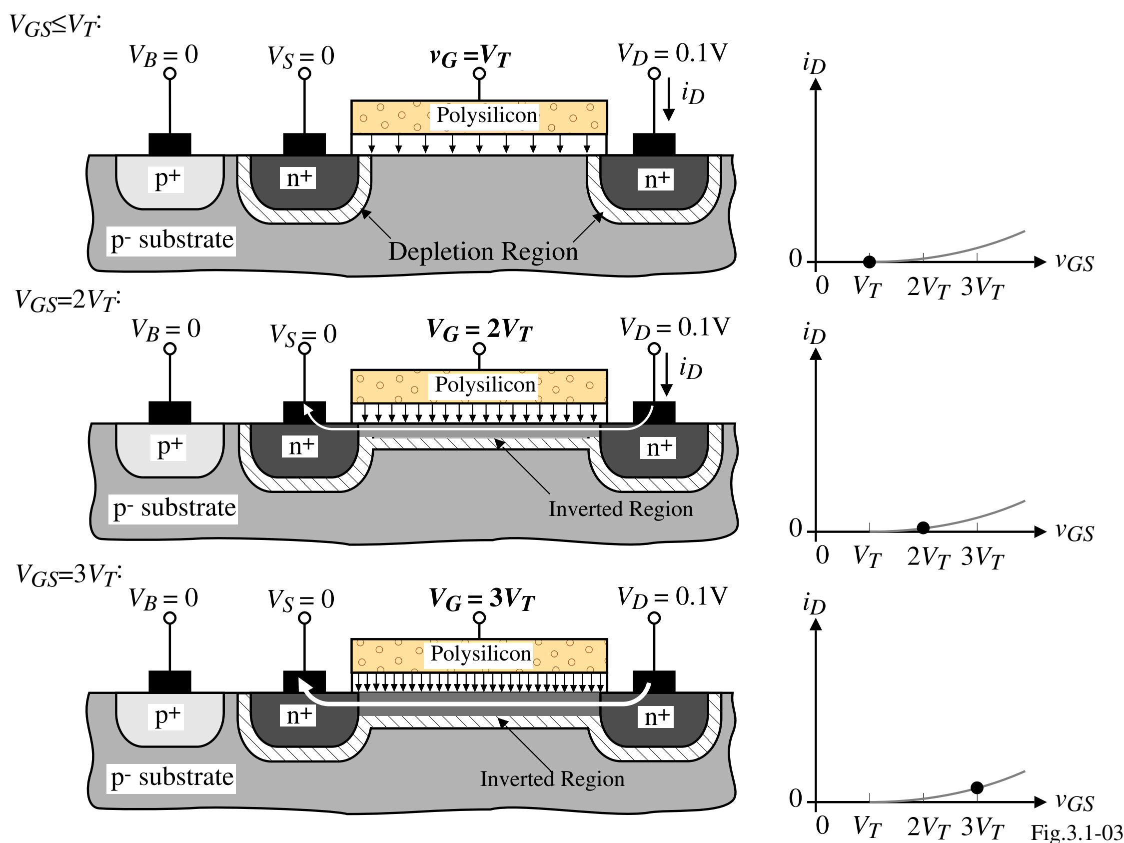
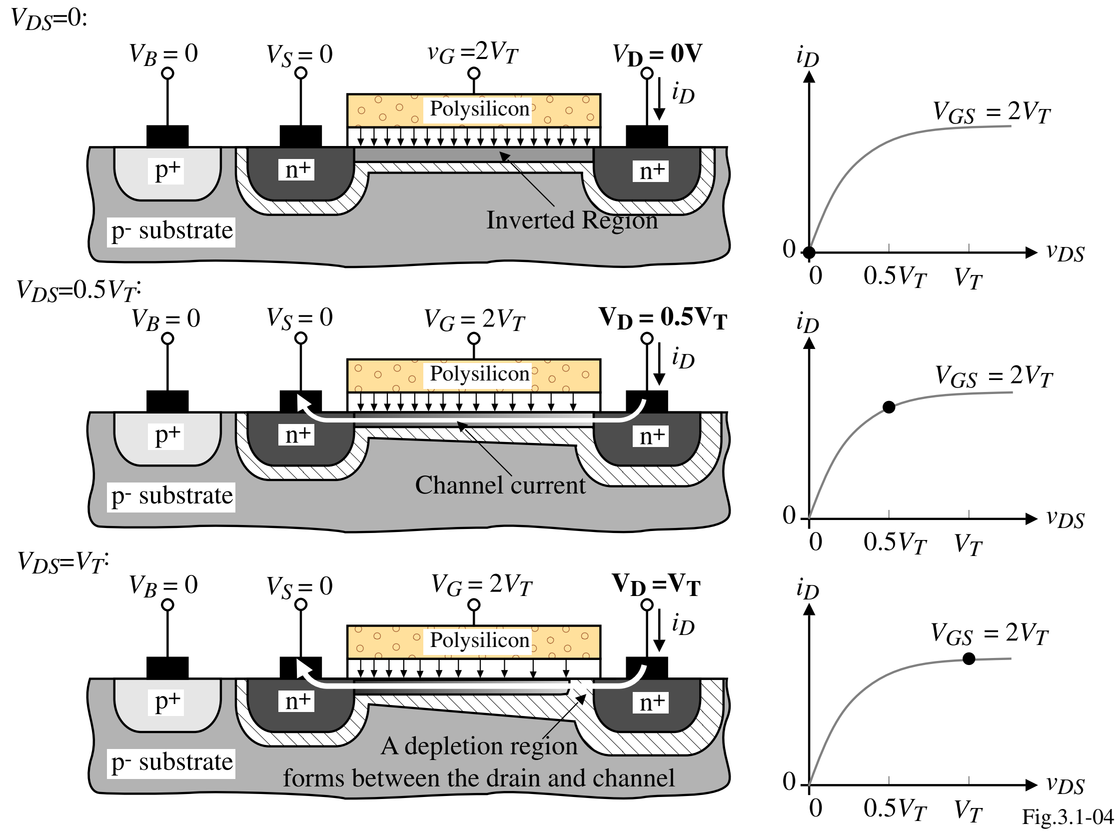
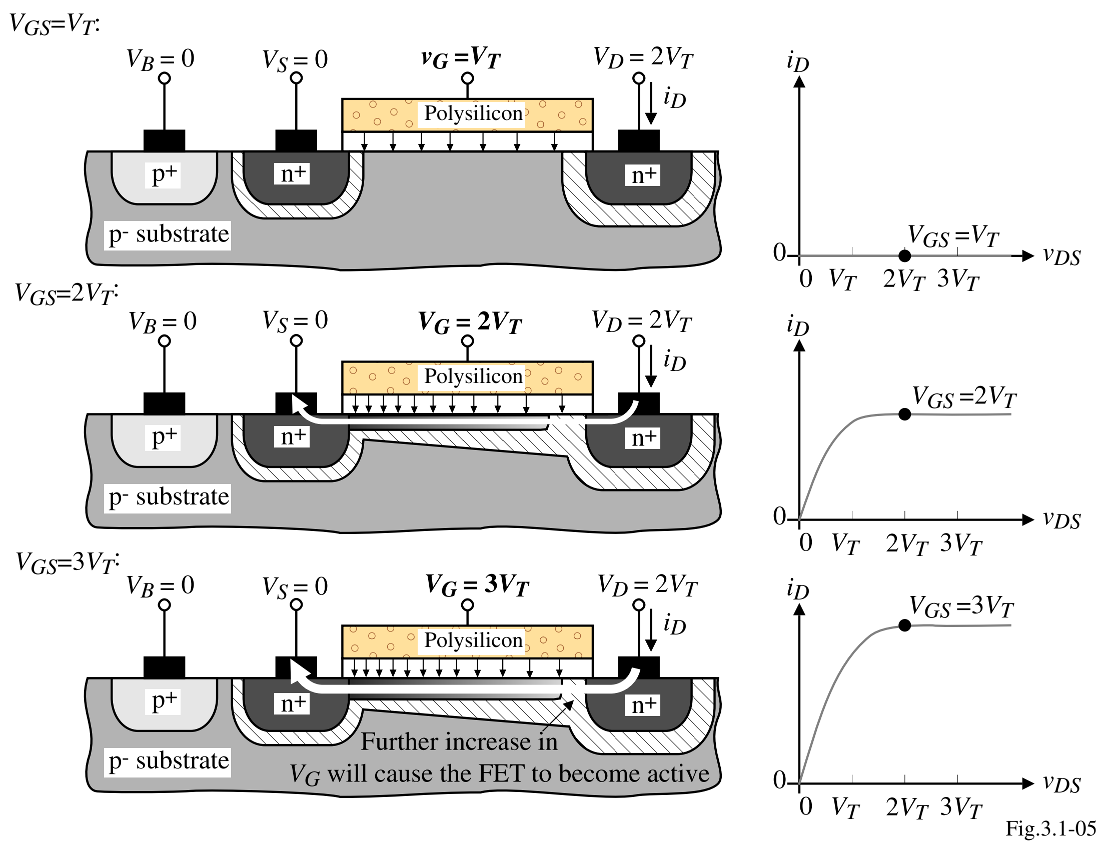


Fig.3.1-03

Output Characteristics of the Enhancement NMOS Transistor for $V_{GS} = 2V_T$



Output Characteristics of the Enhanced NMOS when $v_{DS} = 2V_T$



Output Characteristics of an Enhancement NMOS Transistor

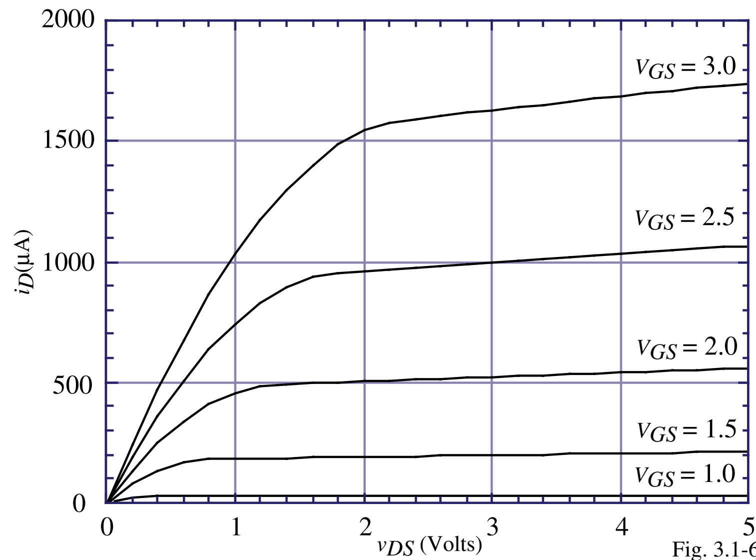


Fig. 3.1-6

SPICE Input File:

```
Output Characteristics for NMOS
M1 6 1 0 0 MOS1 w=5u l=1.0u
VGS1 1 0 1.0
M2 6 2 0 0 MOS1 w=5u l=1.0u
VGS2 2 0 1.5
M3 6 3 0 0 MOS1 w=5u l=1.0u
VGS3 3 0 2.0
M4 6 4 0 0 MOS1 w=5u l=1.0u
VGS4 4 0 2.5
M5 6 5 0 0 MOS1 w=5u l=1.0u
VGS5 5 0 3.0
VDS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 +lambda=.04 phi=.7)
.dc vds 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.end
```


Transconductance Characteristics of an Enhancement NMOS Transistor

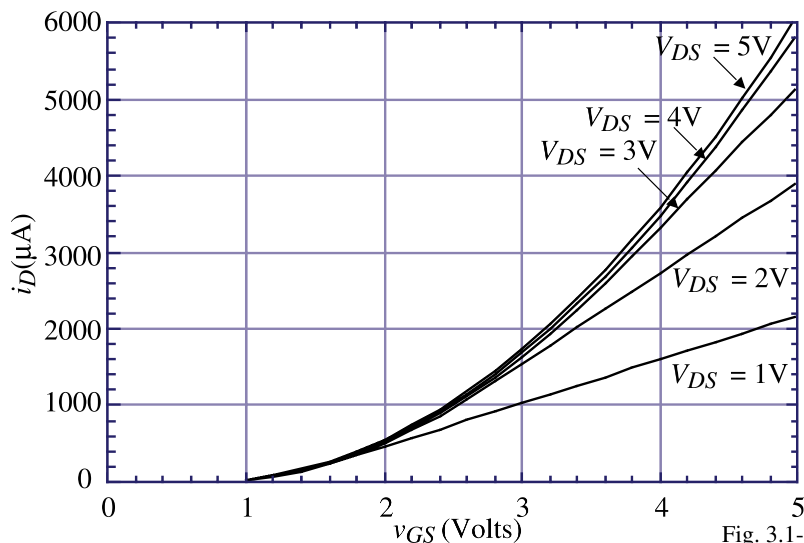


Fig. 3.1-7

SPICE Input File:

```
Transconductance Characteristics for NMOS
M1 1 6 0 0 MOS1 w=5u l=1.0u
VDS1 1 0 1.0
M2 2 6 0 0 MOS1 w=5u l=1.0u
VDS2 2 0 2.0
M3 3 6 0 0 MOS1 w=5u l=1.0u
VDS3 3 0 3.0
M4 4 6 0 0 MOS1 w=5u l=1.0u
VDS4 4 0 4.0
M5 5 6 0 0 MOS1 w=5u l=1.0u
VDS5 5 0 5.0
VGS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 lambda=.04 phi=.7)
.dc vgs 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.probe
.end
```

3.2 - LARGE SIGNAL FET MODEL FOR HAND CALCULATIONS

Large Signal Model Derivation

Derivation-

1.) Let the charge per unit area in the channel inversion layer be

$$Q_I(y) = -C_{ox}[v_{GS}-v(y)-V_T] \quad \text{(coul./cm}^2\text{)}$$

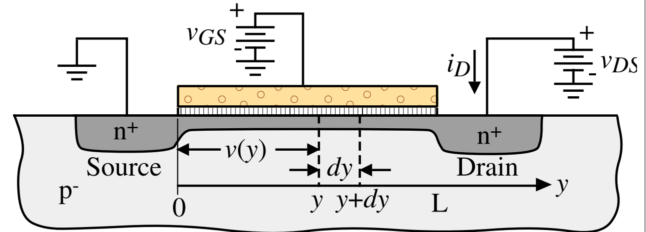


Fig.110-03

2.) Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_I(y) \left(\frac{\text{cm}^2}{\text{v}\cdot\text{s}}\right)\left(\frac{\text{coulombs}}{\text{cm}^2}\right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

3.) Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \rightarrow \quad dv = \frac{-i_D}{\sigma_S W}\, dy = \frac{-i_D dy}{\mu_o Q_I(y) W} \rightarrow \quad i_D\, dy = -W\mu_o Q_I(y) dv$$

4.) Integrating along the channel for 0 to L gives

$$\int_0^L i_D dy = -\int_0^{v_{DS}} W\mu_o Q_I(y) dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS}-v(y)-V_T]\, dv$$

5.) Evaluating the limits gives

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - \frac{v^2(y)}{2}\right]_0^{v_{DS}} \rightarrow \quad \boxed{i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - \frac{v_{DS}^2}{2}\right]}$$

Saturation Voltage - V_{DS}(sat)

Interpretation of the large signal model:

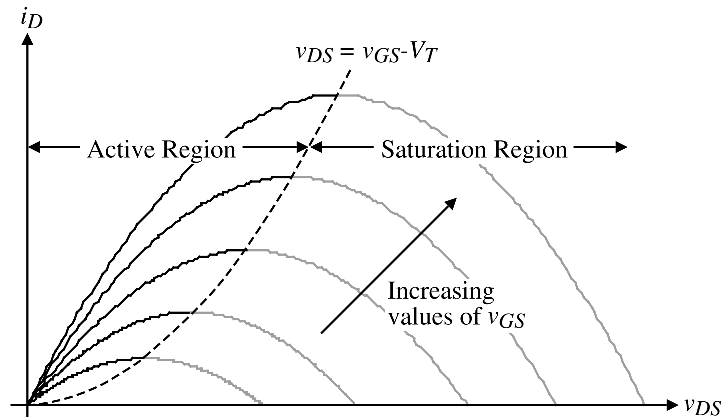


Fig. 110-04

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

$$\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L}[(v_{GS}-V_T) - v_{DS}] = 0$$

$$\boxed{v_{DS}(\text{sat}) = v_{GS} - V_T}$$

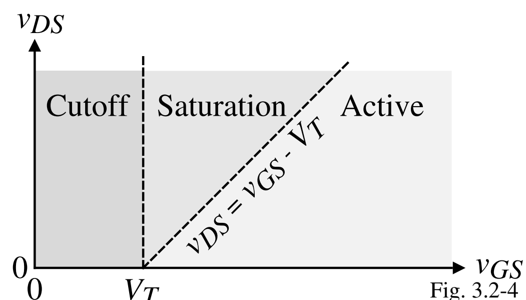


Fig. 3.2-4

Useful definitions:

$$\frac{\mu_o C_{ox} W}{L} = \frac{K'W}{L} = \beta$$

The Simple Large Signal MOSFET Model

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

$v_{GS} - V_T < 0$

$i_D = 0$

(Ignores subthreshold currents)

2.) Active Region

$0 < v_{DS} < v_{GS} - V_T$

$$i_D = \frac{\mu_o C_{ox} W}{2L}[2(v_{GS} - V_T) - v_{DS}]\ v_{DS}$$

3.) Saturation Region

$0 < v_{GS} - V_T < v_{DS}$

$$i_D = \frac{\mu_o C_{ox} W}{2L}(v_{GS} - V_T)^2$$

Output Characteristics of the MOSFET:

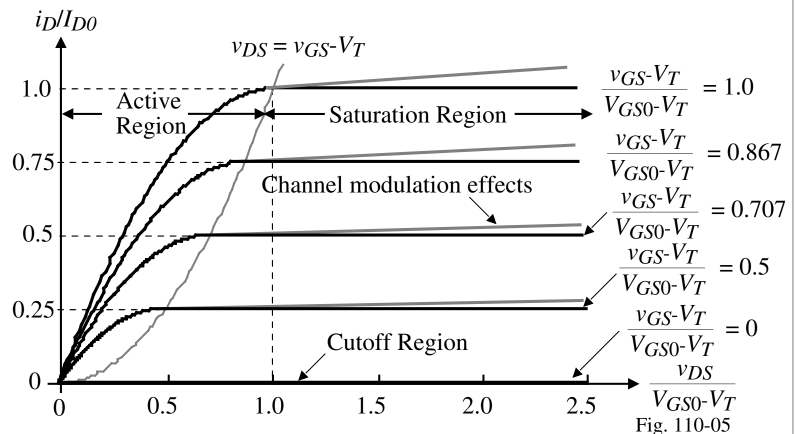
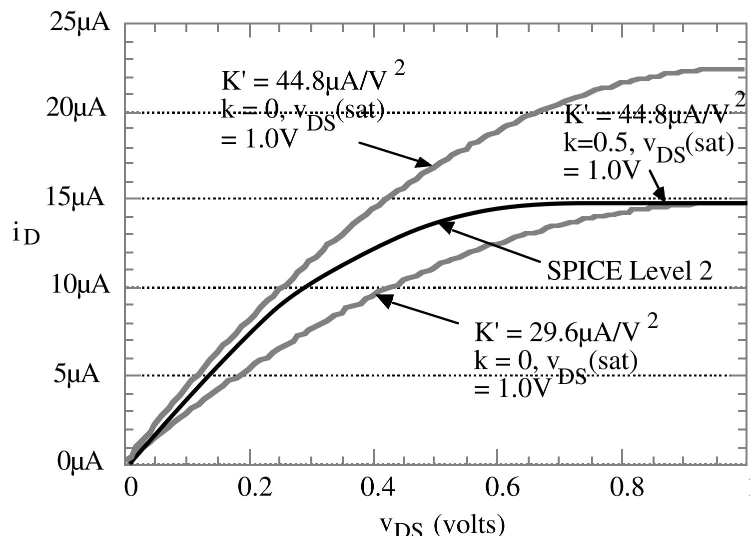


Illustration of the Need to Account for the Influence of v_{DS} on the Simple Sah Model

Compare the Simple Sah model to SPICE level 2:



V_{GS} = 2.0V, W/L = 100µm/100µm, and no mobility effects.

Modification of the Previous Model to Include the Effects of v_{DS} on V_T

From the previous derivation:

$$\int_0^L i_D\,dy = -\int_0^{v_{DS}} W\mu_o Q_I(y)dv = \int_0^{v_{DS}} W\mu_o C_{ox}[v_{GS} - v(y) - V_T]dv$$

Assume that the threshold voltage varies across the channel in the following way:

$$V_T(y) = V_T + kv(y)$$

where V_T is the value of V_T the at the source end of the channel and k is a constant.

Integrating the above gives,

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v(y) - (1+k)\frac{v^2(y)}{2}\right]_0^{v_{DS}}$$

or

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS} - (1+k)\frac{v^2_{DS}}{2}\right]$$

To find v_{DS}(sat), set the di_D/dv_{DS} equal to zero and solve for $v_{DS} = v_{DS}$(sat),

$$v_{DS}(\text{sat}) = \frac{v_{GS} - V_T}{1 + k}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W\mu_o C_{ox}}{2(1+k)L}(v_{GS} - V_T)^2$$

For $k = 0.5$ and $K' = 44.8\mu A/V^2$, excellent correlation is achieved with SPICE 2.

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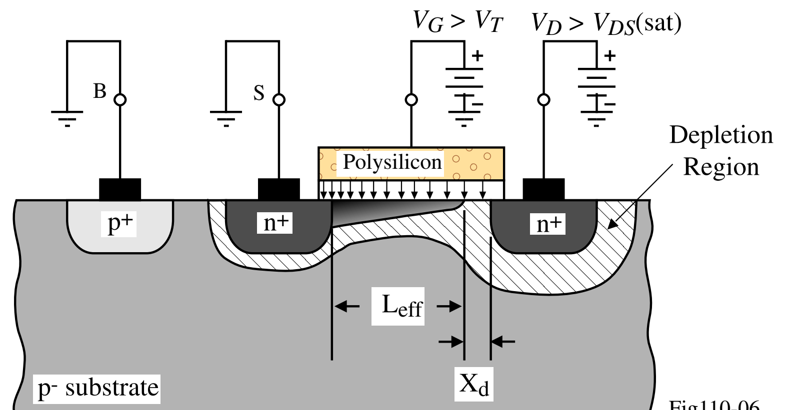
Influence of V_{DS} on the Output Characteristics

Channel modulation effect:

As the value of v_{DS} increases, the effective L decreases causing the current to increase.

Illustration:



Note that $L_{\text{eff}} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{\text{eff}}}(v_{GS}-V_T)^2 \rightarrow \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{\text{eff}}^2}(v_{GS} - V_T)^2\frac{dL_{\text{eff}}}{dv_{DS}} = \frac{i_D}{L_{\text{eff}}}\frac{dX_d}{dv_{DS}} \equiv \lambda i_D$$

Therefore, a good approximation to the influence of v_{DS} on i_D is

$$i_D \approx i_D(\lambda = 0) + \frac{di_D}{dv_{DS}}v_{DS} = i_D(\lambda = 0)(1 + \lambda v_D) = \frac{K'W}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

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Channel Length Modulation Parameter, λ

Assume the MOS is transistor is saturated-

$$\therefore\ i_D = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

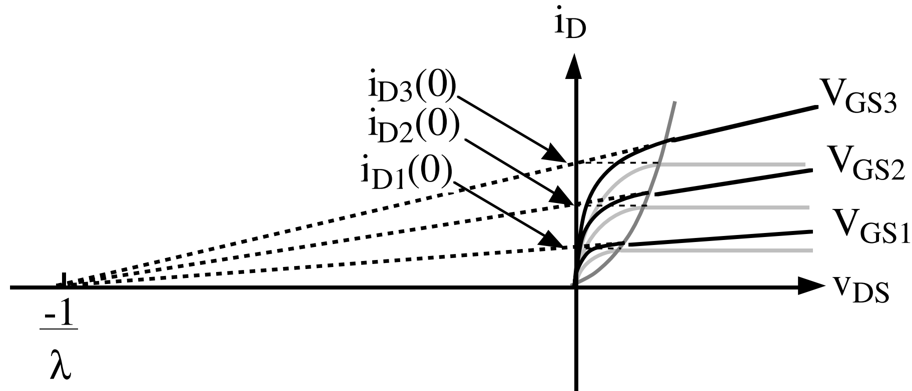
Define $i_D(0) = i_D$ when $v_{DS} = 0\text{V}$.

$$\therefore\ i_D(0) = \frac{\mu C_{ox} W}{2L}(v_{GS} - V_T)^2$$

Now,

$$i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0)\, v_{DS}$$

Matching with $y = mx + b$ gives the value of λ



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Influence of the Bulk Voltage on the Large Signal MOSFET Model

Illustration of the influence of the bulk:

$V_{SB0} = 0\text{V}$:

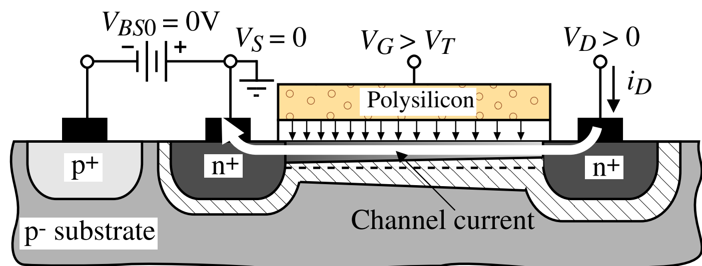

Fig.110-07A

$V_{SB1} > 0\text{V}$:

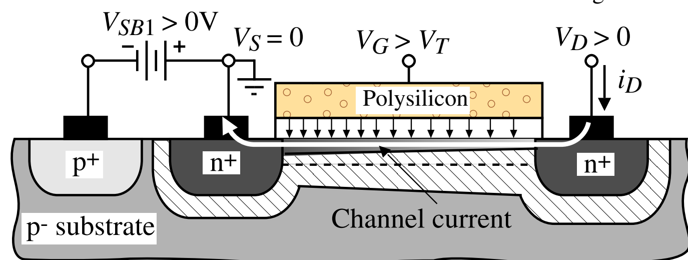

Fig.110-07B

$V_{SB2} > V_{SB1}$:

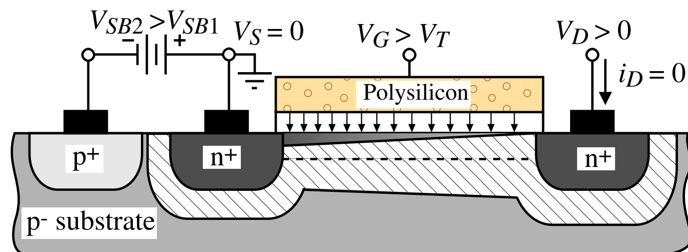

Fig.110-07C

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Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source (v_{BS}) influence on the transconductance characteristics-

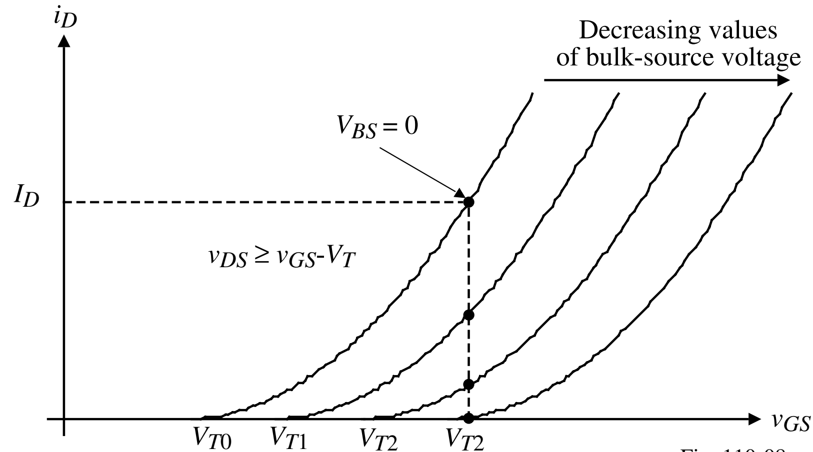

Fig. 110-08

In general, the simple model incorporates the bulk effect into V_T by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma\sqrt{2|\phi_f| + |v_{BS}|} - \gamma\sqrt{2|\phi_f|}$$

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Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

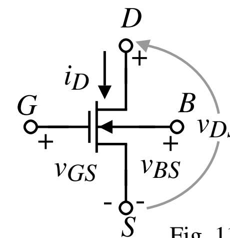

Fig. 110-10

Non-saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_o C_{ox}}{L}\left[(v_{GS}-V_T)v_{DS}(\text{sat}) - \frac{v_{DS}(\text{sat})^2}{2}\right](1+\lambda v_{DS}) = \frac{W\mu_o C_{ox}}{2L}(v_{GS}-V_T)^2(1+\lambda v_{DS})$$

where:

μ_o = zero field mobility (cm^2/volt·sec)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ = channel-length modulation parameter (volts^{-1})

$V_T = V_{T0} + \gamma\left(\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|}\right)$

V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter (volts$^{-0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert current.

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Silicon Constants

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_0	Permittivity of free space	8.854×10^{-14}	F/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

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MOSFET Parameters

Model Parameters for a Typical CMOS Bulk Process (0.8µm CMOS n-well):

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	Typical Parameter Value P-Channel	Units
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.7± 0.15	-0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	110.0 ± 10%	50.0 ± 10%	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$(V)^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L=1 μm) 0.01 (L=2 μm)	$(V)^{-1}$
$2\|\phi_F\|$	Surface potential at strong inversion	0.7	0.8	V

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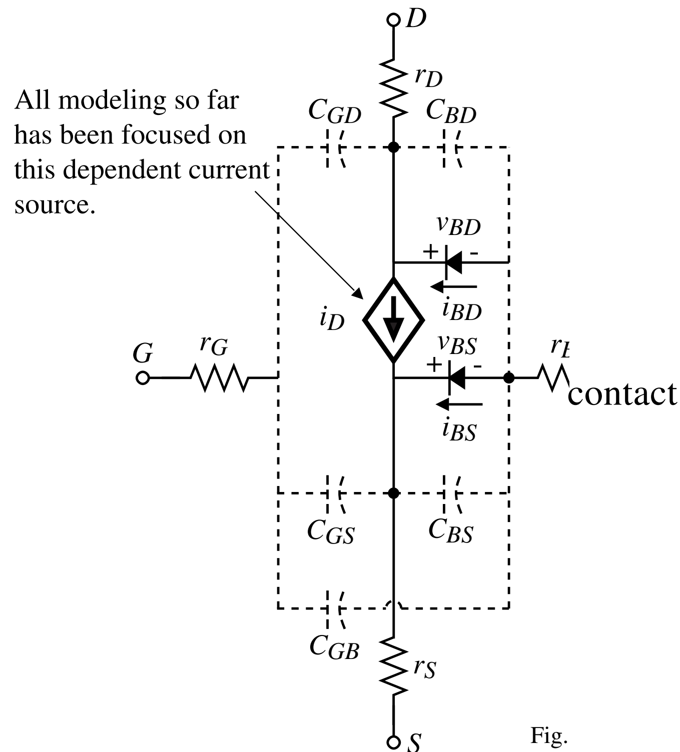
Large Signal Model of the MOS Transistor

Schematic:



where,

r_G, r_S, r_B, and r_D are ohmic and contact resistances

and

$$i_{BD} = I_s\left[exp\left(\frac{v_{BD}}{V_t}\right) - 1\right]$$

and

$$i_{BS} = I_s\left[exp\left(\frac{v_{BS}}{V_t}\right) - 1\right]$$

3.3 - LARGE SIGNAL MODEL EXTENSIONS TO SHORT-CHANNEL MOSFETS

Extensions

- Velocity saturation
- Weak inversion (subthreshold)
- Substrate currents

Substrate Interference

- Problems of mixed signal circuits on the same substrate
- Modeling and potential solutions

VELOCITY SATURATION

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

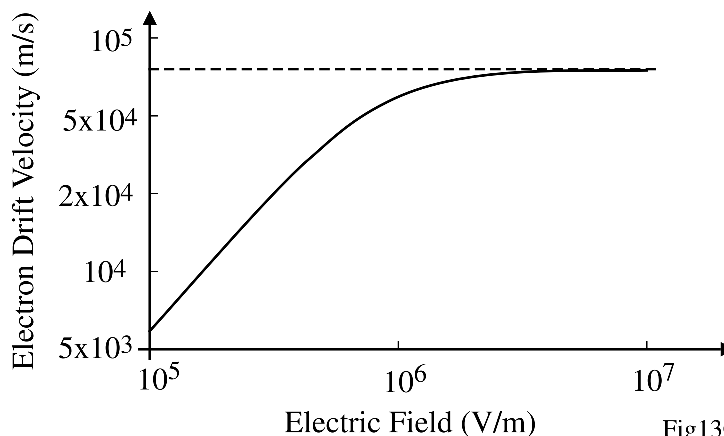


Fig130-1

An expression for the electron drift velocity as a function of the electric field is,

$$v_d \approx \frac{\mu_n E}{1 + E/E_c}$$

where

v_d = electron drift velocity (m/s)

μ_n = low-field mobility ($\approx 0.07 m^2/V \cdot s$)

E_c = critical electrical field at which velocity saturation occurs

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Short-Channel Model Derivation

As before,

$$J_D = J_S = \frac{i_D}{W} = Q_I(y)v_d(y) \rightarrow i_D = WQ_I(y)v_d(y) = \frac{WQ_I(y)\mu_n E}{1 + E/E_c} \rightarrow i_D\left(1+\frac{E}{E_c}\right) = WQ_I(y)\mu_n E$$

Replacing E by dv/dy gives,

$$i_D\left(1 + \frac{1}{E_c}\frac{dv}{dy}\right) = WQ_I(y)\mu_n\frac{dv}{dy}$$

Integrating along the channel gives,

$$\int_0^L i_D\left(1 + \frac{1}{E_c}\frac{dv}{dy}\right)dy = \int_0^{v_{DS}} WQ_I(y)\mu_n dv$$

The result of this integration is,

$$i_D = \frac{\mu_n C_{ox}}{2\left(1 + \frac{1}{E_c}\frac{v_{DS}}{L}\right)}\frac{W}{L}[2(v_{GS}-V_T)v_{DS}-v_{DS}^2] = \frac{K'}{2[1+\theta(v_{GS}-V_T)]}\frac{W}{L}[2(v_{GS}-V_T)v_{DS}-v_{DS}^2]$$

where $\theta = 1/LE_c$ with dimensions of V^{-1}.

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Saturation Voltage

Differentiating i_D with respect to v_{DS} and setting equal to zero gives,

$$\theta v_{DS}^2 + 2v_{DS} - 2(V_{GS}-V_T) = 0$$

Solving for v_{DS} gives,

$$V'_{DS}(\text{sat}) = \frac{1}{\theta}\left(\sqrt{1+2\theta(V_{GS}-V_T}-1\right) \approx (V_{GS}-V_T)\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

or

$$V'_{DS}(\text{sat}) \approx V_{DS}(\text{sat})\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

Therefore the large signal model in the saturation region is,

$$i_D = \frac{K'}{2[1+\theta(v_{GS}-V_T)]}\frac{W}{L}[v_{GS} - V_T]^2, \qquad v_{DS} \geq (V_{GS}-V_T)\left(1 - \frac{\theta(V_{GS}-V_T)}{2} + \cdots\right)$$

The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for K' = 110µA/V^2 and W/L = 1:

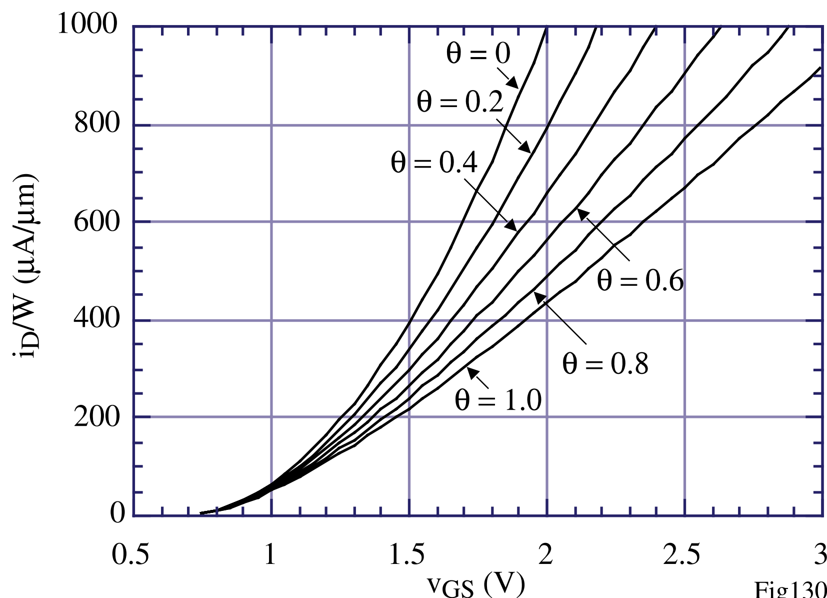

Fig130-2

Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is the following:

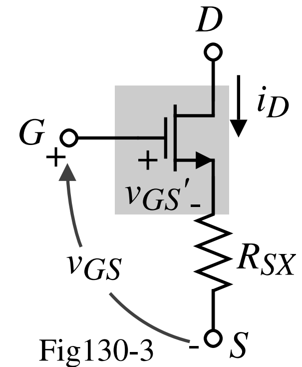

Fig130-3

We know that

$$i_D = \frac{K'W}{2L}(v_{GS}' - V_T)^2 \text{ and } \qquad v_{GS} = v_{GS}' + i_D R_{SX}$$

or

$$v_{GS}' = v_{GS} - i_D R_{XS}$$

Substituting v_{GS}' into the current relationship gives,

$$i_D = \frac{K'W}{2L}(v_{GS} - i_D R_{SX} - V_T)^2$$

Solving for i_D results in,

$$i_D = \frac{K'}{2\left[1 + K'\frac{W}{L}R_{SX}(v_{GS} - V_T)\right]}\frac{W}{L}(v_{GS} - V_T)^2$$

Comparing with the previous result, we see that

$$\theta = K'\frac{W}{L}R_{SX} \qquad \rightarrow \quad R_{SX} = \frac{\theta L}{K'W} = \frac{1}{E_c K'W}$$

Therefore for K' = 110μA/V^2, W = 1μm and E_c = 1.5x10^{6}V/m, we get R_{XS} = 6.06kΩ.

Output Characteristics of Short-Channel MOSFETs†

IBM, 1998, t_{ox} = 3.5nm

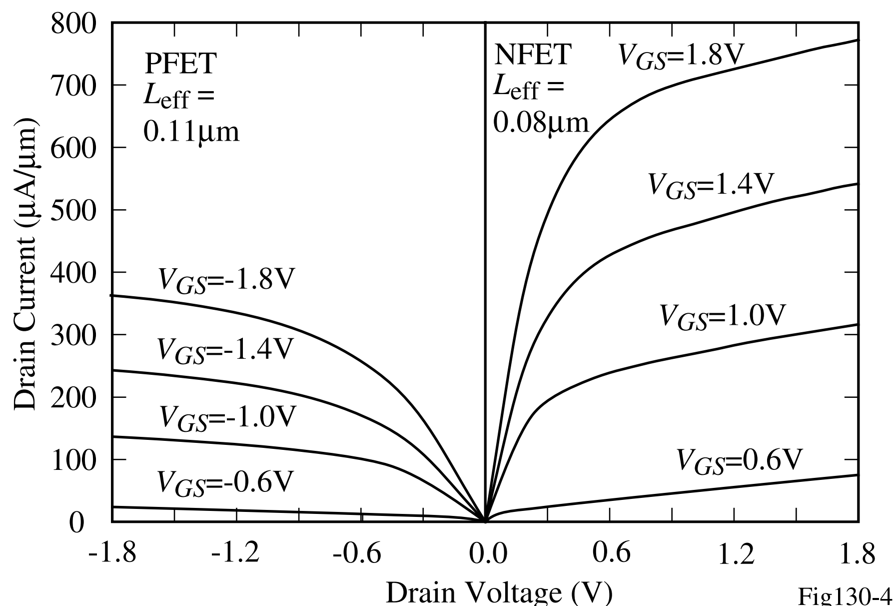

Fig130-4

† Su, L., et.al., "A High Performance Sub-0.25μm CMOS Technology with Multiple Thresholds and Copper Interconnects," *1998 Symposium on VLSI Technology Digest of Technical Papers*, pp. 18-19.

Velocity Saturation Effects

Velocity Saturation Insignificant

$$g_m = K'\frac{W}{2L}(V_{GS}-V_T)$$

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}} \propto L^{-2}$$

Velocity Saturation Significant

$$g_m = WC_{ox}u_oE_c\frac{\sqrt{1+2\theta(V_{GS}-V_T)}-1}{\sqrt{1+2\theta(V_{GS}-V_T)}}$$

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}} \propto L^{-1}$$

Important Short Channel Effects

1.) An approximate plot of the n as a function of channel length is shown below where

$$i_D \propto (v_{GS} - V_T)^n$$

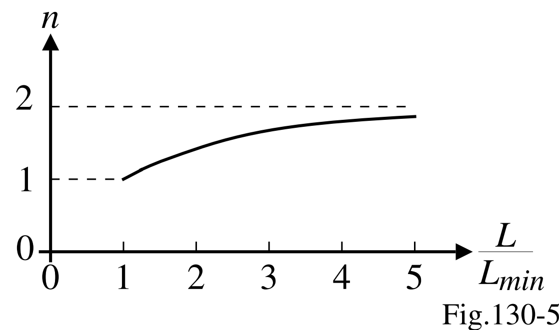

Fig.130-5

2.) Note that the value of λ varies with channel length, L. The data below is from a 0.25µm CMOS technology.

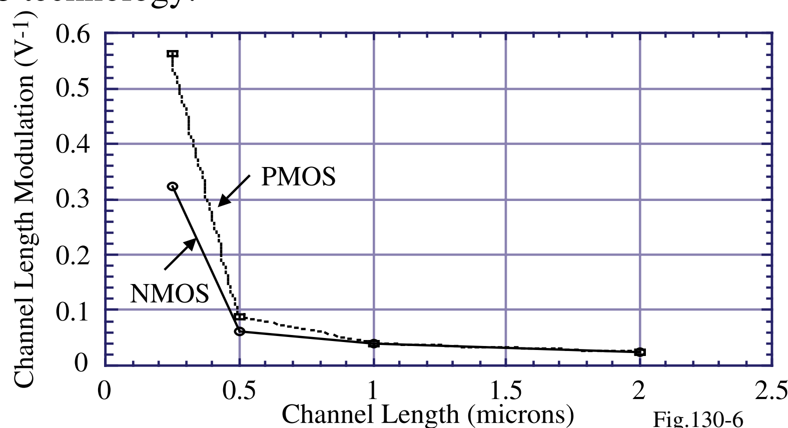

Fig.130-6

SUBTHRESHOLD MOSFET MODEL

What is Weak Inversion Operation?

Weak inversion operation occurs when the applied gate voltage is below V_T and pertains to when the surface of the substrate beneath the gate is weakly inverted.

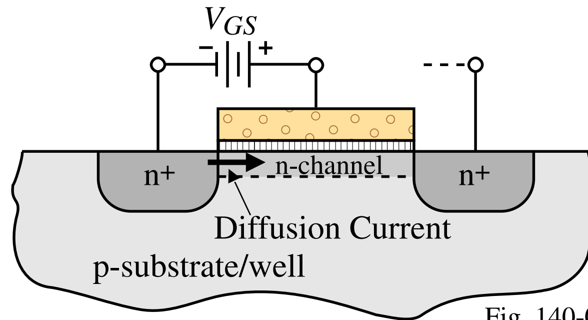

Fig. 140-01

Regions of operation according to the surface potential, ϕ_S (or ψ_S)

$\phi_S < \phi_F$:	Substrate not inverted
$\phi_F < \phi_S < 2\phi_F$:	Channel is weakly inverted (diffusion current)
$2\phi_F < \phi_S$:	Strong inversion (drift current)

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Drift versus Diffusion Current

1.) For strong inversion, the gate voltage controls the charge in the inverted region but not in the depletion region. The concentration of charge across the channel is approximately constant and the current is drift caused by electric field.

2.) For weak inversion, the charge in channel is much less that that in the depletion region and drift current decreases. However, there is a concentration gradient in the channel, that causes diffusion current.

The n-channel MOSFET acts like a NPN BJT: the emitter is the source, the base is the substrate and the collector is the drain.

Illustration:

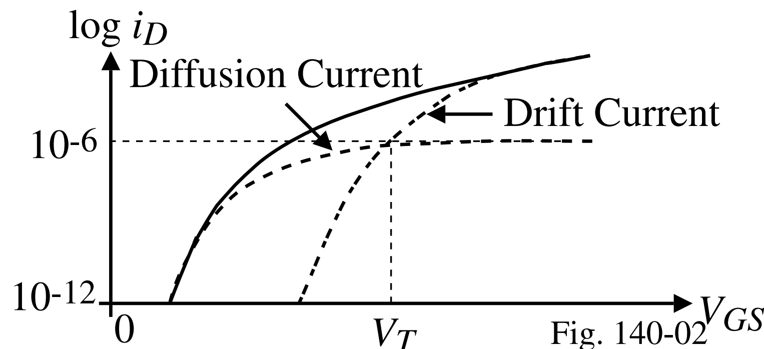

Fig. 140-02

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Large-Signal Model for Weak Inversion

The electrons in the substrate at the source side can be expressed as,

$$n_p(0) = n_{po}\exp\left(\frac{\phi_s}{V_t}\right)$$

The electrons in the substrate at the drain side can be expressed as,

$$n_p(L) = n_{po}\exp\left(\frac{\phi_s - v_{DS}}{V_t}\right)$$

Therefore, the drain current due to diffusion is,

$$i_D = qADn\left(\frac{n_p(L) - n_p(0)}{L}\right) = \frac{W}{L}\,qXD_n n_{po}\exp\left(\frac{\phi_s}{V_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

where X is the thickness of the region in which i_D flows.

In weak inversion, the changes in the surface potential, $\Delta\phi_s$ are controlled by changes in the gate-source voltage, Δv_{GS}, through a voltage divider consisting of C_{ox} and C_{js}, the depletion region capacitance.

$$\therefore\quad \frac{d\phi_s}{dv_{GS}} = \frac{C_{ox}}{C_{ox} + C_{js}} = \frac{1}{n} \quad\rightarrow\quad \phi_s = \frac{v_{GS}}{n} + k_1 = \frac{v_{GS} - V_T}{n} + k_2$$

where

$$k_2 = k_1 + \frac{V_T}{n}$$

Large-Signal Model for Weak Inversion – Continued

Substituting the above relationships back into the expression for i_D gives,

$$i_D = \frac{W}{L}\,qXD_n n_{po}\exp\left(\frac{k_2}{V_t}\right)\exp\left(\frac{v_{GS} - V_T}{nV_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

Define I_t as

$$I_t = qXD_n n_{po}\exp\left(\frac{k_2}{V_t}\right)$$

to get,

$$i_D = \frac{W}{L}\,I_t\exp\left(\frac{v_{GS} - V_T}{nV_t}\right)\left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right)\right]$$

where $n \approx 1.5 - 3$

If $v_{DS} > 0$, then

$$i_D = I_t\frac{W}{L}\exp\left(\frac{v_{GS} - V_T}{nV_t}\right)\left(1 + \frac{v_{DS}}{V_A}\right)$$

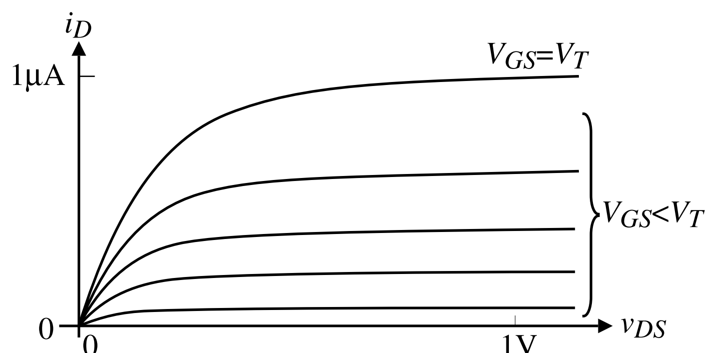

Fig. 140-03

Small-Signal Model for Weak Inversion

Small-signal model:

$$g_m = \frac{di_D}{dv_{GS}}\Big|_Q = I_t \frac{W}{L} \frac{I_t}{nV_t} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right)\left(1+\frac{v_{DS}}{V_A}\right) = \frac{I_D}{nV_t} = \frac{qI_D}{nkT} = \frac{I_D}{V_t}\frac{C_{ox}}{C_{ox}+C_{js}}$$

$$g_{ds} = \frac{di_D}{dv_{DS}}\Big|_Q \approx \frac{I_D}{V_A}$$

The boundary between nonsaturated and saturated is found as,

$$V_{ov} = V_{DS}(\text{sat}) = V_{ON} = V_{GS} - V_T = 2nV_t$$

Simulation of an n-channel MOSFET in both Weak and Strong Inversion

Uses the BSIM model.†

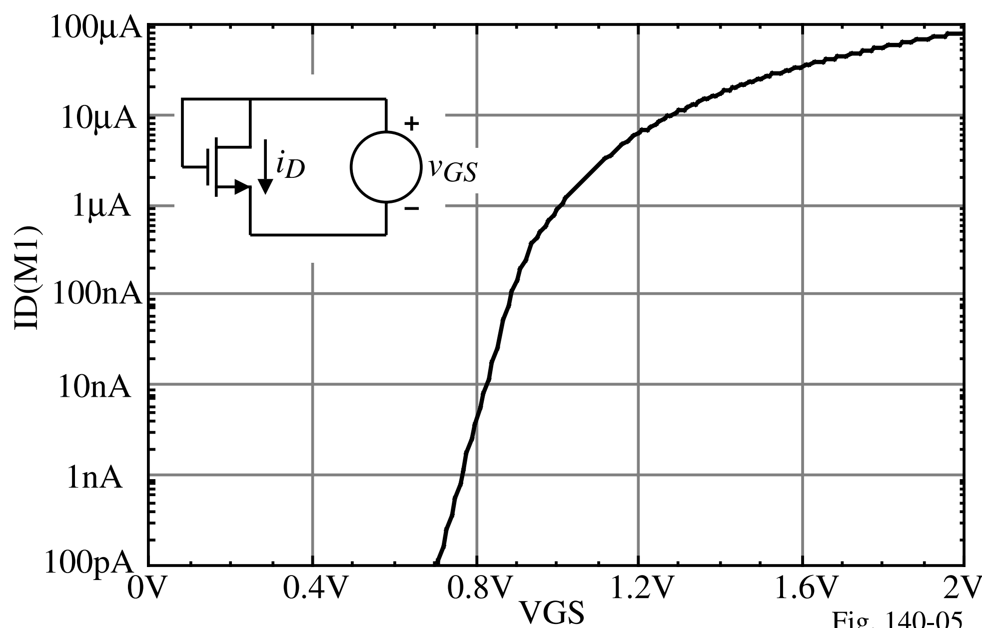

Fig. 140-05

† Y. Cheng and C. Hu, *MOSFET Modeling & BSIM3 User's Guide*, Kluwer Academic Publishers, Boston, 1999.

Example 3-1 – The NMOS in Weak Inversion

Calculate V_{ov} and f_T for an NMOS transistor with I_D = 1µA, I_t = 0.1µA, and $v_{DS}>>V_T$. Assume that W = 10µm, L = 1µm, n = 1.5, K'_N = 200µA/V², t_{ox} = 100Å, and the temperature is 27°C.

Solution

First we find the

$$V_{ov} = V_{DS}(\text{sat}) = V_{ON} = V_{GS} - V_T = 2nV_t = 2(1.5)(25.9\text{mV}) \approx \underline{78\text{mV}}$$

Next, we need to find g_m and C_{gs}.

$$g_m = \frac{I_D}{nV_t} = \frac{1\mu\text{A}}{1.5 \cdot 25.9\text{mV}} = 25.75\mu\text{S}$$

Previously, we found that $n = 1 + \frac{C_{js}}{C_{ox}}$. $\therefore$ $C_{js} = (n-1)C_{ox} = 0.5\ C_{ox}$

It can be shown that

$$C_{gs} = WL\left(\frac{C_{ox}C_{js}}{C_{ox}+C_{js}}\right) = 0.33WLC_{ox} = \frac{10\mu\text{m}^2}{3}\ \frac{3.9\times8.854\times10^{-14}(\text{F/cm})\times(100\text{cm}/10^6\mu\text{m})}{100\text{Å}\times(10^6\mu\text{m}/10^{10}\text{Å})}$$

$$C_{gs} = 11.5\text{fF} \quad \rightarrow \quad f_T = \frac{1}{2\pi}\omega_T = \frac{1}{2\pi}\frac{25.75\mu\text{S}}{11.5\text{fF}} \approx \underline{360\text{MHz}}$$

(Equivalent transistor operating in strong inversion has an f_T = 3.4GHz)

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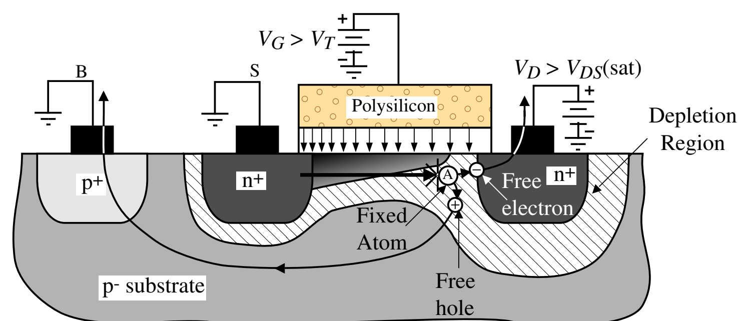
SUBSTRATE CURRENT FLOW IN MOSFETS

Impact Ionization

Impact Ionization:

Occurs because high electric fields cause an impact which generates a hole-electron pair. The electrons flow out the drain and the holes flow into the substrate causing a substrate current flow.

Illustration:



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Model of Substrate Current Flow

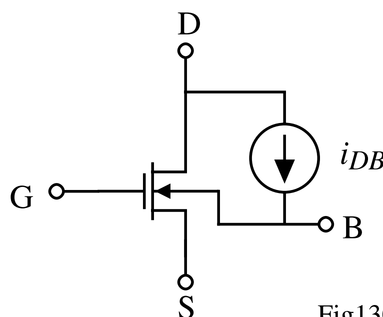
Substrate current:

$$i_{DB} = K_1(v_{DS} - v_{DS}(\text{sat}))i_D e^{-[K_2/(v_{DS}-v_{DS}(\text{sat}))]}$$

where

K_1 and K_2 are process-dependent parameters (typical values: $K_1 = 5\text{V}^{-1}$ and $K_2 = 30\text{V}$)

Schematic model:



Small-signal model:

$$g_{db} = \frac{\partial i_{DB}}{\partial v_{DB}} = K_2 \frac{I_{DB}}{V_{DS} - V_{DS}(\text{sat})}$$

This conductance will have a negative influence on high-output resistance current sinks/sources.

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SUBSTRATE INTERFERENCE IN CMOS CIRCUITS

How Do Carriers Get Injected into the Substrate?

1.) Hot carriers (substrate current)

2.) Electrostatic coupling (across depletion regions and other dielectrics)

3.) Electromagnetic coupling (parallel conductors)

Why is this a Problem?

With decreasing channel lengths, more circuitry is being integrated on the same substrate. The result is that noisy circuits (circuits with rapid transitions) are beginning to adversely influence sensitive circuits (such as analog circuits).

Present Solution

Keep circuit separate by using multiple substrates and put the multiple substrates in the same package.

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Hot Carrier Injection in CMOS Technology without an Epitaxial Region

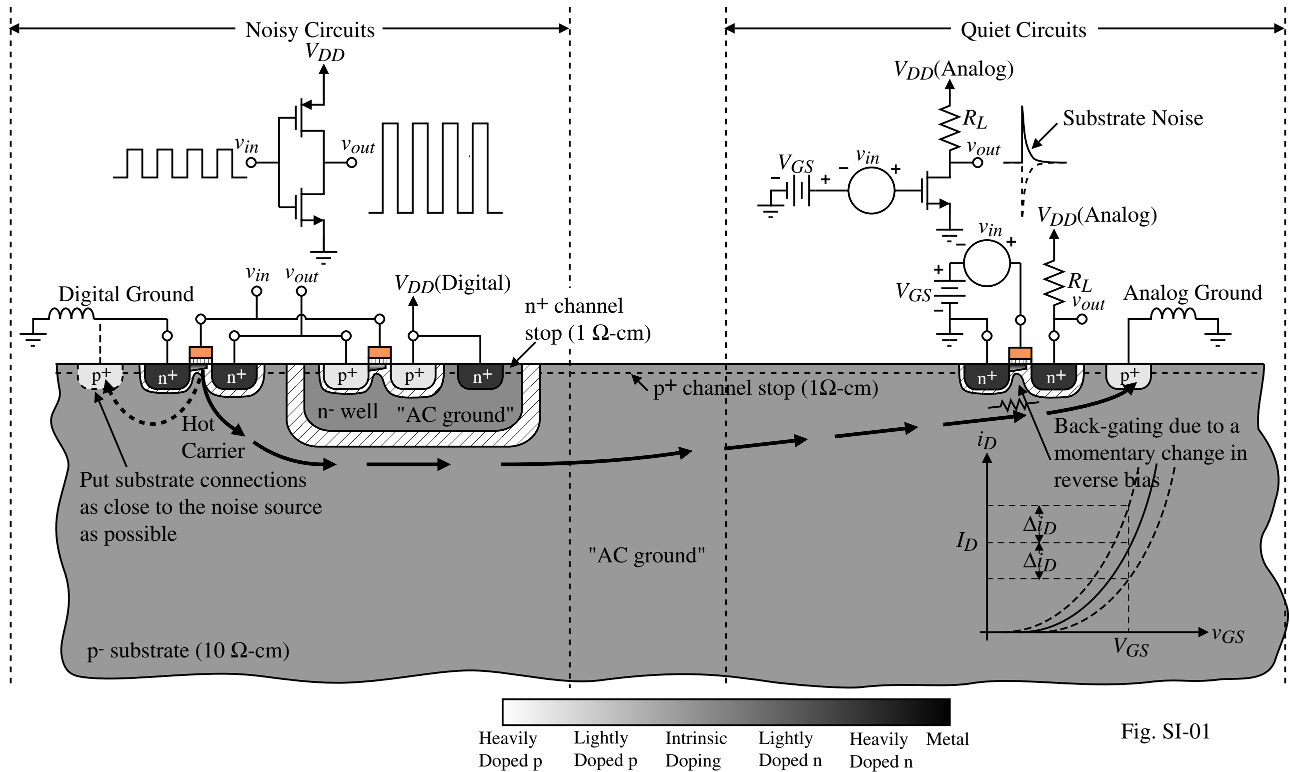


Fig. SI-01

Hot Carrier Injection in CMOS Technology with an Epitaxial Region

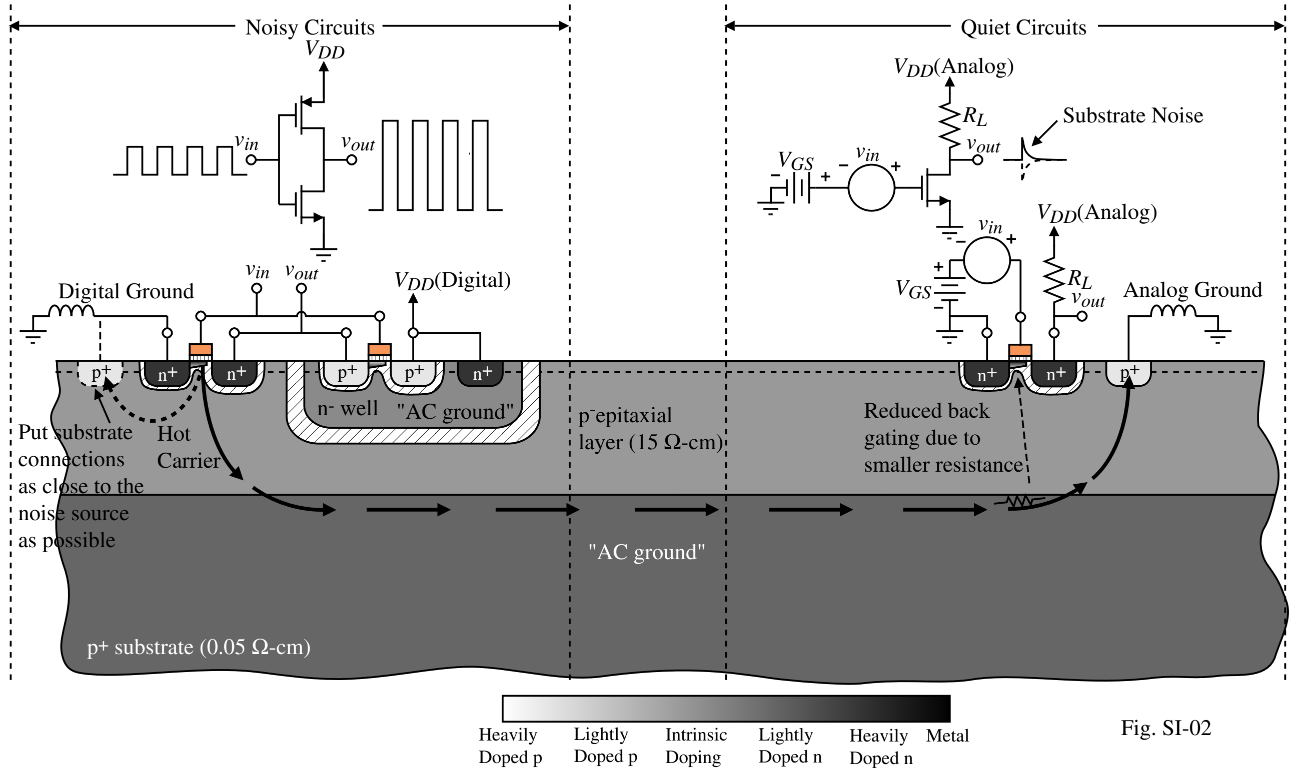
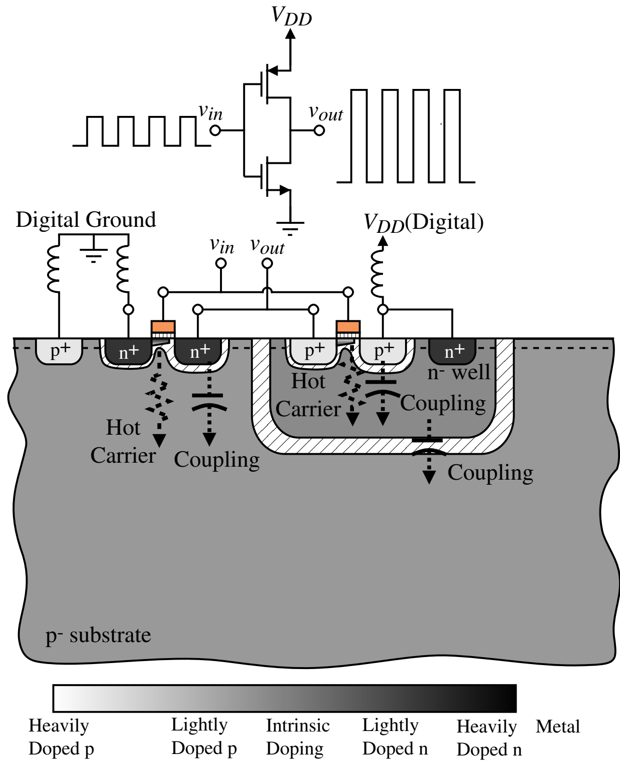
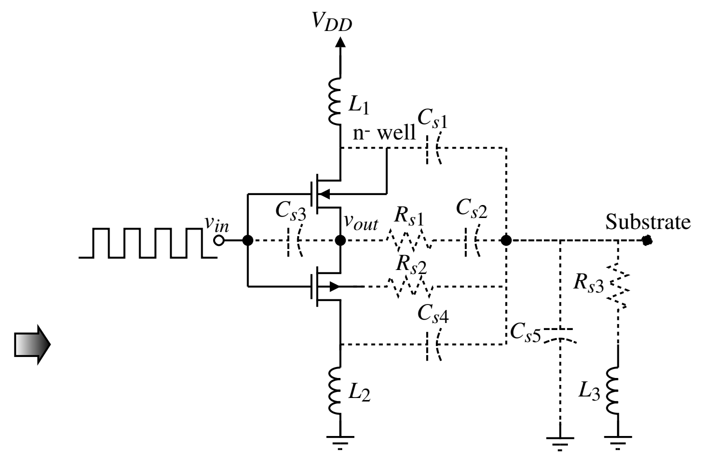


Fig. SI-02

Computer Model for Substrate Interference Using SPICE Primitives

Noise Injection Model:





C_{s1} = Capacitance between n-well and substrate

C_{s2},C_{s3} and C_{s4} = Capacitances between interconnect lines (including bond pads) and substrate

C_{s5} = All capacitance between the substrate and ac ground

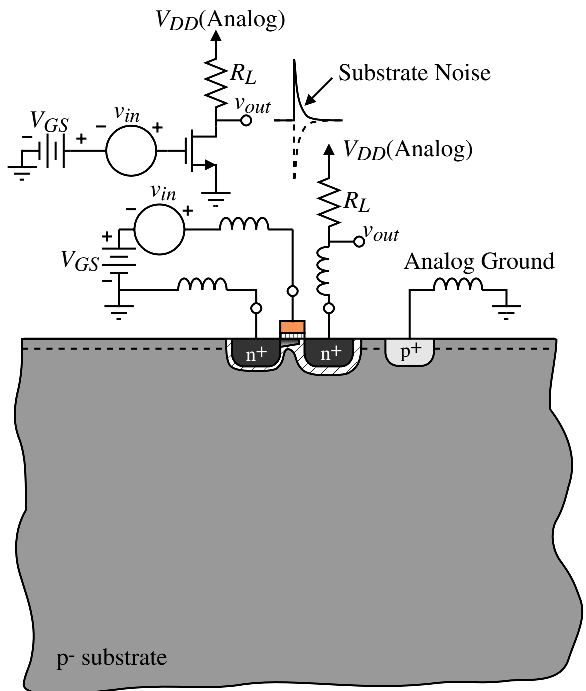
R_{s1},R_{s2} and R_{s3} = Bulk resistances in n-well and substrate

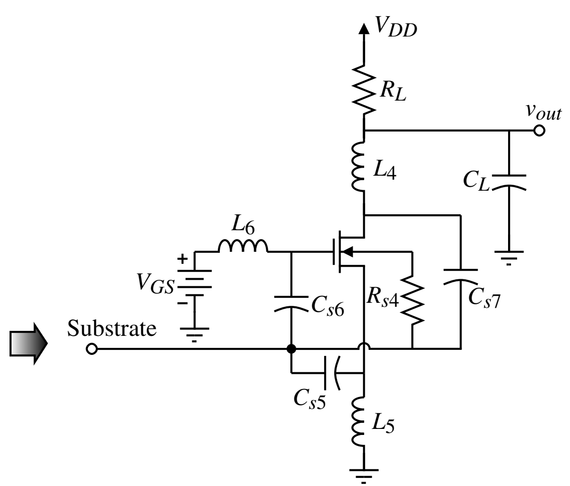
L_1,L_2 and L_3 = Inductance of the bond wires and package leads

Fig. SI-06

Computer Model for Substrate Interference Using SPICE Primitives

Noise Detection Model:





C_{s5},C_{s6} and C_{s7} = Capacitances between interconnect lines (including bond pads) and substrate

R_{s4} = Bulk resistance in the substrate

L_4,L_5 and L_6 = Inductance of the bond wires and package leads

Fig. SI-07

Other Sources of Substrate Injection

(We do it to ourselves and can't blame the digital circuits.)

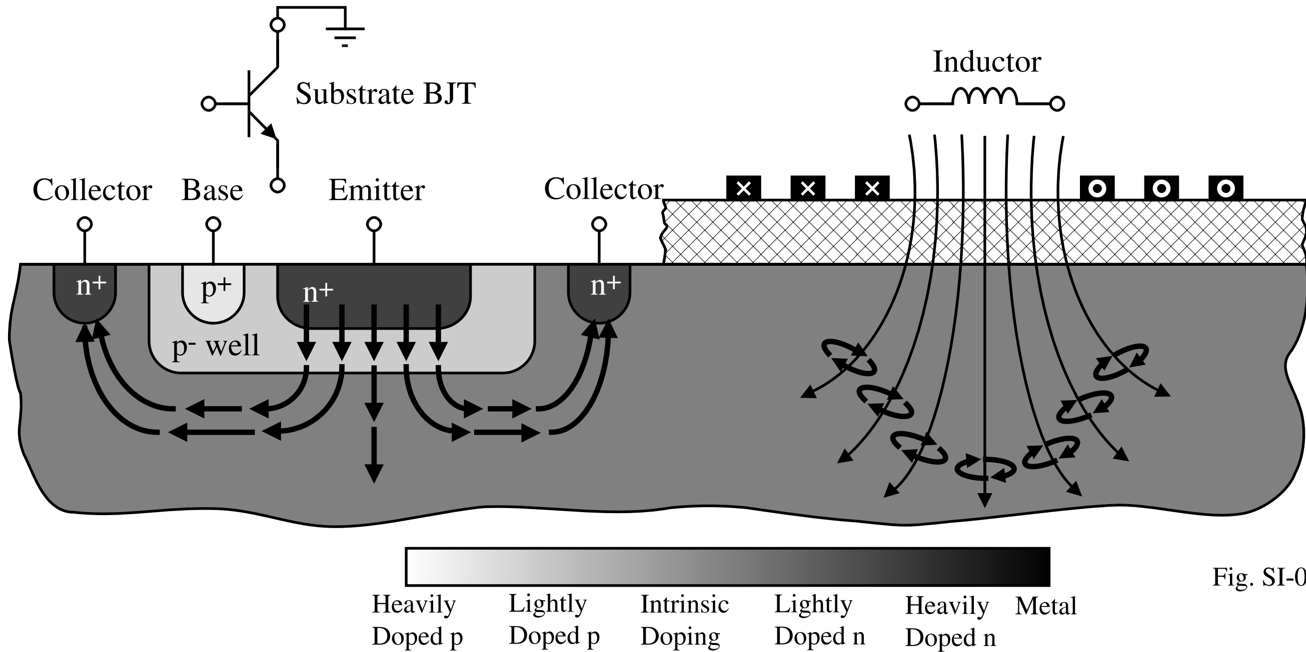


Fig. SI-04

Also, there is coupling from power supplies and clock lines to other adjacent signal lines.

What is a Good Ground?

- On-chip, it is a region with very low bulk resistance.

  It is best accomplished by connecting metal to the region at as many points as possible.

- Off-chip, it is all determined by the connections or bond wires.

  The inductance of the bond wires is large enough to create significant ground potential changes for fast current transients.

$$v = L\frac{di}{dt}$$

  Use multiple bonding wires to reduce the ground noise caused by inductance.

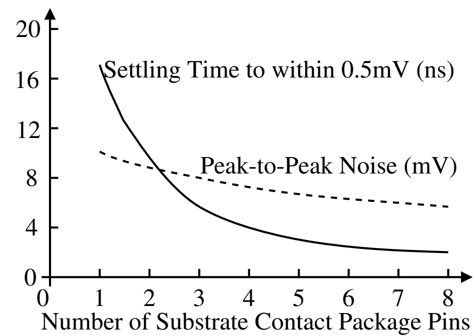


Fig. SI-08

- Fast changing signals have part of their path (circuit through ground and power supplies. Therefore bypass the off-chip power supplies to ground as close to the chip as possible.

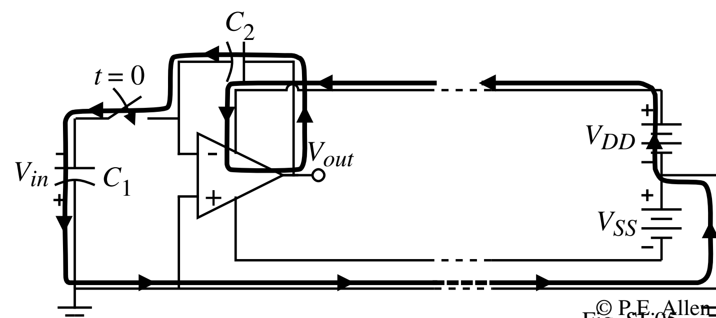


Fig. SI-05

Summary of Substrate Interference

- Methods to reduce substrate noise
  1.) Physical separation
  2.) Guard rings placed close to the sensitive circuits with dedicated package pins.
  3.) Reduce the inductance in power supply and ground leads (best method)
  4.) Connect regions of constant potential (wells and substrate) to metal with as many contacts as possible.
- Noise Insensitive Circuit Design Techniques
  1.) Design for a high power supply rejection ratio (PSRR)
  2.) Use multiple devices spatially distinct and average the signal and noise.
  3.) Use "quiet" digital logic (power supply current remains constant)
  4.) Use differential signal processing techniques.
- Some references

1.) D.K. Su, M.J. Loinaz, S. Masui and B.A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal IC's," *J. of Solid-State Circuits*, vol. 28, No. 4, April 1993, pp. 420-430.

2.) K.M. Fukuda, T. Anbo, T. Tsukada, T. Matsuura and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal ICs," *J. of Solid-State Circuits*, vol. 31, No. 5, May 1996, pp. 726-731.

3.) X. Aragones, J. Gonzalez and A. Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs*, Kluwer Acadmic Publishers, Boston, MA, 1999.

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3.4 - CAPACITANCES OF THE MOSFET

Types of Capacitance

Physical Picture:

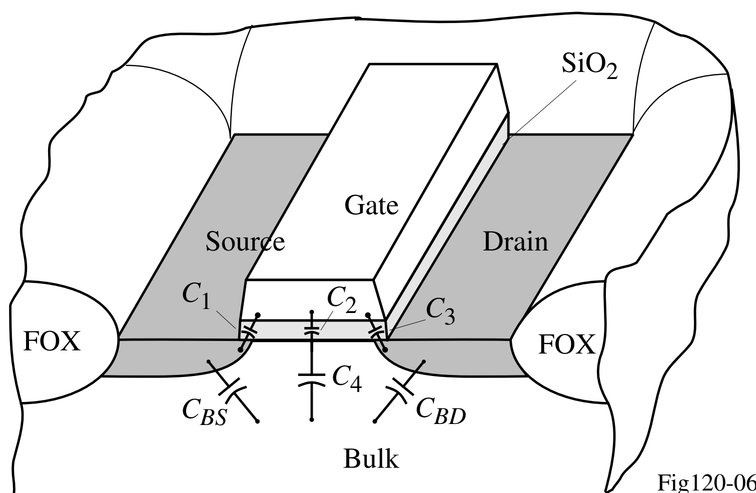

Fig120-06

MOSFET capacitors consist of:
- Depletion capacitances
- Charge storage or parallel plate capacitances

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MOSFET Depletion Capacitors

Model:

1.) $v_{BS} \leq FC{\cdot}PB$

$$C_{BS} = \frac{CJ{\cdot}AS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJ}} + \frac{CJSW{\cdot}PS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJSW}},$$

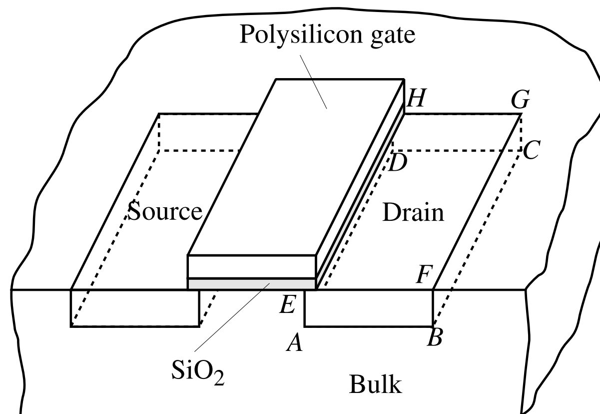


Fig. 120-07

Drain bottom = $ABCD$

Drain sidewall = $ABFE + BCGF + DCGH + ADHE$

and

2.) $v_{BS} > FC{\cdot}PB$

$$C_{BS} = \frac{CJ{\cdot}AS}{(1 - FC)^{1+MJ}}\left(1 - (1+MJ)FC + MJ\frac{V_{BS}}{PB}\right) + \frac{CJSW{\cdot}PS}{(1 - FC)^{1+MJSW}}\left(1 - (1+MJSW)FC + MJSW\frac{V_{BS}}{PB}\right)$$

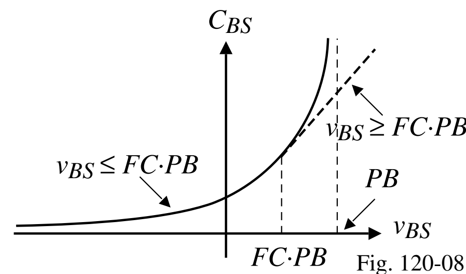


Fig. 120-08

where

AS = area of the source

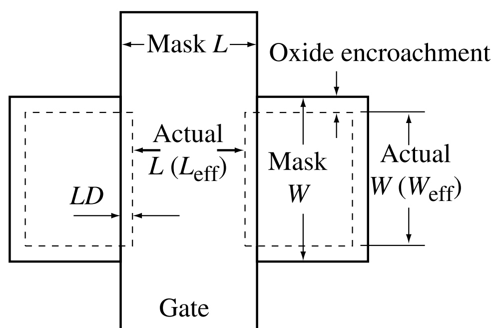
PS = perimeter of the source

$CJSW$ = zero bias, bulk source sidewall capacitance

$MJSW$ = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "S" by "D" in the above.

Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4



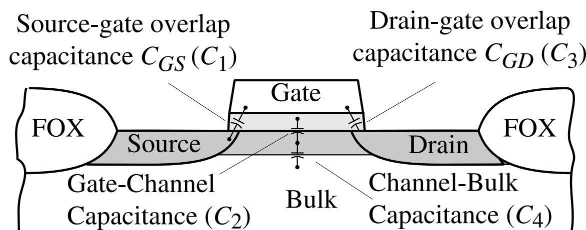


Fig. 120-09

Overlap capacitances:

$C_1 = C_3 = \text{LD}{\cdot}W_{eff}{\cdot}C_{ox}$ = CGSO or CGDO

(LD ≈ 0.015 μm for LDD structures)

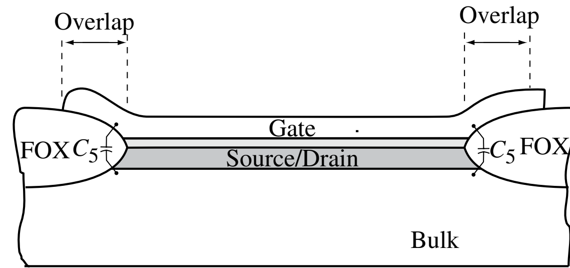
Channel capacitances:

C_2 = gate-to-channel = $C_{ox}W_{eff}{\cdot}(L\text{-}2\text{LD}) = C_{ox}W_{eff}{\cdot}L_{eff}$

C_4 = voltage dependent channel-bulk/substrate capacitance

Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain



C_5 = CGBO

Capacitance values based on an oxide thickness of 140 Å or C_{ox}=24.7 × 10^{-4} F/m^2:

Type	P-Channel	N-Channel	Units
CGSO	220 ×10^{-12}	220 × 10^{-12}	F/m
CGDO	220 × 10^{-12}	220 × 10^{-12}	F/m
CGBO	700 × 10^{-12}	700 × 10^{-12}	F/m
CJ	560 × 10^{-6}	770 × 10^{-6}	F/m^2
CJSW	350 × 10^{-12}	380 × 10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

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Expressions for C_{GD}, C_{GS} and C_{GB}

Cutoff Region:

$$C_{GB} = C_2 + 2C_5 = C_{ox}(W_{eff})(L_{eff}) + 2\text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 \approx C_{ox}(\text{LD})W_{eff} = \text{CGSO}(W_{eff})$$

$$C_{GD} = C_3 \approx C_{ox}(\text{LD})W_{eff} = \text{CGDO}(W_{eff})$$

Saturation Region:

$$C_{GB} = 2C_5 = \text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 + (2/3)C_2 = C_{ox}(\text{LD}+0.67L_{eff})(W_{eff}) = \text{CGSO}(W_{eff}) + 0.67C_{ox}(W_{eff})(L_{eff})$$

$$C_{GD} = C_3 \approx C_{ox}(\text{LD})W_{eff}) = \text{CGDO}(W_{eff})$$

Nonsaturated Region:

$$C_{GB} = 2\,C_5 = 2\text{CGBO}(L_{eff})$$

$$C_{GS} = C_1 + 0.5C_2 = C_{ox}(\text{LD}+0.5L_{eff})(W_{eff}) = (\text{CGSO} + 0.5C_{ox}L_{eff})W_{eff}$$

$$C_{GD} = C_3 + 0.5C_2 = C_{ox}(\text{LD}+0.5L_{eff})(W_{eff}) = (\text{CGDO} + 0.5C_{ox}L_{eff})W_{eff}$$

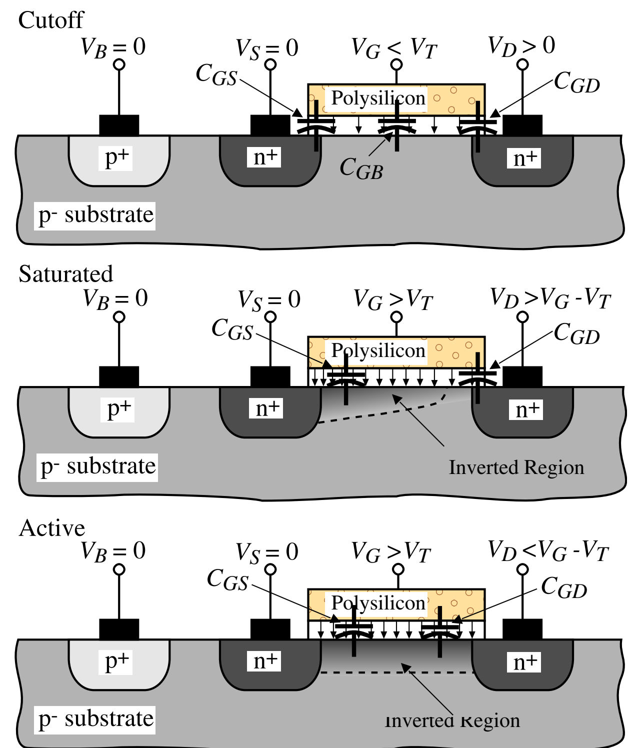

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Illustration of C_{GD}, C_{GS} and C_{GB}

Comments on the variation of C_{BG} in the cutoff region:

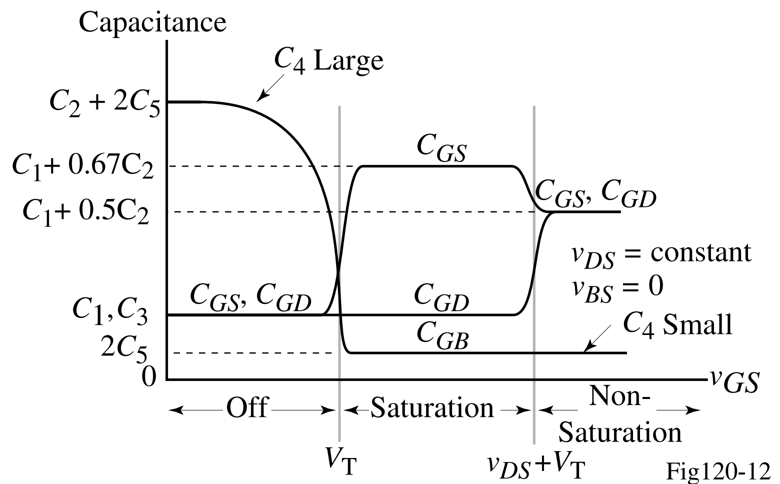
$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

1.) For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$

(C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T))

2.) For $0 < v_{GS} \leq V_T$, $C_{GB} \approx 2C_5$

(C_4 is small because of the thicker inversion layer in strong inversion)



3.5 – SMALL SIGNAL MODELS FOR THE MOSFET

Small-Signal Model for the Saturation Region

The small-signal model is a linearization of the large signal model about a quiescent or operating point.

Consider the large-signal MOSFET in the saturation region ($v_{DS} \geq v_{GS} - V_T$) :

$$i_D = \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

The small-signal model is the linear dependence of i_d on v_{gs}, v_{bs}, and v_{ds}. Written as,

$$i_d \approx g_m v_{gs} + g_{mbs} v_{bs} + g_{ds} v_{ds}$$

where

$$g_m \equiv \frac{di_D}{dv_{GS}}\Big|_Q = \beta(V_{GS}-V_T) = \sqrt{2\beta I_D}$$

$$g_{ds} \equiv \frac{di_D}{dv_{DS}}\Big|_Q = \frac{\lambda I_D}{1 + \lambda V_{DS}} \approx \lambda I_D$$

and

$$g_{mbs} \equiv \frac{di_D}{dv_{BS}}\Big|_Q = \left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dv_{GS}}{dv_{BS}}\right)\Big|_Q = \left(-\frac{di_D}{dV_T}\right)\left(\frac{dV_T}{dv_{BS}}\right)\Big|_Q = \frac{g_m\gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Small-Signal Model – Continued

Complete schematic model:

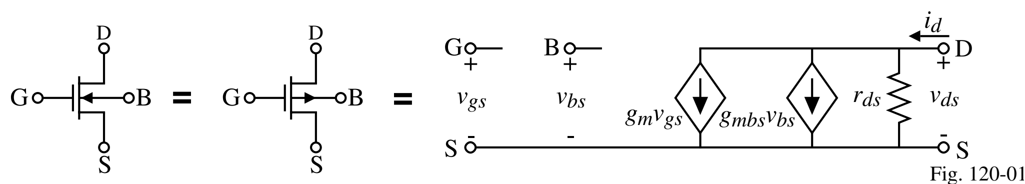


Fig. 120-01

where

$$g_m \equiv \frac{di_D}{dv_{GS}}\Big|_Q = \beta(V_{GS}\text{-}V_T) = \sqrt{2\beta I_D}$$

$$g_{ds} \equiv \frac{di_D}{dv_{DS}}\Big|_Q = \frac{\lambda i_D}{1 + \lambda v_{DS}} \approx \lambda i_D$$

and

$$g_{mbs} = \frac{\partial i_D}{\partial v_{BS}}\Big|_Q = \left(\frac{\partial i_D}{\partial v_{GS}}\right)\left(\frac{\partial v_{GS}}{\partial v_{BS}}\right)\Big|_Q = \left(-\frac{\partial i_D}{\partial v_T}\right)\left(\frac{\partial v_T}{\partial v_{BS}}\right)\Big|_Q = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Simplified schematic model:

An extremely important assumption:

$$g_m \approx 10 g_{mbs} \approx 100 g_{ds}$$

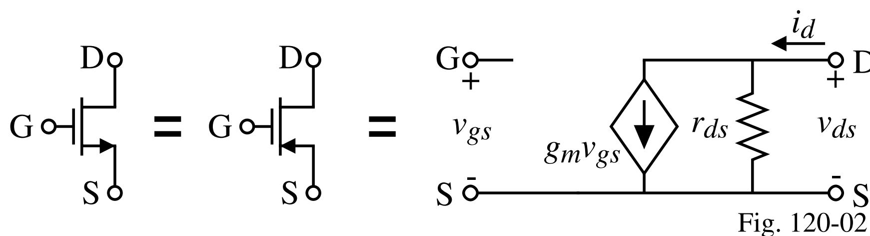


Fig. 120-02

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Illustration of the Small-Signal Model Application

Assume that the gate is connected to the drain.

DC resistor:

$$\text{DC resistance} = \frac{v}{i}\Big|_Q = \frac{V}{I} = R_{DC}$$

Useful for biasing - creating current from voltage and vice versa

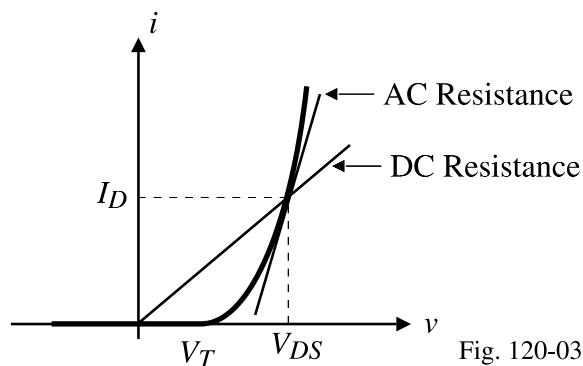

Fig. 120-03

Small-Signal Load (AC resistance):

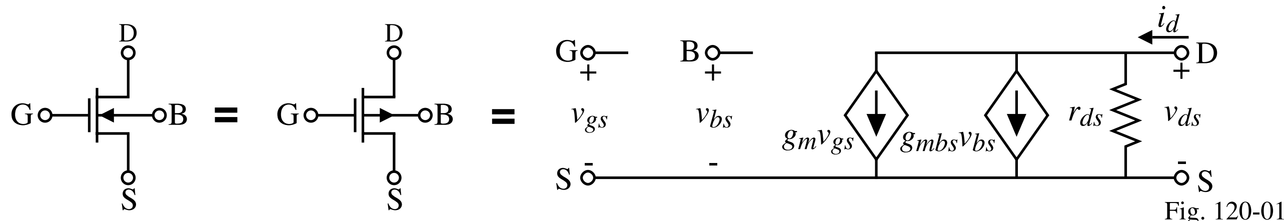

Fig. 120-01

Assume that $v_{bs} = 0$,

$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{v_{gs}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m} = R_{ac}$$

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Small-Signal Model for the Nonsaturated Region

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_Q = \frac{K'WV_{DS}}{L}(1+\lambda V_{DS}) \approx \left(\frac{K'W}{L}\right)V_{DS}$$

$$g_{mbs} = \frac{\partial i_D}{\partial v_{BS}}\Big|_Q = \frac{K'W\gamma V_{DS}}{2L\sqrt{2\phi_F - V_{BS}}}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}}\Big|_Q = \frac{K'W}{L}(V_{GS} - V_T - V_{DS})(1+\lambda V_{DS}) + \frac{I_D\lambda}{1+\lambda V_{DS}} \approx \frac{K'W}{L}(V_{GS} - V_T - V_{DS})$$

Note:

While the small-signal model analysis is independent of the region of operation, the evaluation of the small-signal performance is not.

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Small Signal Model for the Subthreshold Region

If $v_{DS} > 0$, then

$$i_D = K_x \frac{W}{L} e^{v_{GS}/nV_t}(1 + \lambda v_{DS})$$

Small-signal model:

$$g_m = \frac{di_D}{dv_{GS}}\Big|_Q = \frac{qI_D}{nkT}$$

$$g_{ds} = \frac{di_D}{dv_{DS}}\Big|_Q \approx \frac{I_D}{V_A}$$

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Small-Signal Frequency Dependent Model

The depletion capacitors are found by evaluating the large signal capacitors at the DC operating point.

The charge storage capacitors are constant for a specific region of operation.

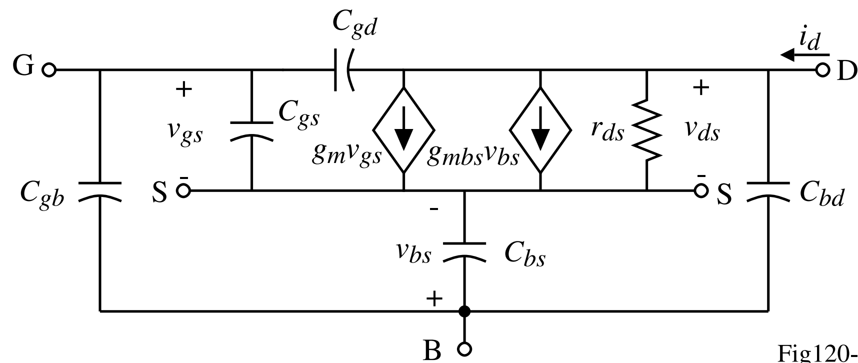

Fig120-13

Gain-bandwidth of the MOSFET:

Assume $V_{SB} = 0$ and the MOSFET is in saturation,

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}} \approx \frac{1}{2\pi}\frac{g_m}{C_{gs}}$$

Recalling that

$$C_{gs} \approx \frac{2}{3} C_{ox}WL \quad \text{and} \quad g_m = \mu_o C_{ox}\frac{W}{L}(V_{GS}\text{-}V_T) \quad \rightarrow \quad f_T = \frac{3}{4\pi}\frac{\mu_o}{L^2}(V_{GS}\text{-}V_T)$$

3.6 - TEMPERATURE AND NOISE MODELS FOR THE MOSFET

Large Signal Temperature Model

Transconductance parameter:

$K'(T) = K'(T_0)\,(T/T_0)^{-1.5}$ (Exponent becomes +1.5 below 77°K)

Threshold Voltage:

$V_T(T) = V_T(T_0) + \alpha(T\text{-}T_0) + \cdots$

Typically α_{NMOS} = -2mV/°C to –3mV/°C from 200°K to 400°K (PMOS has a + sign)

Example

Find the value of I_D for a NMOS transistor at 27°C and 100°C if V_{GS} = 2V and W/L = 5µm/1µm if $K'(T_0)$ = 110µA/V^2 and $V_T(T_0)$ = 0.7V and T_0 = 27°C and α_{NMOS} = -2mV/°C.

Solution

At room temperature, the value of drain current is,

$$I_D(27°\text{C}) = \frac{110\mu\text{A/V}^2\cdot 5\mu\text{m}}{2\cdot 1\mu\text{m}}(2\text{-}0.7)^2 = 465\mu\text{A}$$

At T = 100°C (373°K), $K'(100°\text{C}) = K'(27°\text{C})\,(373/300)^{-1.5}$=110µA/V^2·0.72=79.3µA/V^2

and $V_T(100°\text{C})$ = 0.7 – (.002)(73°C) = 0.554V

$$\therefore \quad I_D(100°\text{C}) = \frac{79.3\mu\text{A/V}^2\cdot 5\mu\text{m}}{2\cdot 1\mu\text{m}}(2\text{-}0.554)^2 = 415\mu\text{A}$$

(Repeat with V_{GS} = 1.5V)

Experimental Verification of the MOSFET Temperature Dependence

NMOS Threshold:

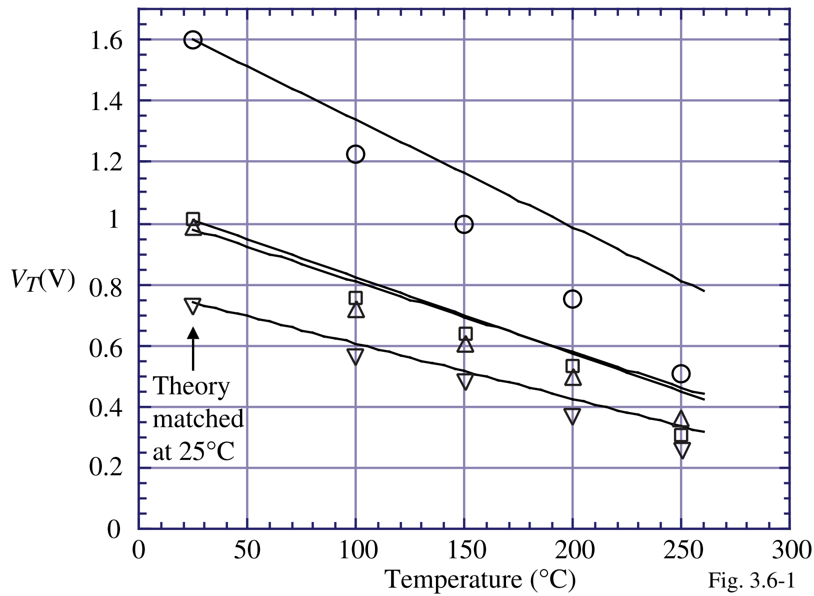

Fig. 3.6-1

Symbol	Min. L	NA (cm^{-3})	tox (Å)	α (mV/°C)
O	6μm	$2x10^{16}$	1000	-3.5
❑	5μm	$1x10^{16}$	650	-2.5
Δ	4μm	$2x10^{16}$	500	-2.3
∇	2μm	$3.3x10^{16}$	275	-1.8

Experimental Verification of the MOSFET Temperature Dependence

PMOS Threshold:

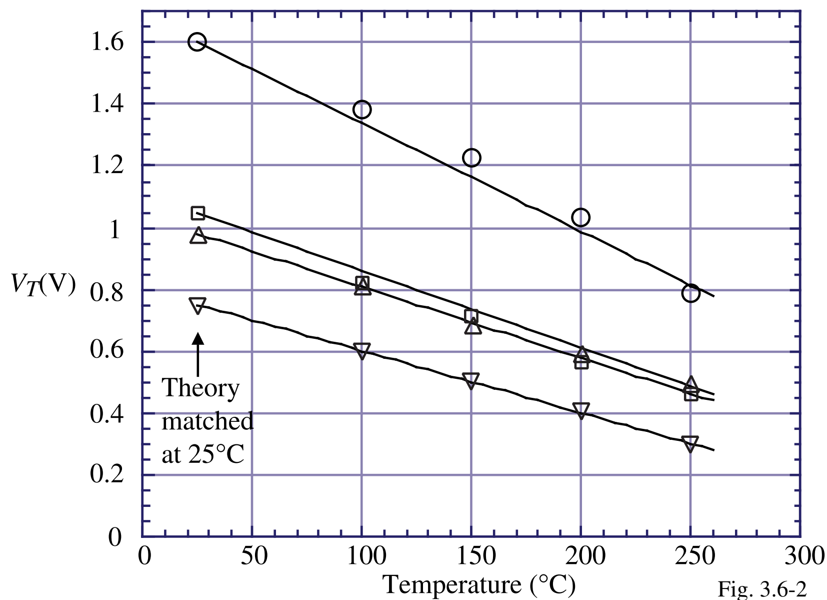

Fig. 3.6-2

Symbol	Min. L	NA (cm^{-3})	Tox (Å)	α (mV/°C)
O	6μm	$2x10^{15}$	1000	+3.5
❑	5μm	$2x10^{15}$	650	+2.5
Δ	4μm	$2x10^{16}$	500	+2.3
∇	2μm	$1.1x10^{16}$	275	+2.0

Experimental Verification of the MOSFET Temperature Dependence

NMOS *K'*:

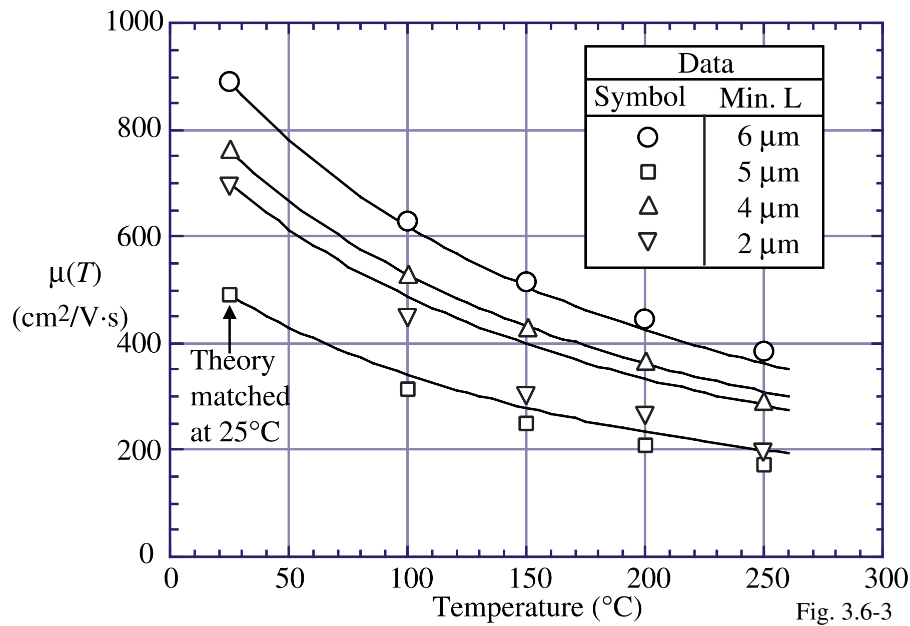

Fig. 3.6-3

Experimental Verification of the MOSFET Temperature Dependence

PMOS *K'*:

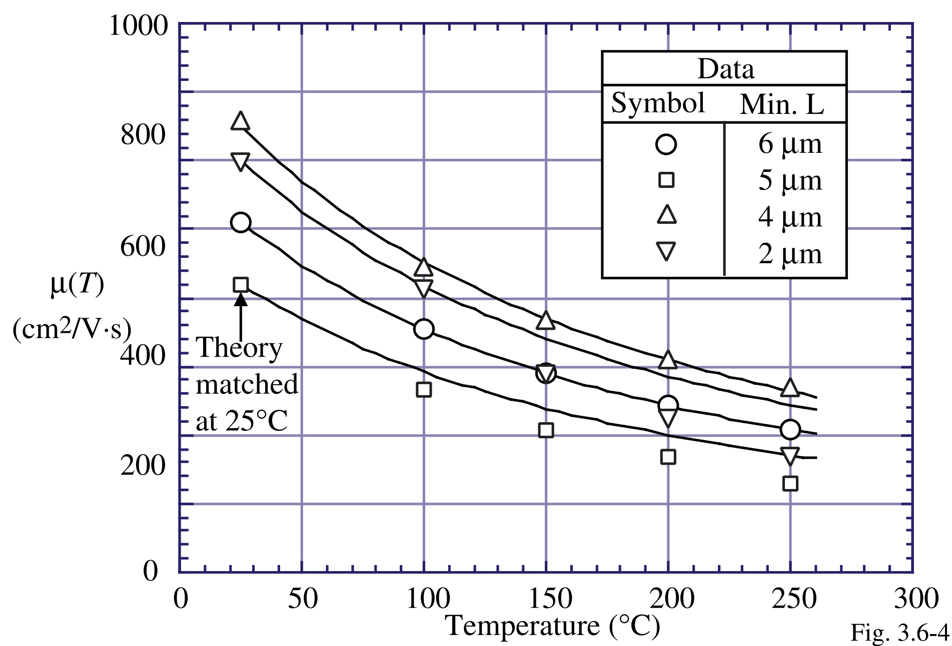

Fig. 3.6-4

Zero Temperature Coefficient (ZTC) Point for MOSFETs

For a given value of gate-source voltage, the drain current of the MOSFET will be independent of temperature. Consider the following circuit:

Assume that the transistor is saturated and that:

$$\mu = \mu_o \left(\frac{T}{T_o}\right)^{-1.5} \quad \text{and} \quad V_T(T) = V_T(T_o) + \alpha(T-T_o)$$

where $\alpha = -0.0023\text{V/°C}$ and $T_o = 27°\text{C}$

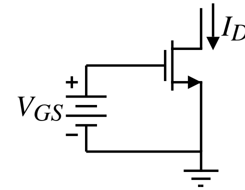

Fig. 4.5-12

$$\therefore \; I_D(T) = \frac{\mu_o C_{ox} W}{2L} \left(\frac{T}{T_o}\right)^{-1.5} [V_{GS} - V_{T0} - \alpha(T-T_o)]^2$$

$$\frac{dI_D}{dT} = \frac{-1.5\mu_o C_{ox}}{2T_o} \left(\frac{T}{T_o}\right)^{-2.5} [V_{GS}-V_{T0}-\alpha(T-T_o)]^2 + \alpha\mu_o C_{ox} \left(\frac{T}{T_o}\right)^{-1.5} [V_{GS}-V_{T0}-\alpha(T-T_o)] = 0$$

$$\therefore \quad V_{GS} - V_{T0} - \alpha(T-T_o) = \frac{-4T\alpha}{3} \quad \Rightarrow \quad \boxed{V_{GS}(\text{ZTC}) = V_{T0} - \alpha T_o - \frac{\alpha T}{3}}$$

Let $K' = 10\mu\text{A/V}^2$, $W/L = 5$ and $V_{T0} = 0.71\text{V}$.

At T=27°C (300°K), V_{GS}(ZTC)=0.71-(-0.0023)(300°K)-(0.333)(-0.0023)(300°K) = 1.63V

At T = 27°C (300°K), $I_D = (10\mu\text{A/V}^2)(5/2)(1.63\text{-}0.71)^2 = 21.2\mu\text{A}$

At T=200°C (473°K), V_{GS}(ZTC)=0.71-(-0.0023)(300°K)-(0.333)(-0.0023)(473°K)=1.76V

Experimental Verification of the ZTC Point

The data below is for a 5µm n-channel MOSFET with W/L=50µm/10µm, N_A=10^{16} cm^{-3}, t_{ox} = 650Å, $u_o C_{ox} = 10\mu\text{A/V}^2$, and V_{T0} = 0.71V.

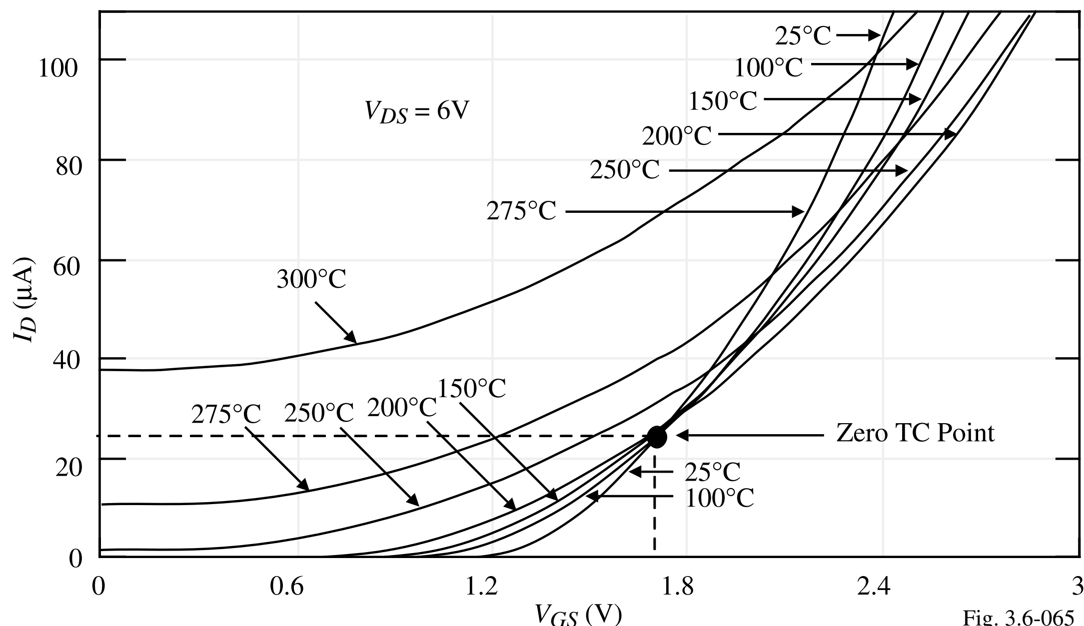

Fig. 3.6-065

ZTC Point for PMOS

The data is for a 5µm p-channel MOSFET with W/L=50µm/10µm, N_D=2x10^{-15}cm^{-3}, and t_{ox} = 650Å.

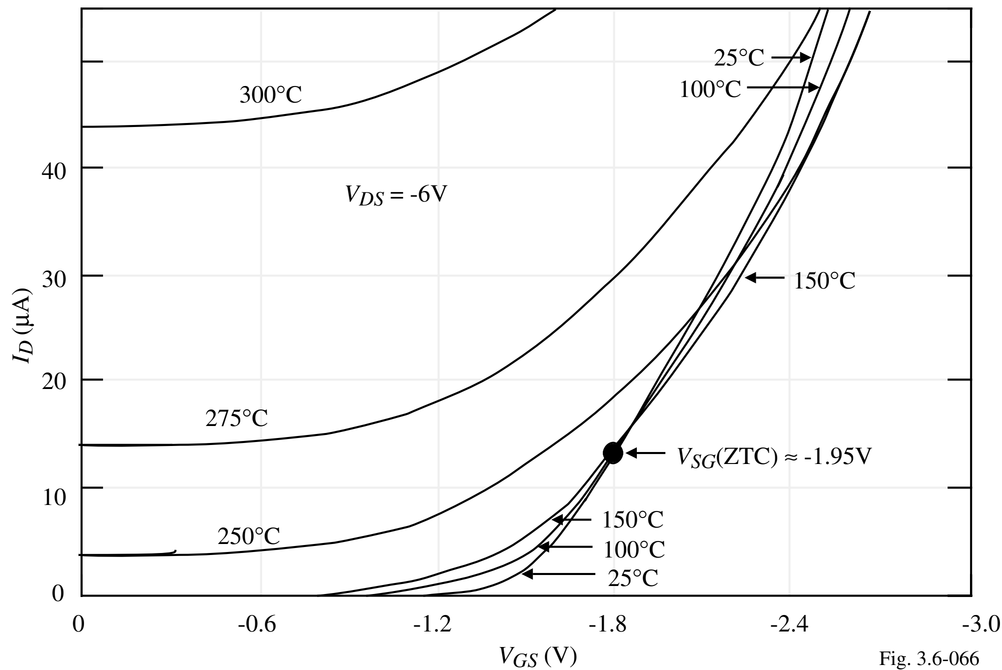

Fig. 3.6-066

Zero temperature coefficient will occur for every MOSFET up to about 200°C.

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Bulk-Drain (Bulk-Source) Leakage Currents (V_{GS}>V_T)

Cross-section of a NMOS in a p-well:

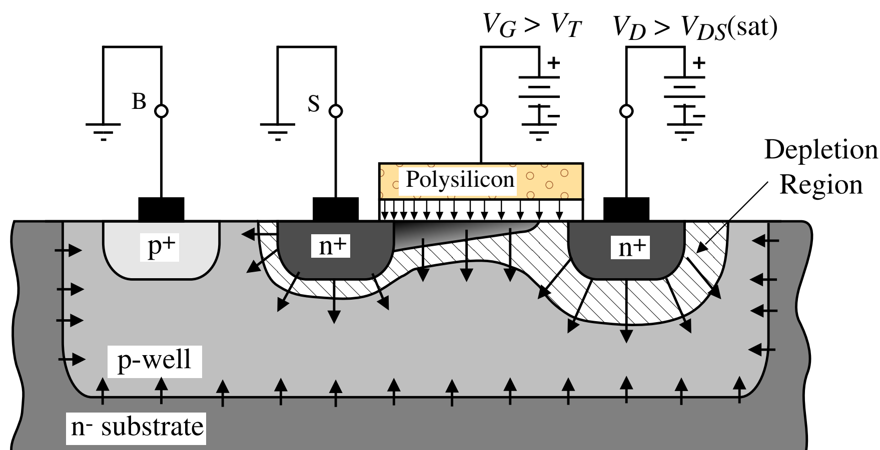

Fig.3.6-5

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Bulk-Drain (Bulk-Source) Leakage Currents ($V_{GS}<V_T$)

Cross-section of a NMOS in a p-well:

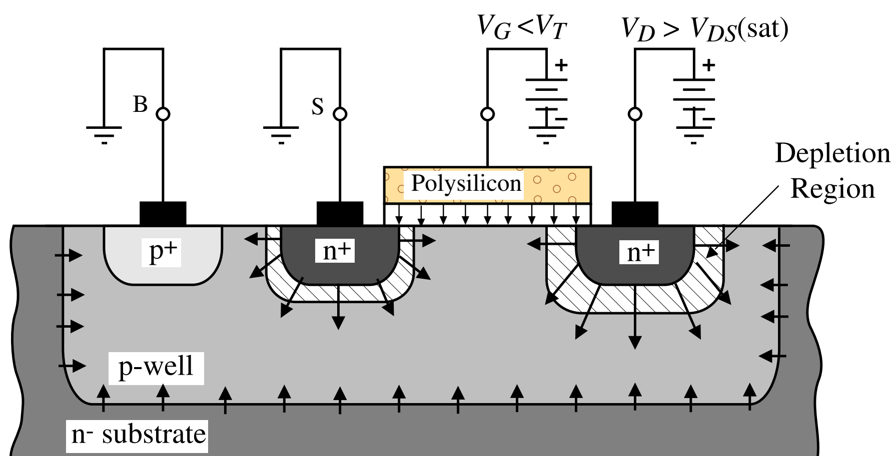


Fig.3.6-6

Temperature Modeling of the PN Junction

PN Junctions (Reverse-biased only):

$$-i_D \cong I_s = qA\left[\frac{Dppno}{L_p} + \frac{Dnnpo}{L_n}\right] \cong \frac{qAD}{L}\frac{n_i^2}{N} = KT^3 \exp\left(\frac{-V_{Go}}{V_t}\right)$$

Differentiating with respect to temperature gives,

$$\frac{dI_s}{dT} = \frac{3KT^3}{T}\exp\left(\frac{-V_{Go}}{V_t}\right) + \frac{qKT^3V_{Go}}{KT^2}\exp\left(\frac{-V_{Go}}{V_t}\right) = \frac{3I_s}{T} + \frac{I_s}{T}\frac{V_{Go}}{V_t}$$

$$TC_F = \frac{dI_S}{I_S dT} = \frac{3}{T} + \frac{1}{T}\frac{V_{Go}}{V_t}$$

Example

Assume that the temperature is 300°K (room temperature) and calculate the reverse diode current change and the TC_F for a 5°K increase.

Solution

The TC_F can be calculated from the above expression as

$$TC_F = 0.01 + 0.155 = 0.165$$

Since the TC_F is change per degree, the reverse current will increase by a factor of 1.165 for every degree K (or °C) change in temperature. Multiplying by 1.165 five times gives an increase of approximately 2. Thus, the reverse saturation current approximately doubles for every 5°C temperature increase. Experimentally, the reverse current doubles for every 8 °C increase in temperature because the reverse current is part leakage current.

Experimental Verification of the PN Junction Temperature Dependence

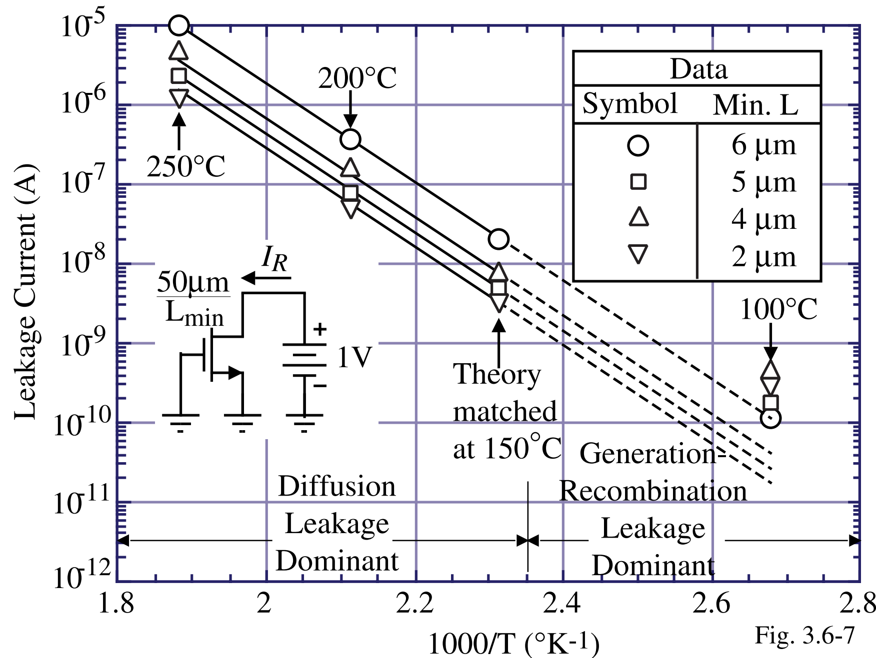


Fig. 3.6-7

Theory:

$$I_s(T) \propto T^3 \exp\left(\frac{V_G(T)}{kT}\right)$$

Temperature Modeling of the PN Junction – Continued

PN Junctions (Forward biased – v_D constant):

$$i_D \cong I_s \exp\left(\frac{v_D}{V_t}\right)$$

Differentiating this expression with respect to temperature and assuming that the diode voltage is a constant ($v_D = V_D$) gives

$$\frac{di_D}{dT} = \frac{i_D}{I_s}\frac{dI_s}{dT} - \frac{1}{T}\frac{V_D}{V_t} i_D$$

The fractional temperature coefficient for i_D is

$$\frac{1}{i_D}\frac{di_D}{dT} = \frac{1}{I_s}\frac{dI_s}{dT} - \frac{V_D}{TV_t} = \frac{3}{T} + \left[\frac{V_{Go} - V_D}{TV_t}\right]$$

If V_D is assumed to be 0.6 volts, then the fractional temperature coefficient is equal to 0.01 + (0.155 - 0.077) = 0.0879. The forward diode current will double for a 10°C.

PN Junctions (Forward biased – i_D constant):

$$V_D = V_t \ln(I_D/I_s)$$

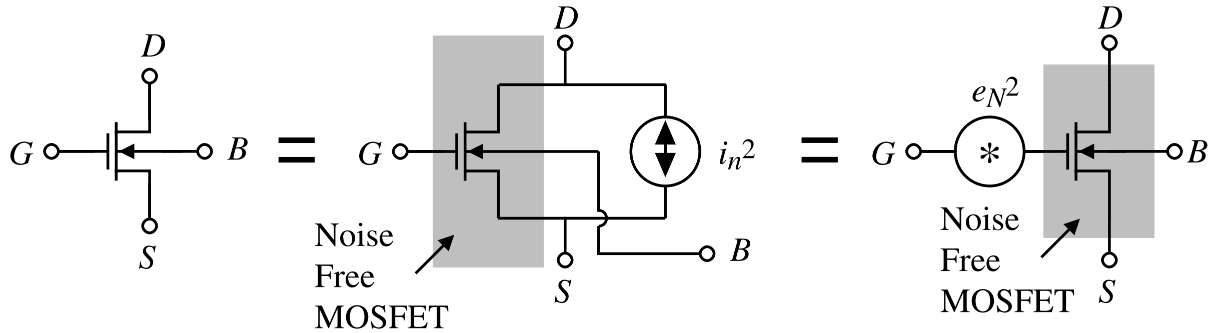
Differentiating with respect to temperature gives

$$\frac{dv_D}{dT} = \frac{v_D}{T} - V_t\left(\frac{1}{I_s}\frac{dI_s}{dT}\right) = \frac{v_D}{T} - \frac{3V_t}{T} - \frac{V_{Go}}{T} = -\left[\frac{V_{Go} - v_D}{T}\right] - \frac{3V_t}{T}$$

Assuming that $v_D = V_D = 0.6$ V the temperature dependence of the forward diode voltage at room temperature is approximately -2.3 mV/°C.

MOSFET NOISE

MOS Device Noise at Low Frequencies



where

$$\overline{i_n^2} = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{KF\ I_D}{f^S C_{ox} L^2} \right] \Delta f \quad \text{(amperes}^2\text{)}$$

Δf = bandwidth at a frequency, f

$\eta = \dfrac{g_{mbs}}{g_m}$

k = Boltzmann's constant

KF = Flicker noise coefficient

S = Slope factor of the 1/f noise

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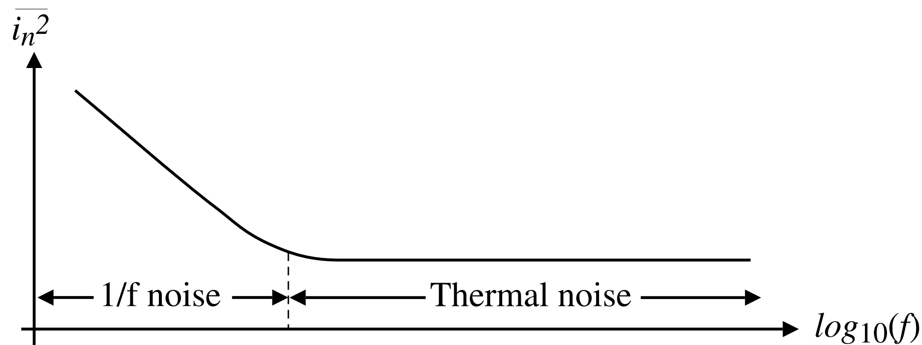
Reflecting the MOSFET Noise to the Gate

Dividing $\overline{i_n^2}$ by g_m^2 gives

$$\overline{e_n^2} = \frac{\overline{i_n^2}}{g_m^2} = \left[\frac{8kT(1+\eta)}{3g_m} + \frac{KF}{2fC_{ox}WL\,K'} \right] \Delta f \quad \text{(volts}^2\text{)}$$

It will be convenient to use $B = \dfrac{KF}{2C_{ox}K'}$ for model simplification.



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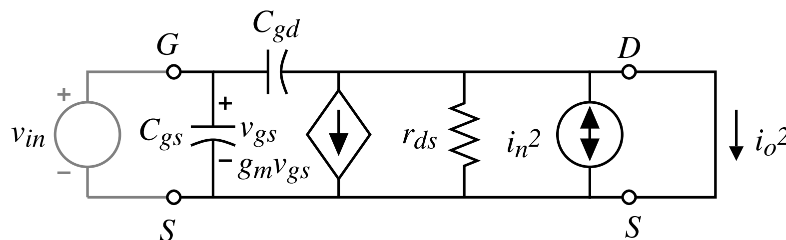
MOS Experimental Noise Data

W/L	I_D(μA)	Noise Voltage at 100Hz (nV/$\sqrt{Hz}$)	Thermal Noise Voltage (nV/$\sqrt{Hz}$)
25/25	90	360	40
25/25	50	360	35
25/25	20	360	25
1.2/1.2	90	10,000	350
1.2/1.2	50	10,000	200
1.2/1.2	20	10,000	180
0.8/0.8	90	70,000	1800
0.8/0.8	50	60,000	1500
0.8/0.8	20	50,000	1200
25/2	90	900	30
25/2	50	850	28
25/2	20	-	-
25/1	90	1000	38
25/1	50	850	33
25/1	20	1000	30
25/0.6	90	950	50
25/0.6	50	750	42
25/0.6	20	700	35

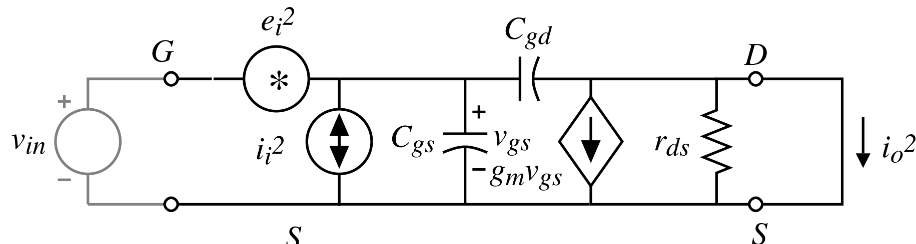
MOSFET Noise Model at High Frequencies

At high frequencies, the source resistance can no longer be assumed to be small. Therefore, a noise current generator at the input results.

MOSFET Noise Models:



Circuit 1: Frequency Dependent Noise Model



Circuit 2: Input-referenced Noise Model

MOSFET Noise Model at High Frequencies – Continued

To find e_i^2 and i_i^2, we will perform the following calculations:

e_i^2:

Short-circuit the input and find i_o^2 of both models and equate to get $\overline{e_i^2}$.

Ckt. 1: $i_o^2 = i_n^2$

Ckt. 2: $i_o^2 = g_m^2\, e_i^2 + (\omega C_{gd})^2 e_i^2$

$$\left.\right\} e_i^2 = \frac{i_n^2}{g_m^2 + (\omega C_{gd})^2}$$

i_i^2:

Open-circuit the input and find i_o^2 of both models and equate to get $\overline{i_i^2}$.

Ckt. 1: $i_o^2 = i_n^2$

$$\text{Ckt. 2: } i_o^2 = \left(\frac{(1/C_{gs})}{(1/C_{ds}) + (1/C_{gs})}\right)^2 i_i^2 + \frac{g_m^2 i_i^2}{\omega^2 (C_{gs}+C_{ds})^2}$$

$$\approx \frac{g_m^2}{\omega^2 C_{gs}^2}\, i_n^2 \text{ if } C_{gd} < C_{gs} \quad \Rightarrow \quad i_i^2 = \frac{\omega^2 C_{gs}^2}{g_m^2}\, i_n^2$$

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SEC. 3.7 – BJT MODELS

Bipolar Transistor Symbol and Sign Convention

The bipolar junction transistor (BJT) is a three-terminal device whose symbol and sign convention (according to the text) is given as shown:

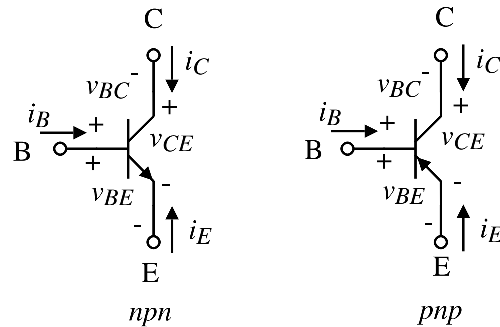

Fig.07-02

Description of the three terminals:

- Emitter - The emitter is the source of majority carriers that result in the gain mechanism of the BJT. These carriers which are "emitted" into the base are electrons for the *npn* transistor and holes for the *pnp* transistor.
- Base - The base is a region which physically separates the emitter and collector and has an opposite doping (holes for the *npn* and electrons for the *pnp* BJTs). The word "base" comes from the way that the first transistors were constructed. The base was the physical support for the whole transistor.
- Collector - The collector serves to "collect" those carries injected from the emitter into the base and which reach the collector without recombination.

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Physical Aspects of an npn BJT

A cross-section of an npn BJT is shown below:

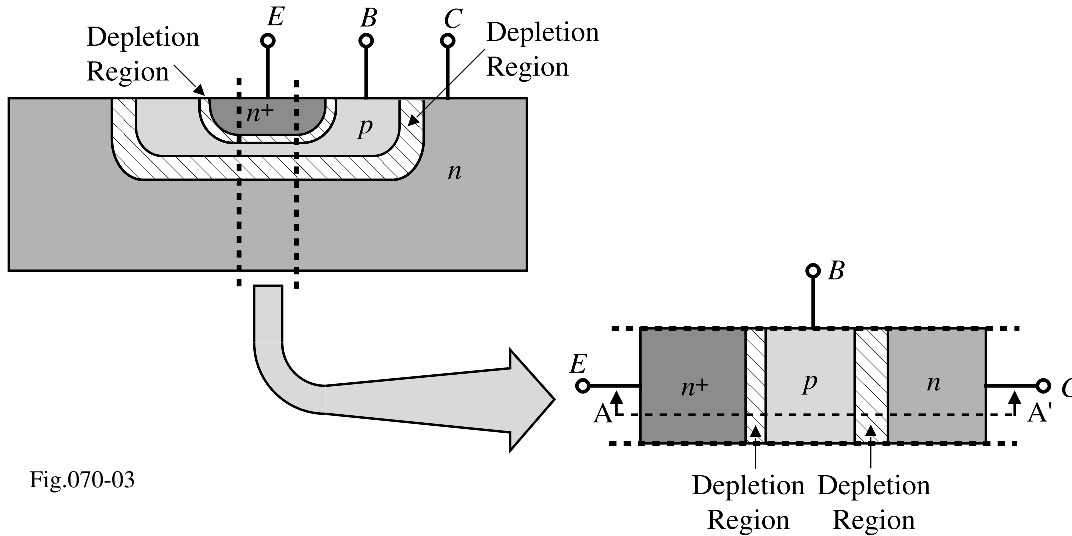


Fig.070-03

Comments:

- The emitter-base depeletion region is generally smaller in width because the doping level is higher and base-emitter junction is generally forward-biased.
- The next slide will examine the carrier concentrations see looking into the above A-A' cross-section.

Carrier Concentrations of the *npn* BJT

The carrier concentrations (not to scale) for the *npn* BJT are shown below.

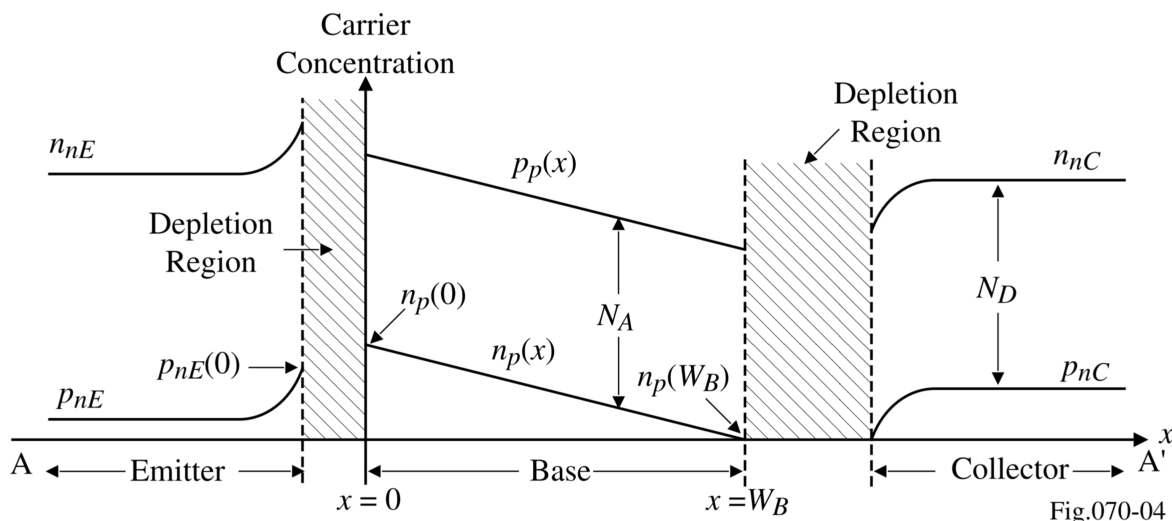


Fig.070-04

Comments:

- The above carrier concentrations assume that the base-emitter junction is forward biased and the base-collector junction is reverse biased.
- The above carrier concentration will be used to derive the large signal model on the next slide.

Derivation of the BJT Large Signal Model in the Foward Active Region

1.) Carrier concentrations in the base on the emitter side. The concentration of electrons in the base on the emitter side ($x = 0$) is

$$n_p(0) = n_{po}\exp(v_{BE}/V_t)$$

The concentration of electrons in the base on the collector side ($x = W_B$) is

$$n_p(W_B) = n_{po}\exp(v_{BC}/V_t) \approx 0 \text{ because } v_{BC} \text{ is negative and large.}$$

2.) If the recombination of electrons in the base is small, then the minority-carrier concentrations, $n_p(x)$, are straight lines and shown on the previous page. From charge-neutrality requirements for the base,

$$N_A + n_p(x) = p_p(x) \quad \rightarrow \quad n_p(x) - p_p(x) = N_A$$

3.) The collector current is produced by minority-carrier electrons in the base diffusing in the direction of the concentration gradient and being swept across the collector-base depletion region by the field existing there. Therefore, the diffusion current density due to electrons in the base is

$$J_n = qD_n\left(\frac{dn_p(x)}{d_x}\right)$$

where D_n is the diffusion constant for electrons. The derivative is the slope of the concentration profile in the base which gives,

$$J_n = -qD_n\left(\frac{n_p(0)}{W_B}\right)$$

Derivation of the BJT Large Signal Model in the Foward Active Region - Continued

3.) Continued

If the collector current is defined as positive flowing into the collector terminal, then

$$i_C = qAD_n\left(\frac{n_p(0)}{W_B}\right) = \frac{qAD_n n_{po}}{W_B}\exp\left(\frac{v_{BE}}{V_t}\right)$$

where A is the cross-sectional area of the emitter. The desired result is

$$\boxed{i_C = I_S\exp\left(\frac{v_{BE}}{V_t}\right)}$$

where the *saturation current*, I_S, is defined as

$$I_S = \frac{qAD_n n_{po}}{W_B}$$

Since, $n_i^2 = n_{po}N_A$, we can rewrite I_S as

$$I_S = \frac{qAD_n n_i^2}{W_B N_A} = \frac{qAD_n n_i^2}{Q_B}$$

where Q_B is the number of doping atoms in the base per unit area of the emitter.

Derivation of the Forward Current Gain of the BJT, β_F

1.) The base current, i_B, consists of two major components. These components are due to the recombination of holes and electrons in the base, i_{B1}, and the injection of holes from the base into the emitter, i_{B2}. It can be shown that,

$$i_{B1} = \frac{1}{2}\frac{n_{po}W_B qA}{\tau_b}\exp\left(\frac{v_{BE}}{V_t}\right) \quad \text{and} \quad i_{B2} = \frac{qAD_p}{L_p}\frac{n_i^2}{N_D}\exp\left(\frac{v_{BE}}{V_t}\right)$$

2.) Therefore the total base current is

$$i_B = i_{B1} + i_{B2} = \left(\frac{1}{2}\frac{n_{po}W_B qA}{\tau_b} + \frac{qAD_p}{L_p}\frac{n_i^2}{N_D}\right)\exp\left(\frac{v_{BE}}{V_t}\right)$$

3.) Define the forward active current gain, β_F, as

$$\beta_F = \frac{i_C}{i_B} = \frac{\frac{qAD_n n_{po}}{W_B}}{\frac{1}{2}\frac{n_{po}W_B qA}{\tau_b} + \frac{qAD_p}{L_p}\frac{n_i^2}{N_D}} = \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \approx 50 \text{ to } 150$$

Note that β_F is increased by decreasing W_B and increasing N_D/N_A.

Derivation of the Current Gain from Emitter to Collector in Forward Active Region

1.) Emitter to collector current gain is designated as, $\alpha_F = \frac{i_C}{i_E}$.

2.) Since sum of all currents flowing into the transistor must be zero, we can write that

$$i_E = -(i_C + i_B) = -\left(i_C + \frac{i_C}{\beta_F}\right) = -i_C\left(1 + \frac{1}{\beta_F}\right) = -\frac{i_C}{\alpha_F}$$

$$\therefore \qquad \alpha_F = \frac{\beta_F}{1+\beta_F} = \frac{1}{1+\frac{1}{\beta_F}} = \frac{1}{1 + \frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \approx \alpha_T\gamma$$

where

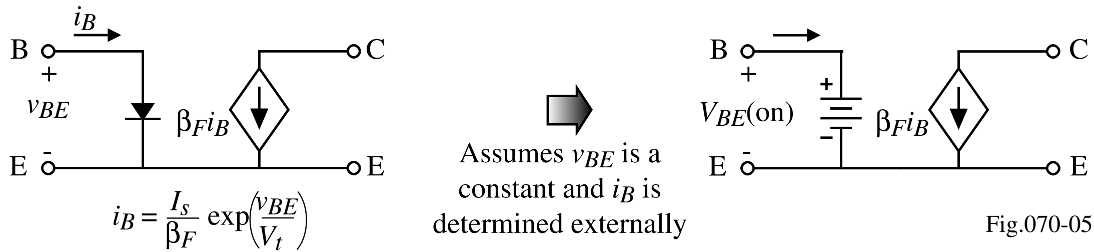
$$\alpha_T \equiv \textit{Base Transport factor} \approx \frac{1}{1 + \frac{W_B^2}{2\tau_b D_n}} \rightarrow 1$$

and

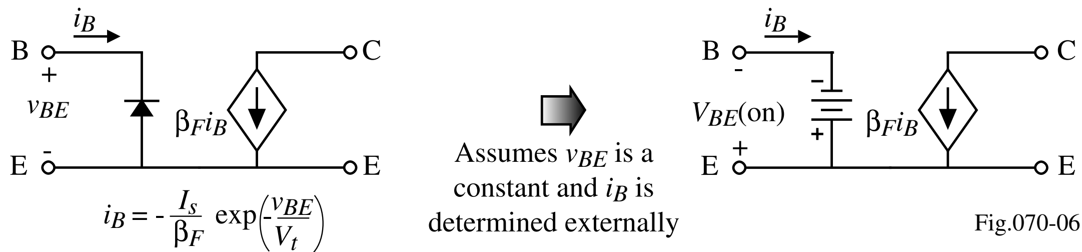
$$\gamma \equiv \textit{Emitter injection efficiency} \approx \frac{1}{1 + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \rightarrow 1$$

Large Signal Model for the BJT in the Forward Active Region

Large-signal model for a *npn* transistor:



Large-signal model for a *pnp* transistor:



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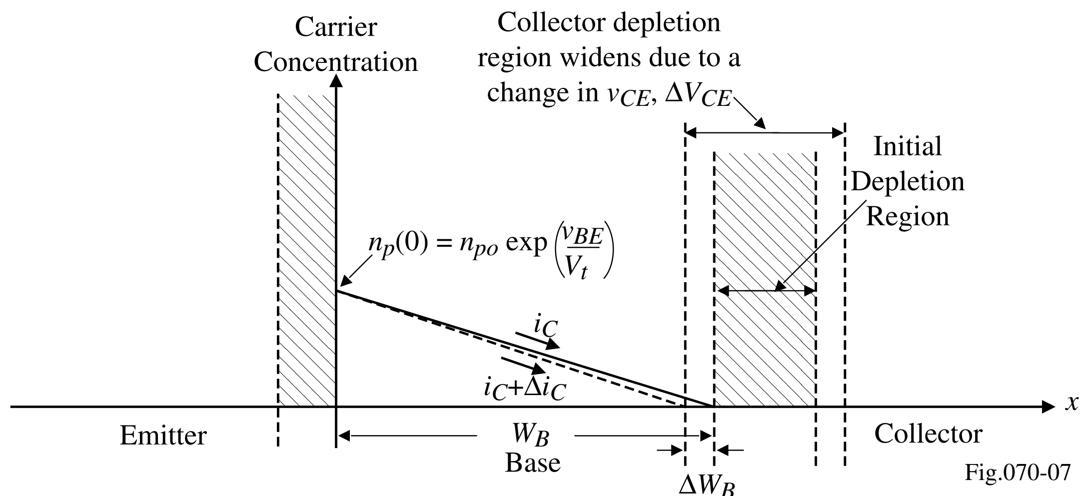
COLLECTOR VOLTAGE INFLUENCE ON THE LARGE SIGNAL MODEL

Base Width Dependence on the Collector-Emitter Voltage

The large signal model so far has the collector current as a function of only the base-emitter voltage. However, there is a weak dependence of the collector current on the collector-emitter voltage that is developed here.

Influence of the base-collector depletion region width:



Note that the change of the collector-emitter voltage causes the amount of charge in the base to change slightly influencing the collector current.

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The Early Voltage of BJTs

Previously we saw that,

$$i_C = \frac{qAD_n n_i^2}{Q_B} \exp\left(\frac{v_{BE}}{V_t}\right)$$

Differentiation of i_C with respect to v_{CE} gives,

$$\frac{\partial i_C}{\partial v_{CE}} = -\frac{qAD_n n_i^2}{Q_B^2}\left(\exp\frac{V_{BE}}{V_t}\right)\frac{\partial Q_B}{\partial v_{CE}} = -\frac{I_C}{Q_B}\frac{\partial Q_B}{\partial v_{CE}}$$

For a uniform-base transistor, $Q_B = W_B N_A$ so that the derivative becomes

$$\frac{\partial i_C}{\partial v_{CE}} = -\frac{I_C}{W_B}\frac{\partial W_B}{\partial v_{CE}} \equiv -\frac{I_C}{V_A} \qquad \Rightarrow \qquad V_A = -W_B\frac{\partial v_{CE}}{\partial W_B}$$

where V_A is called the *Early voltage*.

Illustration of the Early Voltage

The output characteristics of an *npn* BJT:

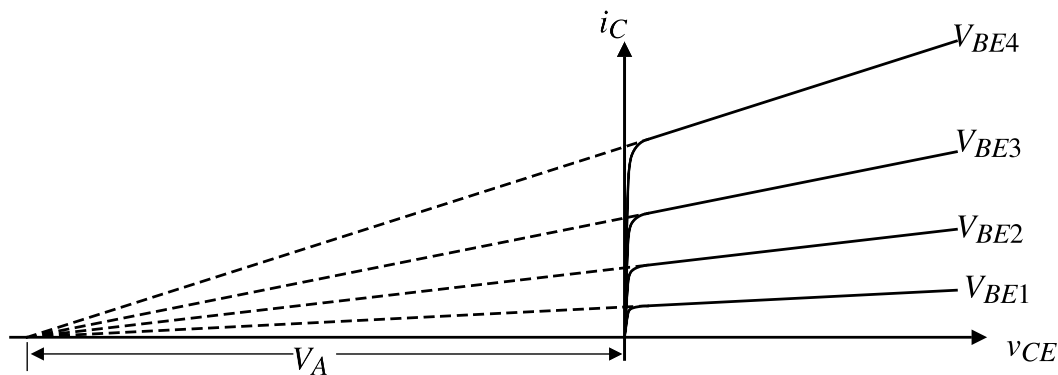

Fig.070-08

Modified large signal model now becomes,

$$i_C = I_S\left(1 + \frac{v_{CE}}{V_A}\right)\exp\left(\frac{v_{BE}}{V_t}\right)$$

SATURATION AND INVERSE ACTIVE REGIONS

Regions of Operation of the BJT

If we consider the transistor as back-to-back diodes, we can clearly see the four regions of operation.

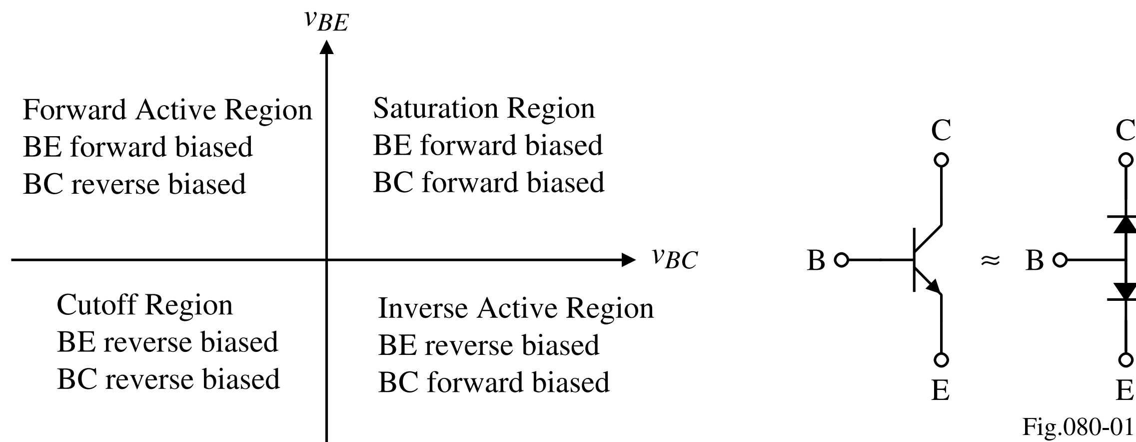

Fig.080-01

Note: While the back-to-back diode model is appropriate here, it is not a suitable model for the BJT in general because it does not model the current gain mechanism of the BJT. Essentially, the back-to-back diode model has a very wide base region and all the injected carriers from the emitter recombine in the base ($\beta_F = 0$).

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Saturation Region

In the saturation region, both the base-emitter and base-collector *pn* junctions are forward biased.

Consequently, there is injection of electrons into the base from both the emitter and collector.

The carrier concentrations in saturation are:

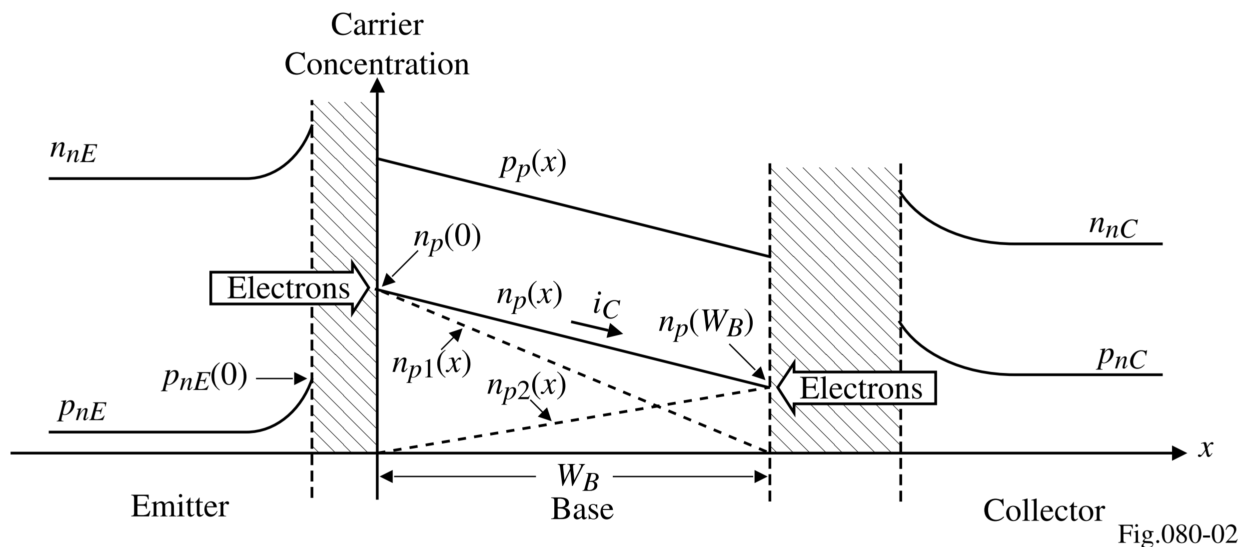

Fig.080-02

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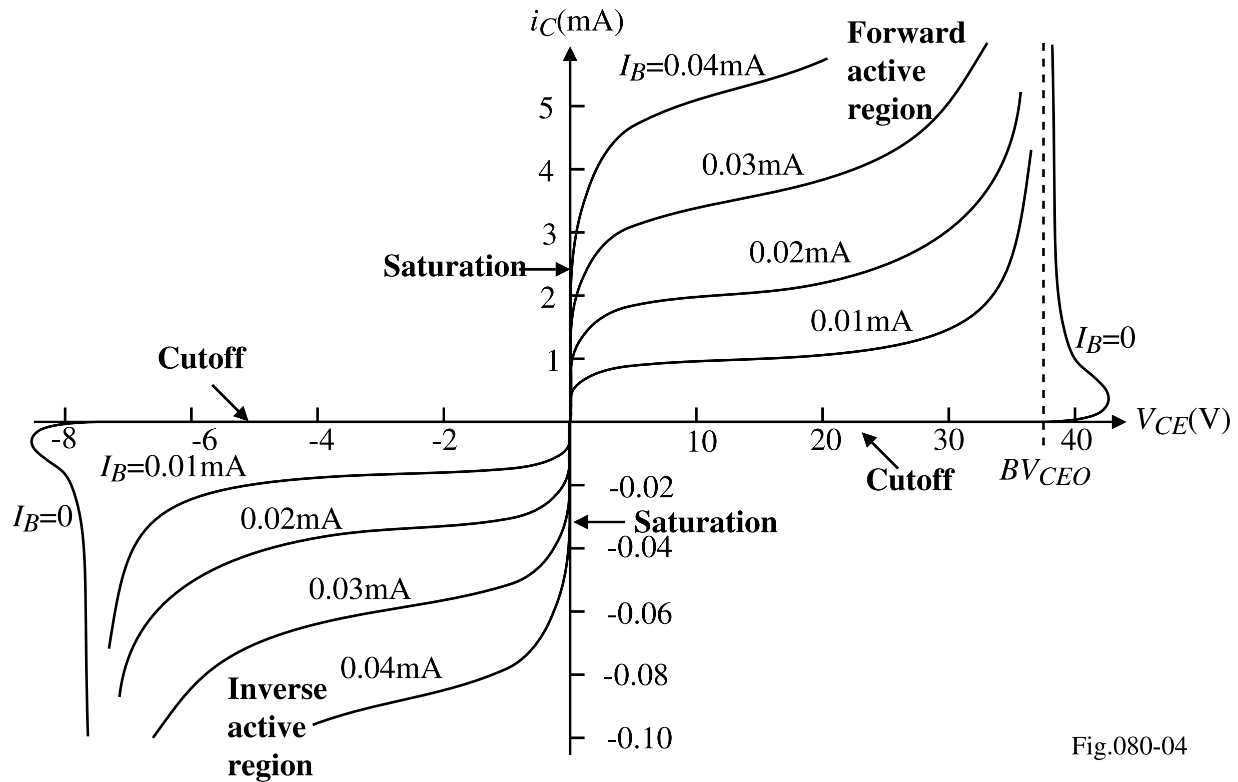
Typical Output Characteristics for an *npn* BJT



Large Signal Model in Saturation

In saturation, both junctions are forward biased and the impedance levels looking into the emitter or collector is very low.

Simplified model:

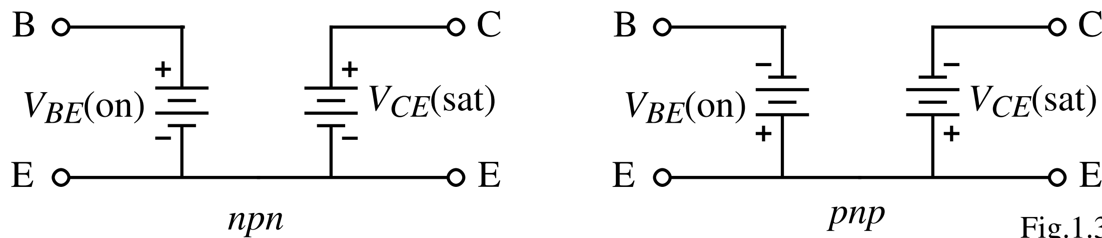


Fig.1.3-11

where V_{BE}(on) ≈ 0.6 to 0.7V and V_{CE}(sat) ≈ 0.2V

The Ebers-Moll Large Signal Model

Consider the saturation condition with both *pn* junctions forward biased.

1.) The emitter injected current in the base resulting from $n_{p1}(x)$ is,

$$i_{EF} = -I_{ES}\left(\exp\frac{v_{BE}}{V_t} - 1\right)$$

where I_{ES} is a constant called "saturation current"

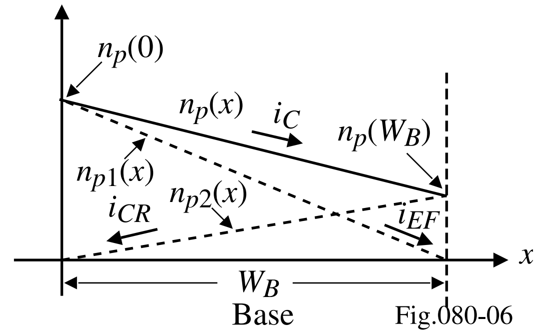


Fig.080-06

2.) The collector injected current in the base resulting from $n_{p2}(x)$ is,

$$i_{CR} = -I_{CS}\left(\exp\frac{v_{BC}}{V_t} - 1\right)$$

where I_{CS} is a constant called "saturation current"

3.) The total collector current, i_C, given as

$$i_C = i_{CR} + \alpha_F i_{EF} = \alpha_F I_{ES}\left(\exp\frac{v_{BE}}{V_t} - 1\right) - I_{CS}\left(\exp\frac{v_{BC}}{V_t} - 1\right)$$

Also, we can write,

$$i_E = i_{EF} + \alpha_R i_{CR} = I_{ES}\left(\exp\frac{v_{BE}}{V_t} - 1\right) + \alpha_R I_{CS}\left(\exp\frac{v_{BC}}{V_t} - 1\right)$$

where α_R is the collector efficiency (as an emitter) and $\beta_R = \alpha_R/(1-\alpha_R)$.

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The Ebers-Moll Equations - Continued

The reciprocity condition allows us to write,

$$\alpha_F I_{EF} = \alpha_R I_{CR} = I_S$$

Substituting into the previous form of the Ebers-Moll equations gives,

$$i_C = I_S\left(\exp\frac{v_{BE}}{V_t} - 1\right) - \frac{I_S}{\alpha_R}\left(\exp\frac{v_{BC}}{V_t} - 1\right)$$

and

$$i_E = -\frac{I_S}{\alpha_F}\left(\exp\frac{v_{BE}}{V_t} - 1\right) + I_S\left(\exp\frac{v_{BC}}{V_t} - 1\right)$$

These equations are valid for all four regions of operation of the BJT.

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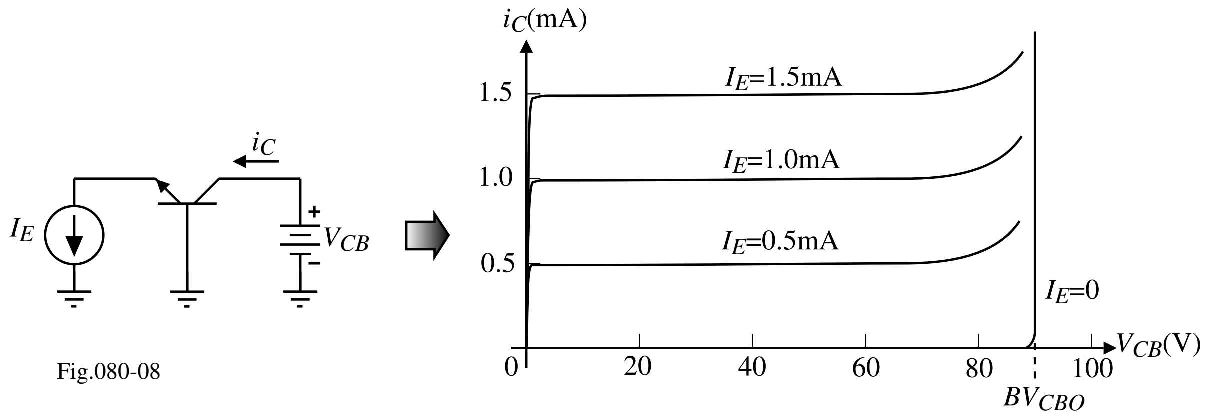
TRANSISTOR BREAKDOWN VOLTAGES

Common-Base Transistor Breakdown Characteristics



As the collector-base voltage becomes large, the collector current can be written as,

$$i_C = -\alpha_F i_E M$$

where

$$M = \frac{1}{1 - \left(\frac{v_{CB}}{BV_{CBO}}\right)^n}$$

Common-Emitter Transistor Breakdown Characteristics

Assume that a constant base current, i_B, is applied. Using the previous result gives

$$i_C = -\alpha_F i_E M \;\Rightarrow\; i_E = \frac{i_C}{-\alpha_F M}$$

$$\therefore \quad i_C = -(i_E + i_B) \quad \Rightarrow \quad i_C\left(1 - \frac{1}{\alpha_F M}\right) = -i_B \quad \Rightarrow \quad i_C = \frac{\alpha_F M}{1-\alpha_F M}\, i_B$$

where,

$$M = \frac{1}{1 - \left(\frac{v_{CB}}{BV_{CBO}}\right)^n}$$

Breakdown occurs when $\alpha_F M = 1$.

Assuming that $v_{CE} \approx v_{CB}$ gives,

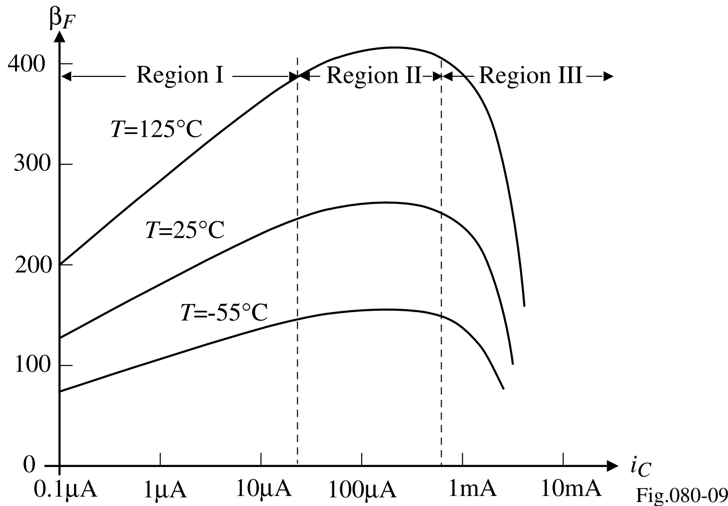
$$\frac{\alpha_F}{1 - \left(\frac{BV_{CEO}}{BV_{CBO}}\right)^n} = 1 \quad \Rightarrow \quad \frac{BV_{CEO}}{BV_{CBO}} = \left(1-\alpha_F\right)^{1/n} \approx \frac{BV_{CBO}}{\beta_F{}^{1/n}}$$

Note that BV_{CEO} is less than BV_{CBO}. For $\beta_F = 100$ and $n = 4$, $BV_{CEO} \approx 0.5BV_{CBO}$.

DEPENDENCE OF β_F ON OPERATING CONDITIONS

Transistor β_F Dependence on Collector Current and Temperature

Plot of β_F as a function of i_C:



Region I: Low current region where β_F decreases as i_C decreases.

Region II: Midcurrent region where β_F is approximately constant.

Region III: High current region where β_F decreases as i_C increases.

The temperature coefficient of β_F is,

$$\mathrm{TC_F} = \frac{1}{\beta_F}\frac{\partial\beta F}{\partial T} \approx +7000\text{ppm/°C (ppm = parts per million)}$$

Variation of Forward Beta with Collector Current

Region II:

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_t}\right) \quad \text{and} \quad i_B \approx \frac{I_S}{\beta_{FM}} \exp\left(\frac{v_{BE}}{V_t}\right)$$

where β_{FM} = the maximum value of β_F.

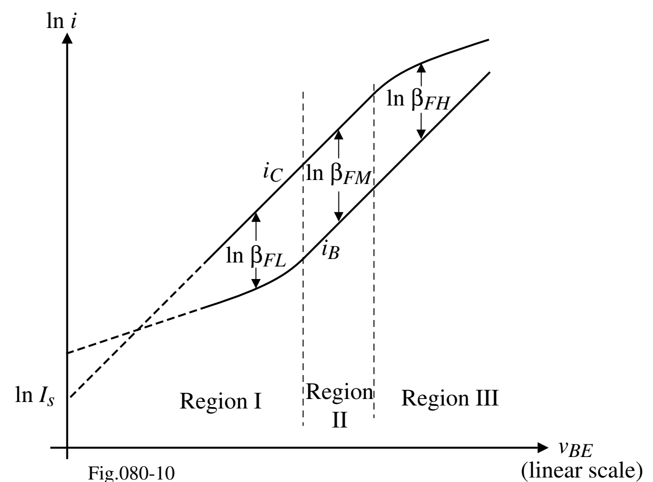
Region I:

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_t}\right) \quad \text{and } i_{BX} = I_{SX} \exp\left(\frac{v_{BE}}{mV_t}\right)$$

due to recombination, $m \approx 2$

1.) $$\beta_{FL} = \frac{i_C}{i_{BX}} = \frac{I_S}{I_{SX}} \exp\left[\frac{v_{BE}}{V_t}\left(1 - \frac{1}{m}\right)\right]$$

$$\approx \frac{I_S}{I_{SX}}\left(\frac{i_C}{I_s}\right)^{[1-(1/m)]} \quad \text{for } m = 2,\ \beta_{FL} \propto \sqrt{i_C}$$



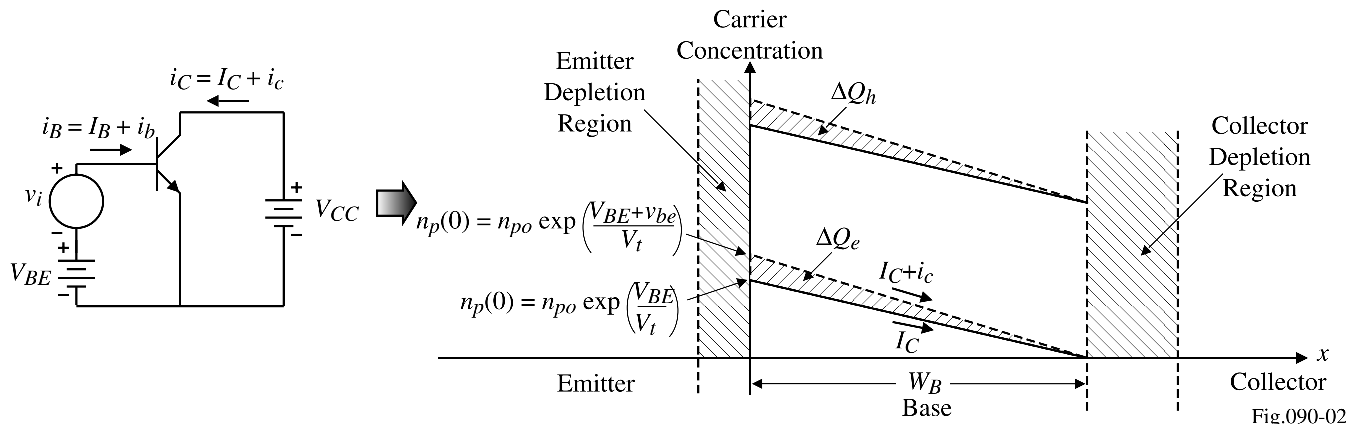
Region III:

$$i_C = I_{SH} \exp\left(\frac{v_{BE}}{2V_t}\right) \text{ due to the high level injection} \quad \text{and } i_B \approx \frac{I_S}{\beta_{FM}} \exp\left(\frac{v_{BE}}{V_t}\right)$$

$$\beta_{FH} \approx \frac{I_{SH}}{I_S} \beta_F \exp\left(- \frac{v_{BE}}{2V_t}\right) \approx \frac{I_{SH}^2}{I_S} \beta_{FM} \frac{1}{i_C}$$

BJT, Common-Emitter, Forward-Active Region

Effect of a small-signal input voltage applied to a BJT.



An increase in v_{BE} (v_i) causes more electrons to be injected in the base increasing the base current i_B by an amount i_b. The increased base current causes the collector current i_C to increase by an amount i_c.

$$v_i \quad \Rightarrow \quad i_b \quad \Rightarrow \quad i_c$$

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Transconductance of the Small Signal BJT Model

The small signal transconductance is defined as

$$g_m \equiv \frac{di_C}{dv_{BE}}\bigg|_Q = \frac{\Delta i_C}{\Delta v_{BE}} = \frac{i_c}{v_{be}} = \frac{i_c}{v_i} \qquad \Rightarrow \qquad i_c = g_m v_i$$

The large signal model for i_C is

$$i_C = I_S \exp\frac{v_{BE}}{V_t} \qquad \Rightarrow \quad g_m = \left(\frac{d}{dv_{BE}} I_S \exp\frac{v_{BE}}{V_t}\right)\bigg|_Q = \frac{I_S}{V_t} \exp\frac{V_{BE}}{V_t} = \frac{I_C}{V_t}$$

$$\therefore \qquad \boxed{g_m = \frac{I_C}{V_t}}$$

Another way to develop the small signal transconductance

$$i_C = I_S \exp\left(\frac{V_{BE}+v_i}{V_t}\right) = I_S \exp\left(\frac{V_{BE}}{V_t}\right) \exp\left(\frac{v_i}{V_t}\right) = I_C \exp\left(\frac{v_i}{V_t}\right) \approx I_C\left[1 + \frac{v_i}{V_t} + \frac{1}{2}\left(\frac{v_i}{V_t}\right)^2 + \frac{1}{6}\left(\frac{v_i}{V_t}\right)^3 + \cdots\right]$$

But

$$i_C = I_C + i_c$$

$$\therefore \quad i_c \approx I_C \frac{v_i}{V_t} + \frac{I_C}{2}\left(\frac{v_i}{V_t}\right)^2 + \frac{I_C}{6}\left(\frac{v_i}{V_t}\right)^3 + \cdots \approx \frac{I_C}{V_t} v_i = g_m v_i$$

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Input Resistance of the Small Signal BJT Model

In the forward-active region, we can write that

$$i_B = \frac{i_C}{\beta_F}$$

Small changes in i_B and i_C can be related as

$$\Delta i_B = \frac{d}{di_C}\left(\frac{i_C}{\beta_F}\right)\Delta i_C$$

The small signal current gain, β_o, can be written as

$$\beta_o = \frac{\Delta i_C}{\Delta i_B} = \frac{1}{\frac{d}{di_C}\left(\frac{i_C}{\beta_F}\right)} = \frac{i_c}{i_b}$$

Therefore, we define the small signal input resistance as

$$r_\pi \equiv \frac{v_i}{i_b} = \frac{\beta_o v_i}{i_c} = \frac{\beta_o}{g_m}$$

$$\boxed{r_\pi = \frac{\beta_o}{g_m}}$$

Output Resistance of the Small Signal BJT Model

In the forward-active region, we can write that the small signal output conductance, g_o ($r_o = 1/g_o$) as

$$g_o \equiv \frac{di_C}{dv_{CE}}\Big|_Q = \frac{\Delta i_C}{\Delta v_{CE}} = \frac{i_c}{v_{ce}} \qquad \Rightarrow \qquad i_c = g_o v_{ce}$$

The large signal model for i_C , including the influence of v_{CE}, is

$$i_C = I_S\left(1 + \frac{v_{CE}}{V_A}\right)\exp\frac{v_{BE}}{V_t}$$

$$g_o \equiv \frac{di_C}{dv_{CE}}\Big|_Q = I_S\left(\frac{1}{V_A}\right)\exp\frac{V_{BE}}{V_t} \approx \frac{I_C}{V_A}$$

$$\therefore \qquad \boxed{r_o = \frac{V_A}{I_C}}$$

Simple Small Signal BJT Model

Implementing the above relationships, $i_c = g_m v_i$, $i_c = g_o v_{ce}$, and $v_i = r_\pi i_b$, into a schematic model gives,

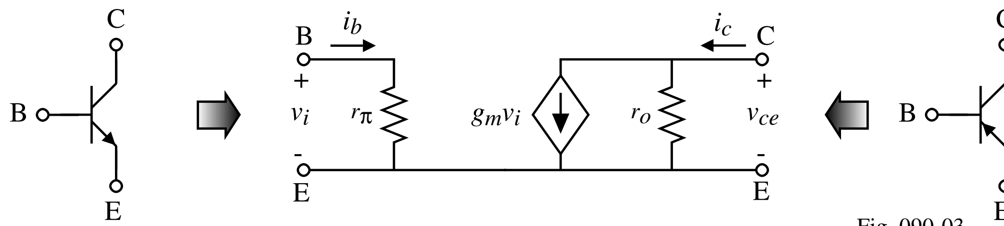

Fig. 090-03

Note that the small signal model is the same for either a *npn* or a *pnp* BJT.

Example:

Find the small signal input resistance, R_{in}, the output resistance, R_{out}, and the voltage gain of the common emitter BJT if the BJT is unloaded ($R_L = \infty$), v_{out}/v_{in}, the dc collector current is 1mA, the Early voltage is 100V, and β_o at room temperature.

$$g_m = \frac{I_C}{V_t} = \frac{1\text{mA}}{26\text{mV}} = \frac{1}{26}\text{ mhos} \qquad R_{in} = r_\pi = \frac{\beta_o}{g_m} = 100 \cdot 26 = 2.6\text{k}\Omega$$

$$R_{out} = r_o = \frac{V_A}{I_C} = \frac{100\text{V}}{1\text{mA}} = 100\text{k}\Omega \qquad \frac{v_{out}}{v_{in}} = -g_m\, r_o = -\,26\text{mS}\cdot 100\text{k}\Omega = -2600\text{V/V}$$

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EXTENSIONS OF THE SMALL SIGNAL BJT MODEL

Collector-Base Resistance of the Small Signal BJT Model

Recall the influence of V on the base width:

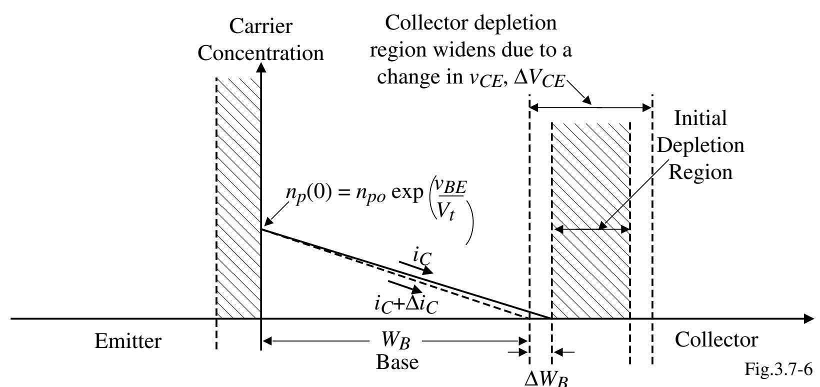

Fig.3.7-6

We noted that an increase in v_{CE} causes and increase in the depletion width and a decrease in the total minority-carrier charge stored in the base and therefore a decrease in the base recombination current, i_{B1}.

This influence is modeled by a collector-base resistor, r_μ, defined as

$$r_\mu = \frac{\Delta v_{CE}}{\Delta i_{B1}} = \frac{\Delta v_{CE}}{\Delta i_C}\frac{\Delta i_C}{\Delta i_{B1}} = r_o\frac{\Delta i_C}{\Delta i_{B1}} \approx \beta_o r_o \quad \text{(if base current is primarily recomb.)}$$

In general, $r_\mu \geq 10\ \beta_o r_o$ for the *npn* BJT and about 2-5 $\beta_o r_o$ for the lateral *pnp* BJT.

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Base-Charging Capacitance of the Small Signal BJT Model

Consider changes in base-carrier concentrations once again.

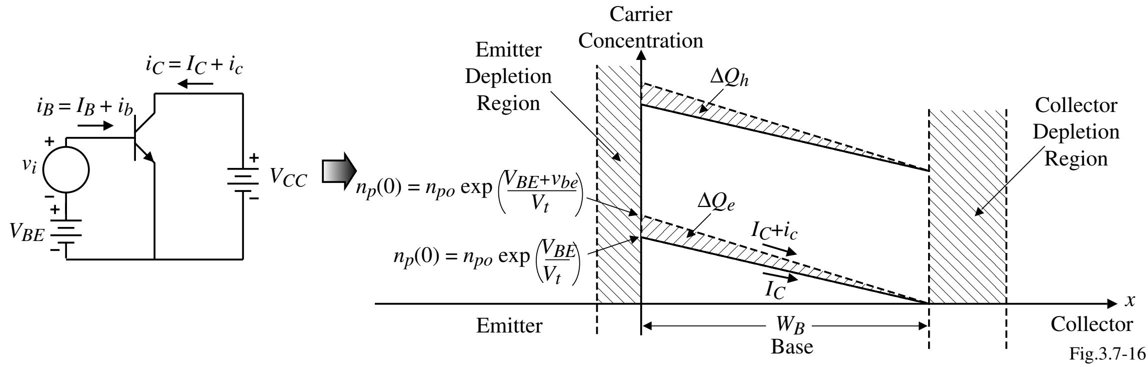

Fig.3.7-16

The Δv_{BE} change causes a change in the minority carriers, $\Delta Q_e = q_e$, which must be equal to the change in majority carriers, $\Delta Q_h = q_h$. This charge can be related to the voltage across the base, v_i, as

$$q_h = C_b v_i$$

where C_b is the base-charging capacitor and is given as

$$C_b = \frac{q_h}{v_i} = \frac{\tau_F\, i_c}{v_i} = \tau_F\, g_m = \tau_F \frac{I_C}{V_t}$$

The base transit time τ_F is defined as $\dfrac{W_B{}^2}{2D_n}$

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Parasitic Elements of the BJT Small Signal Model

Typical cross-section of the *npn* BJT:

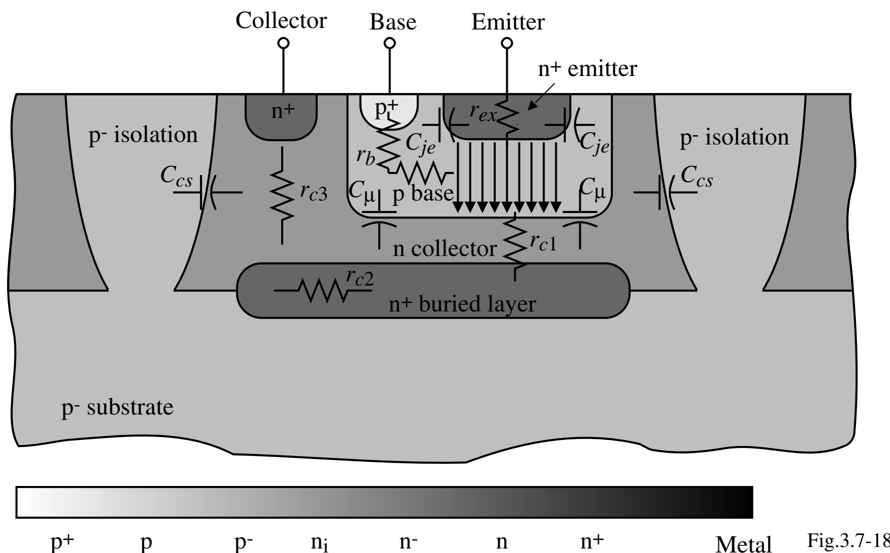

Fig.3.7-18

C_{je} = base-emitter depletion capacitance (forward biased)

$$C_\mu = \frac{C_{\mu 0}}{\left(1 - \dfrac{v_{CB}}{\psi_0}\right)^m} = \text{collector-base depletion capacitance (reverse biased)}$$

Resistances are all bulk ohmic resistances. r_b, r_c, and r_{ex} are important. Also, $r_b = f(I_C)$.

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Complete Small Signal BJT Model

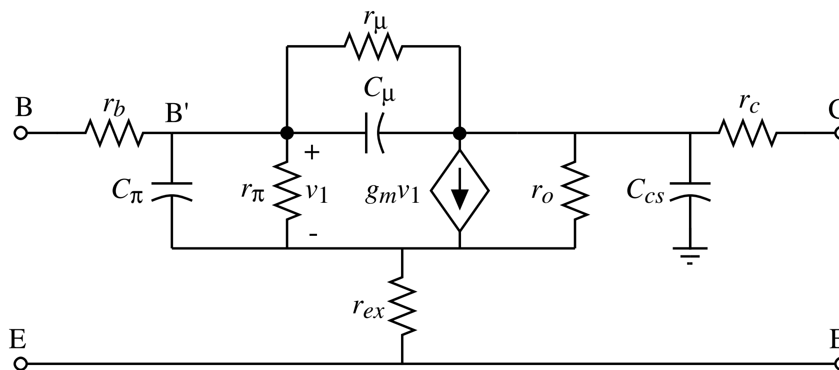

Fig. 3.7-19

The capacitance, C_π, consists of the sum of C_{je} and C_b.

$$C_\pi = C_{je} + C_b$$

Example

Derive the complete small signal equivalent circuit for a BJT at I_C = 1mA, V_{CB} = 3V, and V_{CS} = 5V. The device parameters are $Cje0$ = 10fF, n_e = 0.5, ψ_{0e} = 0.9V, $C_{\mu 0}$ = 10fF, n_c = 0.3, ψ_{0c} = 0.5V, C_{cs0} = 20fF, n_s = 0.3, ψ_{0s} = 0.65V, β_o = 100, τ_F = 10ps, V_A = 20V, r_b = 300Ω, r_c = 50Ω, r_{ex} = 5Ω, and $r_\mu = 10\beta_o r_o$.

Solution

Because C_{je} is difficult to determine and usually an insignificant part of C_π, let us approximate it as $2C_{je0}$.

$$C_{je} = 20\text{fF}$$

$$C_\mu = \frac{C_{\mu 0}}{\left(1+\frac{V_{CB}}{\psi_{0c}}\right)^{n_e}} = \frac{10\text{fF}}{\left(1+\frac{3}{0.5}\right)^{0.3}} = 5.6\text{fF} \quad \text{and} \quad C_{cs} = \frac{C_{cs0}}{\left(1+\frac{V_{CS}}{\psi_{0s}}\right)^{n_s}} = \frac{20\text{F}}{\left(1+\frac{5}{0.65}\right)^{0.3}} = 10.5\text{fF}$$

$$g_m = \frac{I_C}{V_t} = \frac{1\text{mA}}{26\text{mV}} = 38\text{mA/V} \qquad C_b = \tau_F\, g_m = (10\text{ps})(38\text{mA/V}) = 0.38\text{pF}$$

$$C_\pi = C_b + C_{je} = 0.38\text{pF}+0.02\text{pF} = 0.4\text{pF}$$

$$r_\pi = \frac{\beta_o}{g_m} = 100\cdot 26\Omega = 2.6\text{k}\Omega,\ r_o = \frac{V_A}{I_C} = \frac{20\text{V}}{1\text{mA}} = 20\text{k}\Omega,\ \text{and}\ r_\mu = 10\beta_o r_o = 10\cdot 100\cdot 20\text{k}\Omega = 20\text{M}\Omega$$

FREQUENCY RESPONSE OF THE BJT

Transition Frequency, f_T

f_T is the frequency where the magnitude of the short-circuit, common-emitter current equal unity.

Circuit and model:

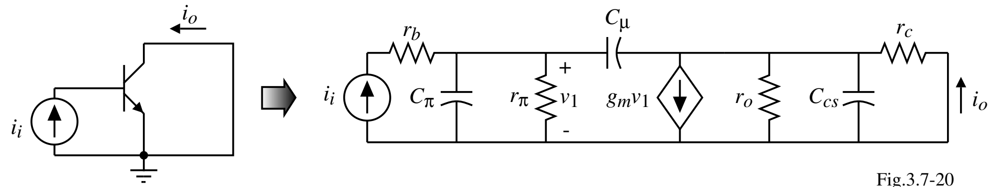

Fig.3.7-20

Assume that $r_c \approx 0$. As a result, r_o and C_{cs} have no effect.

$$\therefore \; V_1 \approx \frac{r_\pi}{1 + r_\pi (C_\pi + C_b)s} I_i \quad \text{and} \quad I_o \approx g_m V_1 \Rightarrow \frac{I_o(j\omega)}{I_i(j\omega)} = \frac{g_m r_\pi}{1 + g_m r_\pi \frac{(C_\pi + C_b)s}{g_m}} = \frac{\beta_o}{1 + \beta_o \frac{(C_\pi + C_b)s}{g_m}}$$

Now,

$$\beta(j\omega) = \frac{I_o(j\omega)}{I_i(j\omega)} = \frac{\beta_o}{1 + \beta_o \frac{(C_\pi + C_b)j\omega}{g_m}}$$

At high frequencies,

$$\beta(j\omega) \approx \frac{g_m}{j\omega\,(C_\pi + C_b)} \Rightarrow \text{ When } |\beta(j\omega)| = 1 \text{ then } \omega_T = \frac{g_m}{C_\pi + C_b} \text{ or } f_T = \frac{1}{2\pi} \frac{g_m}{C_\pi + C_b}$$

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Illustration of the BJT Transition Frequency

β as a function of frequency:

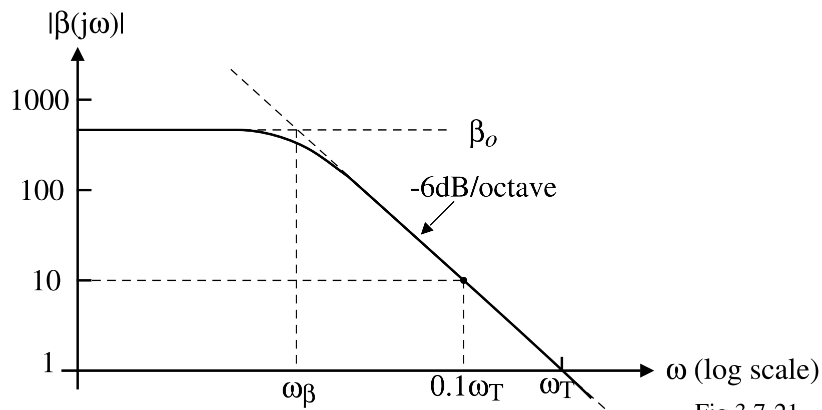

Fig.3.7-21

Note that the product of the magnitude and frequency at any point on the –6dB/octave curve is equal to ω_T.

For example,

$$0.1\ \omega_T \text{ x}10 = \omega_T$$

In measuring ω_T, the value of $|\beta(j\omega)|$ is measured at some frequency less than ω_T (say ω_x) and ω_T is calculated by taking the product of $|\beta(j\omega_x)|$ and ω_x to get ω_T.

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Current Dependence of f_T

Note that $\tau_T = \dfrac{1}{\omega_T} = \dfrac{C_\pi}{g_m} + \dfrac{C_\mu}{g_m} = \dfrac{C_b}{g_m} + \dfrac{C_{je}}{g_m} + \dfrac{C_\mu}{g_m} = \tau_F + \dfrac{C_{je}}{g_m} + \dfrac{C_\mu}{g_m}$

At low currents, the C_{je} and C_μ terms dominate causing τ_T to rise and ω_T to fall.

At high currents, τ_T approaches τ_F which is the maximum value of ω_T.

For further increases in collector current, ω_T decreases because of high-level injection effects and the Kirk effect.

Typical frequency dependence of f_T:

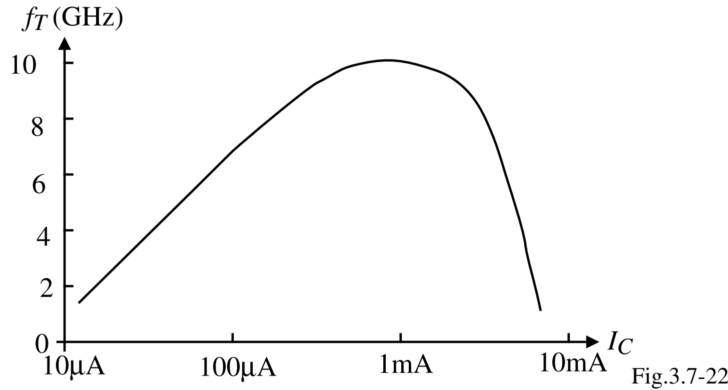
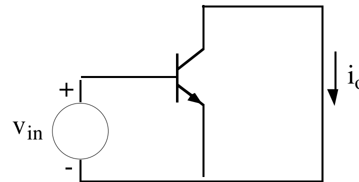


Fig.3.7-22

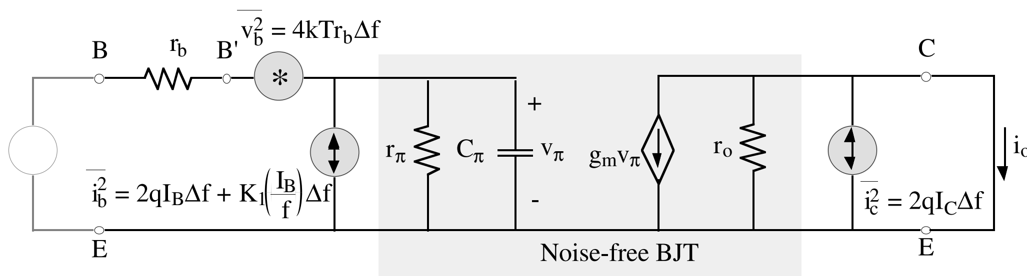
NOISE MODEL FOR THE BJT

Model Development

Consider the BJT in the following mode of operation:



Add all internal noise sources to the BJT small signal model to get:



where

$\overline{v_b^2}$ = thermal noise of the base resistance

$\overline{i_b^2}$ = base shot and flicker noise currents

and

$\overline{i_c^2}$ = collector shot and flicker noise currents

Equivalent BJT Noise Model

Find an equivalent input noise current, $\overline{i_i^2}$, and input noise voltage, $\overline{v_i^2}$, given as:

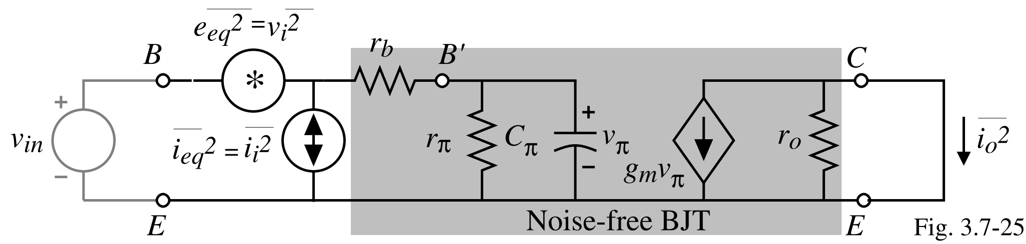


Fig. 3.7-25

To find $\overline{i_i^2}$ and $\overline{v_i^2}$, perform the following steps:

1.) Short circuit the input and find $\overline{i_o^2}$ of both models and equate to get $\overline{v_i^2}$.

2,) Open circuit the input and find $\overline{i_o^2}$ of both models and equate to get $\overline{i_i^2}$.

Calculations:

1,) Short circuit the input (assume $r_b << r_\pi$)

Ckt 1: $\overline{i_o^2} = g_m{}^2\,\overline{v_b^2} + \overline{i_c^2}$

Ckt 2: $\overline{i_o^2} = g_m{}^2\,\overline{v_i^2}$

$$\overline{v_{eq}^2} = \overline{v_i^2} = \overline{v_b^2} + \frac{\overline{i_c^2}}{g_m^2}$$

Equivalent BJT Noise Model – Continued

2.) Open circuit the input (assume $r_b << r_\pi$)

Circuit 1:

$$\overline{i_o^2} = \overline{i_c^2} + g_m^2\left(\frac{\frac{r_\pi}{sC_\pi}}{r_\pi + \frac{1}{sC_\pi}}\right)^2 \overline{i_b^2} = \overline{i_c^2} + g_m^2 r_\pi^2\left(\frac{1}{sr_\pi C_\pi+1}\right)^2 \overline{i_b^2}$$

$$\overline{i_o^2} = \overline{i_c^2} + \beta_o^2\left(\frac{1}{\frac{s}{\omega_\beta}+1}\right)^2 \overline{i_b^2} = \overline{i_c^2} + |\beta(j\omega)|^2\, \overline{i_b^2}$$

Circuit 2:

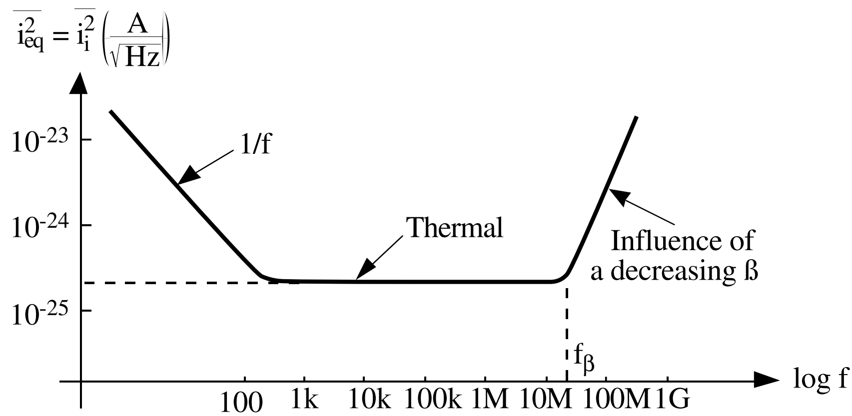
$$\overline{i_o^2} = |\beta(j\omega)|^2\, \overline{i_i^2}$$

Equating the above results gives

$$\overline{i_{eq}^2} = \overline{i_i^2} = \overline{i_b^2} + \frac{\overline{i_c^2}}{|\beta(j\omega)|^2} = 2qI_B\Delta f + \frac{K_1 I_B \Delta f}{f} + \frac{2qI_C\Delta f}{|\beta(j\omega)|^2}$$

Frequency Dependence of the BJT Noise Model

Frequency response of $\overline{i_i^1}$ or $\overline{i_{eq}^2}$,



Thermal Noise due to Parasitic Resistances

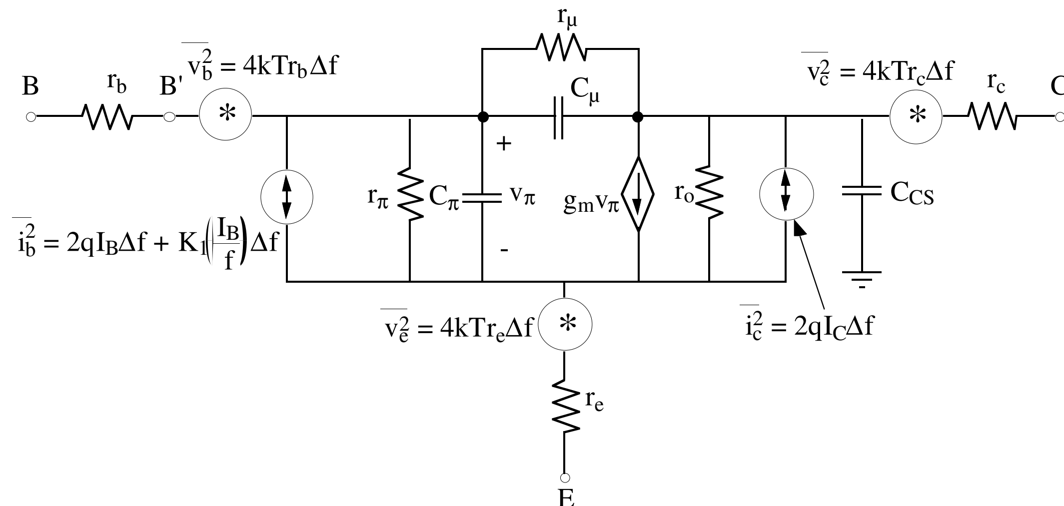
$$\overline{v_c^2} = 4kTr_c/Area$$

$$\overline{v_e^2} = 4kTr_c/Area$$

and

$$\overline{v_b^2} = 4kTr_b/Area \text{ (already included)}$$

Modified BJT noise model:



COMPARISON OF THE MOS AND BIPOLAR TRANSISTORS

Quantity	MOS Transistor	Bipolar Transistor
Intrinsic Gain	$\sqrt{\frac{2K'W}{\lambda^2 L I_D}} \propto \sqrt{\frac{1}{I_D}}$	$\frac{V_A}{V_t}$
ω_T	$\frac{g_m}{C_{gs}} = \frac{3}{2C_{ox}}\sqrt{\frac{2K'I_D}{WL^3}}$	$\frac{1}{\tau_F}$
Input Noise Voltage (V^2/Hz)	$\frac{8kT}{3g_m} + \frac{K'}{WLC_{ox}f}$	$4kTr_b + \frac{2qI_C}{g_m^2}$
Input Noise Current (A^2/Hz)	0	$2q\left[I_B + K_1\frac{I_B{}^a}{f} + \frac{I_C}{\lvert\beta(j\omega)\rvert^2}\right]$
Input Offset Voltage	$\Delta V_T + \frac{V_{GS}-V_T}{2}\left[-\frac{\Delta R}{R} - \frac{\Delta(W/L)}{W/L}\right]$	$\frac{kT}{q}\left[-\frac{\Delta R}{R} - \frac{\Delta A_E}{A_E} - \frac{\Delta Q_B}{Q_B}\right]$
R_{out}	$\frac{1}{\lambda I_D}$	$\frac{V_A}{I_C}$
R_{in}	∞	r_π
g_m	$\sqrt{\frac{2K'WI_D}{L}}$	$\frac{I_C}{V_t}$

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SEC. 3.8 – SPICE LEVEL 2 MODEL

SECOND-ORDER EFFECTS IN THE LARGE SIGNAL MODEL

Derivation of the Second-Order Model

Consider the following illustration of a MOSFET in the active region:

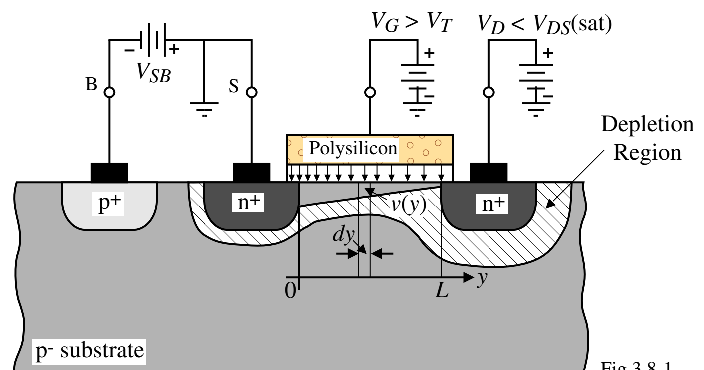

Fig.3.8-1

Assume, the charge in the depletion region between the channel and bulk is no longer constant and is dependent on $v(y)$. Therefore, we model the dependence of threshold voltage, V_T, on y as

$$V_T(y) = VT0 + \gamma\left[\sqrt{2|\phi_F| + v_{CB}} - \sqrt{2\phi_F}\right]$$

where v_{CB} is the voltage across the depletion region at y and is expressed as

$$v_{CB} = v_S + v(y) - v_B = v(y) + v_{SB}$$

$$\therefore \quad V_T(y) = VT0 + \gamma\left[\sqrt{2|\phi_F| + v(y) + v_{SB}} - \sqrt{2\phi_F}\right]$$

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Derivation of the Second-Order Model – Continued

Now we repeat the previous analysis using this expression for V_T.

The charge in the inversion layer was written as,

$$Q_I(y) = C_{ox}[v_{GS} - v(y) - V_T(y)] = C_{ox}\left[v_{GS} - v(y) - V_{T0} - \gamma\sqrt{2|\phi_F| + v(y) + v_{SB}} + \sqrt{2\phi_F}\right]$$

Using Ohm's law for an increment, dy, of channel, we can write

$$dv(y) = i_D dR = \frac{i_D dy}{\mu_n Q_I(y) W} \qquad \Rightarrow \qquad i_D dy = \mu_n W Q_I(y) dv(y)$$

Integrating this result over the channel from source to drain gives,

$$i_D = \int_0^L dy = \mu_n W C_{ox} \int_0^{v_{DS}} \left[v_{GS} - v(y) - V_{T0} - \gamma\sqrt{2|\phi_F| + v(y) + v_{SB}} + \sqrt{2\phi_F}\right] dv$$

Evaluating the limits gives,

$$i_D L = \mu_n W C_{ox}\left[\left(v_{GS} - V_{T0} + \gamma\sqrt{2|\phi_F|} - \frac{v_{DS}}{2}\right)v_{DS} - \frac{2}{3}\gamma\left(2|\phi_F| + v_{SB} + v_{DS}\right)^{1.5} + \frac{2}{3}\gamma\left(2|\phi_F| + v_{SB}\right)^{1.5}\right]$$

or $$i_D = \frac{\mu_n W C_{ox}}{L}\left[\left(v_{GS} - V_{T0} + \gamma\sqrt{2|\phi_F|} - \frac{v_{DS}}{2}\right)v_{DS} - \frac{2}{3}\gamma\left(2|\phi_F| + v_{SB} + v_{DS}\right)^{1.5} + \frac{2}{3}\gamma\left(2|\phi_F| + v_{SB}\right)^{1.5}\right]$$

These results agree with the first edition of the text if the following definitions are made:

$$V_{BIN} \approx V_{T0} - \gamma\sqrt{2|\phi_F|}, \qquad \theta \approx 1 \qquad \text{and} \qquad \frac{\pi\varepsilon_{si}}{4C_{ox}W} \approx 1$$

SECOND-ORDER EFFECTS DUE TO SMALL GEOMETRIES

Second-Order Effects

1.) Mobility degradation, μ_s

2.) Corrected threshold voltage, V_{BIN}

3.) Corrected bulk threshold parameter, γ_s

4.) Effective channel length, L_{mod}

New model:

$$i_D = \frac{\boldsymbol{\mu_s} W C_{ox}}{\boldsymbol{L_{mod}}}\left\{\left[v_{GS} - \boldsymbol{V_{BIN}} - \frac{\theta v_{DS}}{2}\right]v_{DS} - \frac{2}{3}\boldsymbol{\gamma_s}\left[\left(2|\phi_F| + v_{SB} + v_{DS}\right)^{1.5} + \left(2|\phi_F| + v_{SB}\right)^{1.5}\right]\right\}$$

Mobility Degradation

The degradation of the surface mobility μ_o can be written as

$$\mu_s = \mu_o \left[\frac{UCRIT \cdot \varepsilon_{si}}{C_{ox}\,[v_{GS} - V_T - UTRA \cdot v_{DS}]} \right]^{UEXP}$$

where

$UCRIT$ = Critical field for mobility degradation (Volts/cm)

$UTRA$ = Transverse field coefficient for mobility degradation

$UEXP$ = Critical field exponent for mobility degradation

Normally, $\mu_s \le \mu_o$

Corrected Threshold Voltage

The corrected built-in threshold voltage for short channel transistors can be expressed as

$$V_{BIN} = V_{FB} + 2\phi_F + \Delta \frac{\pi \varepsilon_{si}}{4C_{ox}W} (2\phi F - |v_{BS}|)$$

where

Δ = an empirical channel width factor which adjusts the threshold voltage

$$\theta = 1 + \frac{\pi \varepsilon_{si}}{4C_{ox}W}$$

Corrected Bulk Threshold Parameter

Consider the following geometrical situation for short channels:

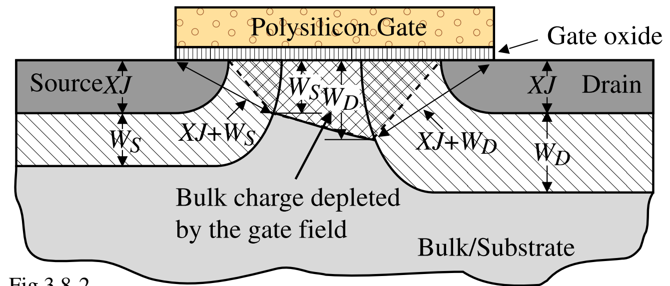


Fig.3.8-2

Define the corrected bulk threshold parameter as

$$\gamma_s = \gamma(1 - \alpha_S - \alpha_D)$$

where

$$\alpha_S = \frac{XJ}{2L}\left(\sqrt{1+\frac{2W_S}{XJ}} - 1\right)$$

$$\alpha_D = \frac{XJ}{2L}\left(\sqrt{1+\frac{2W_D}{XJ}} - 1\right)$$

where

XJ = metallurgical junction depth (meters)

$$W_S = \text{source depletion width} = \sqrt{\frac{2\varepsilon_{si}}{q\cdot NSUB}(2\phi_F + |v_{SB}|)\,)}$$

$$W_D = \text{Drain depletion width} = \sqrt{\frac{2\varepsilon_{si}}{q\cdot NSUB}(2\phi_F + |v_{SB}| + v_{DS})\,)}$$

Effective Channel Length

Effective channel length, L_{mod} can be expressed as,

$$L_{mod} = L_{eff}(1 - \lambda v_{DS})$$

where

$$L_{eff} = L - 2\cdot XJ\cdot LD$$

LD = lateral diffusion

$$\lambda = \frac{1}{L_{eff}v_{DS}}\sqrt{\frac{2\varepsilon si}{q\cdot NSUB}}\sqrt{\frac{v_{DS}-v_{DS}(\text{sat})}{4} + \sqrt{1+\left(\frac{v_{DS}-v_{DS}(\text{sat})}{4}\right)^2}}$$

and

$$v_{DS}(\text{sat}) = \frac{v_{GS}-V_{BIN}}{\theta} + \frac{\gamma_s^2}{2\theta^2}\left[1 - \sqrt{1+\frac{\theta^2}{\gamma_s^2}\left(\frac{v_{GS}-V_{BIN}}{\theta} + 2\phi_F + |v_{BS}|\right)}\right]$$

Other short channel effects not considered here:

- Saturation due to scattering-limited velocity
- Hot electron effects

SEC. 3.9 – MODELS FOR SIMULATION OF MOS CIRCUITS

FET Model Generations

- First Generation – Physically based analytical model including all geometry dependence.
- Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
- Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

Performance Comparison of Models (from Cheng and Hu, *MOSFET Modeling & BSIM3 Users Guide*)

Model	Minimum L (μm)	Minimum Tox (nm)	Model Continuity	i_D Accuracy in Strong Inversion	i_D Accuracy in Subthreshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not Modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

First Generation Models

Level 1 (MOS1)

- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift)

Level 2 (MOS2)

- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a “developing ground” for better modeling techniques.

Level 3 (MOS3)

- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.

Second Generation Models

BSIM (Berkeley Short-Channel IGFET Model)

- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
- Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28

- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2

- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design
- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature

Third Generation Models

BSIM3

- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

MOS Model 9

- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

Other Candidates

- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design

BSIM2 Model

Generic composite expression for the model parameters:

$$X = X_o + \frac{LX}{L_{eff}} + \frac{WX}{W_{eff}}$$

where

X_o = parameter for a given W and L

LX (WX) = first-order dependence of X on L (W)

Modeling features of BSIM2:

Mobility

- Mobility reduction by the vertical field
- Mobility reduction by the lateral field

Drain Current

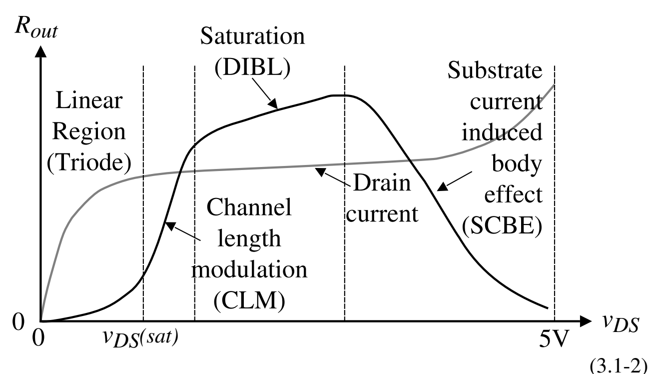
- Velocity saturation
- Linear region drain current
- Saturation region drain current
- Subthreshold current

$$i_{DS} = \frac{\mu_o C_{ox} W_{eff}}{L_{eff}} \cdot \left(\frac{kT}{q}\right) \frac{e^{v_{GS}-V_t-V_{off}}}{n} \cdot \left[1 - e^{qV_{DS}/kT}\right]$$

where

$$V_{off} = VOF + VOFB \cdot v_{BS} + VOFD \cdot v_{DS} \quad \text{and} \quad n = NO + \frac{NB}{\sqrt{PHI - v_{BS}}} + ND \cdot v_{DS}$$

BSIM2 Output Conductance Model



(3.1-2)

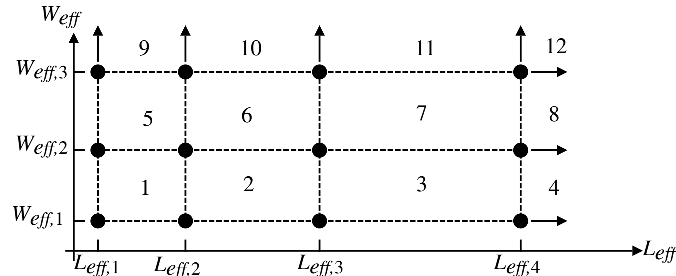
- Drain-Induced Barrier Lowering (DIBL) – Lowering of the potential barrier at the source-bulk junction allowing carriers to traverse the channel at a lower gate bias than would otherwise be expected.
- Substrate Current-Induced Body Effect (SCBE) – The high field near the drain accelerates carriers to high energies resulting in impact ionization which generates a hole-electron pair (hot carrier generation). The opposite carriers are swept into the substrate and have the effect of slightly forward-biasing the source-substrate junction. This reduces the threshold voltage and increases the drain current.

Charge Model

- Eliminates the partitioning choice (50%/50% is used)
- BSIM charge model better documented with more options

BSIM2 Basic Parameter Extraction

- A number of devices with different W/L are fabricated and measured



- A long, wide device is used as the base to add geometry effects as corrections.
- Procedure:

1.) Oxide thickness and the differences between the drawn and effective channel dimensions are provided as process input.

2.) A long, wide device is used to determine some base parameters which are used as the starting point for each individual device extraction in the second phase.

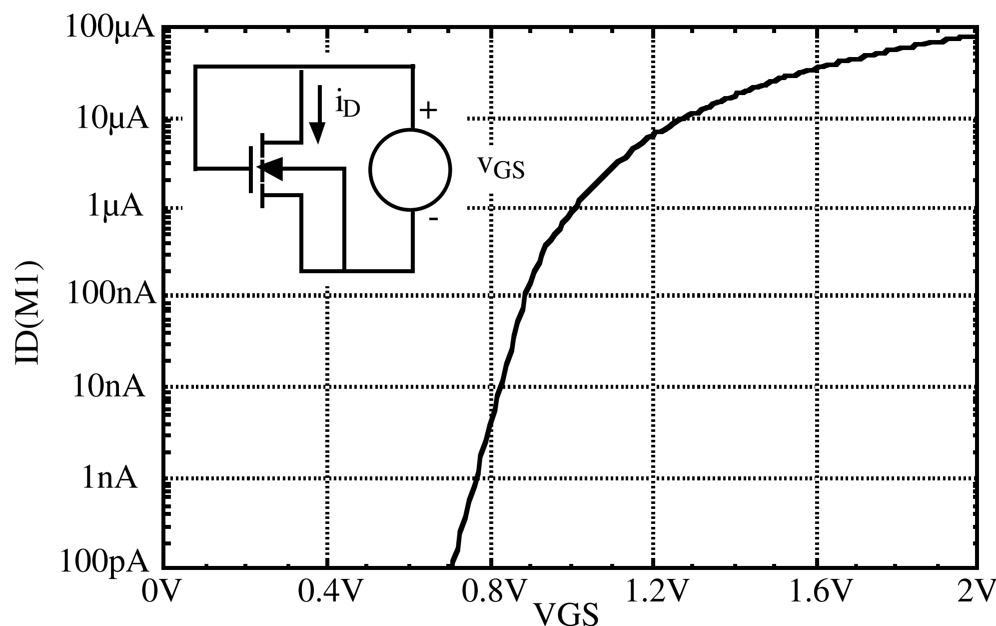
3.) In the second phase, a set of parameters is extracted independently for each device. This phase represents the fitting of the data for each independent device to the intrinsic equation structure of the model

2.) In the third phase, the compiled parameters from the second phase are used to determine the geometry parameters. This represents the imposition of the extrinsic structure onto the model.

BSIM2 Model used in Subthreshold

```
BSIM Model Parameters used in Subthreshold
VDS 1 0 DC 3.0
M1 1 1 0 0 CMOSN W=5UM L=2UM
.MODEL CMOSN NMOS LEVEL=4
+VFB=-7.92628E-01      LVFB= 1.22972E-02      WVFB=-1.00233E-01
+PHI= 7.59099E-01      LPHI= 0.00000E+00      WPHI= 0.00000E+00
+K1= 1.06705E+00       LK1= 5.08430E-02       WK1= 4.72787E-01
+K2=-4.23365E-03       LK2= 6.76974E-02       WK2= 6.27415E-02
+ETA=-4.30579E-03      LETA= 9.05179E-03      WETA= 7.33154E-03
+MUZ= 5.58459E+02      DL=6.86137E-001        DW=-1.04701E-001
+U0= 5.52698E-02       LU0= 6.09430E-02       WU0=-6.91423E-02
+U1= 5.38133E-03       LU1= 5.43387E-01       WU1=-8.63357E-02
+X2MZ= 1.45214E+01     LX2MZ=-3.08694E+01     WX2MZ= 4.75033E+01
+X2E=-1.67104E-04      LX2E=-4.75323E-03      WX2E=-2.74841E-03
+X3E= 5.33407E-04      LX3E=-4.69455E-04      WX3E=-5.26199E-03
+X2U0= 2.45645E-03     LX2U0=-1.46188E-02     WX2U0= 2.63555E-02
+X2U1=-3.80979E-04     LX2U1=-1.71488E-03     WX2U1= 2.23520E-02
+MUS= 5.48735E+02      LMUS= 3.28720E+02      WMUS= 1.35360E+02
+X2MS= 6.72261E+00     LX2MS=-3.48094E+01     WX2MS= 9.84809E+01
+X3MS=-2.79427E+00     LX3MS= 6.31555E+01     WX3MS=-1.99720E-01
+X3U1= 1.18671E-03     LX3U1= 6.13936E-02     WX3U1=-3.49351E-03
+TOX=4.03000E-002      TEMP= 2.70000E+01      VDD= 5.00000E+00
+CGDO=4.40942E-010     CGSO=4.40942E-010      CGBO=6.34142E-010
+XPART=-1.00000E+000
+N0=1.00000E+000       LN0=0.00000E+000       WN0=0.00000E+000
+NB=0.00000E+000       LNB=0.00000E+000       WNB=0.00000E+000
+ND=0.00000E+000       LND=0.00000E+000       WND=0.00000E+000
+RSH=0 CJ=4.141500e-04 CJSW=4.617400e-10      JS=0    PB=0.8
+PBSW=0.8    MJ=0.4726      MJSW=0.3597       WDF=0   DELL=0
.DC VDS 5.0 0 0.01
.PRINT DC ID(M1)
.PROBE
.END
```

Results of the BSIM2 Model Simulation in Subthreshold



BSIM3 Model

The background for the BSIM3 model and the equations are given in detail in the text *MOSFET Modeling & BSIM3 User's Guide*, by Y. Cheng and C. Hu, Kluwer Academic Publishers, 1999.

The short channel effects included in the BSIM3 model are:

- Normal and reverse short-channel and narrow-width effects on the threshold.
- Channel length modulation (*CLM*).
- Drain induced barrier lowering (*DIBL*).
- Velocity saturation.
- Mobility degradation due to the vertical electric field.
- Impact ionization.
- Band-to-band tunnelling.
- Velocity overshoot.
- Self-heating.

1.) Channel quantiztion.

2.) Polysilicon depletion.

BSIM3v3 Model Equations for Hand Calculations

In strong inversion, approximate hand equations are:

$$i_{DS} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \frac{1}{1+\frac{v_{DS}}{E_{sat}L_{eff}}} \left(v_{GS} - V_{th} - \frac{A_{bulk}v_{DS}}{2}\right) v_{DS}\ , \qquad v_{DS} < V_{DS}(\text{sat})$$

$$i_{DS} = W_{eff} v_{sat} C_{ox} [v_{GS} - V_{th} - A_{bulk}V_{DS}(\text{sat})] \left(1+\frac{v_{DS} - V_{DS}(\text{sat})}{V_A}\right), \qquad v_{DS} > V_{DS}(\text{sat})$$

where

$$V_{DS}(\text{sat}) = \frac{E_{sat}L_{eff}(v_{GS}-V_{th})}{A_{bulk}E_{sat}L_{eff} + (v_{GS}-V_{th})}$$

$L_{eff} = L_{drawn} - 2dL$

$W_{eff} = W_{drawn} - 2dW$

E_{sat} = Electric field where the drift velocity (v) saturates

v_{sat} = saturation velocity of carriers in the channel

$$\mu = \frac{\mu_{eff}}{1+(E_y/E_{sat})} \Rightarrow \qquad \mu_{eff} = \frac{2v_{sat}}{E_{sat}}$$

Note: Assume $A_{bulk} \approx 1$ and extract V_{th} and V_A.

MOSIS Parametric Test Results

http://www.mosis.org/

RUN: T02D VENDOR: TSMC
TECHNOLOGY: SCN025 FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 0251P5M.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.36/0.24			
Vth		0.54	-0.50	volts
SHORT	20.0/0.24			
Idss		557	-256	uA/um
Vth		0.56	-0.56	volts
Vpt		7.6	-7.2	volts
WIDE	20.0/0.24			
Ids0		6.6	-1.5	pA/um
LARGE	50.0/50.0			
Vth		0.47	-0.60	volts
Vjbkd		5.8	-7.0	volts
Ijlk		-25.0	-1.1	pA
Gamma		0.44	0.61	$V^{0.5}$
K' (Uo*Cox/2)		112.0	-23.0	uA/V^2

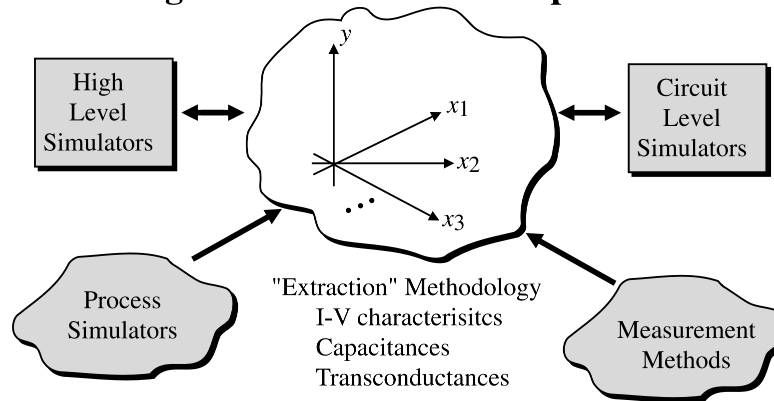
0.25µm BSIM3v3.1 NMOS Parameters

```
.MODEL CMOSN NMOS (                          LEVEL   = 49
+VERSION = 3.1         TNOM    = 27          TOX     = 5.7E-9
+XJ      = 1E-7        NCH     = 2.3549E17   VTH0    = 0.4273342
+K1      = 0.3922983   K2      = 0.0185825   K3      = 1E-3
+K3B     = 2.0947677   W0      = 2.171779E-7 NLX     = 1.919758E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 7.137212E-3 DVT1    = 6.066487E-3 DVT2    = -0.3025397
+U0      = 403.1776038 UA      = -3.60743E-12 UB     = 1.323051E-18
+UC      = 2.575123E-11 VSAT   = 1.616298E5  A0      = 1.4626549
+AGS     = 0.3136349   B0      = 3.080869E-8 B1      = -1E-7
+KETA    = 5.462411E-3 A1      = 4.653219E-4 A2      = 0.6191129
+RDSW    = 345.624986  PRWG    = 0.3183394   PRWB    = -0.1441065
+WR      = 1           WINT    = 8.107812E-9 LINT    = 3.375523E-9
+XL      = 3E-8        XW      = 0           DWG     = 6.420502E-10
+DWB     = 1.042094E-8 VOFF    = -0.1083577  NFACTOR = 1.1884386
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 4.914545E-3 ETAB    = 4.215338E-4
+DSUB    = 0.0313287   PCLM    = 1.2088426   PDIBLC1 = 0.7240447
+PDIBLC2 = 5.120303E-3 PDIBLCB = -0.0443076  DROUT   = 0.7752992
+PSCBE1  = 4.451333E8  PSCBE2  = 5E-10       PVAG    = 0.2068286
+DELTA   = 0.01        MOBMOD  = 1           PRT     = 0
+UTE     = -1.5        KT1     = -0.11       KT1L    = 0
+KT2     = 0.022       UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11    AT      = 3.3E4       WL      = 0
+WLN     = 1           WW      = -1.22182E-16 WWN    = 1.2127
+WWL     = 0           LL      = 0           LLN     = 1
+LW      = 0           LWN     = 1           LWL     = 0
+CAPMOD  = 2           XPART   = 0.4         CGDO    = 6.33E-10
+CGSO    = 6.33E-10    CGBO    = 1E-11       CJ      = 1.766171E-3
+PB      = 0.9577677   MJ      = 0.4579102   CJSW    = 3.931544E-10
+PBSW    = 0.99        MJSW    = 0.2722644   CF      = 0
+PVTH0   = -2.126483E-3 PRDSW  = -24.2435379 PK2     = -4.788094E-4
+WKETA   = 1.430792E-3 LKETA   = -6.548592E-3 )
```


0.25µm BSIM3v3.1 PMOS Parameters

```
MODEL CMOSP PMOS (                           LEVEL   = 49
+VERSION = 3.1         TNOM    = 27          TOX     = 5.7E-9
+XJ      = 1E-7        NCH     = 4.1589E17   VTH0    = -0.6193382
+K1      = 0.5275326   K2      = 0.0281819   K3      = 0
+K3B     = 11.249555   W0      = 1E-6        NLX     = 1E-9
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 3.1920483   DVT1    = 0.4901788   DVT2    = -0.0295257
+U0      = 185.1288894 UA      = 3.40616E-9  UB      = 3.640498E-20
+UC      = -6.35238E-11 VSAT   = 1.975064E5  A0      = 0.4156696
+AGS     = 0.0702036   B0      = 3.111154E-6 B1      = 5E-6
+KETA    = 0.0253118   A1      = 2.421043E-4 A2      = 0.6754231
+RDSW    = 866.896668  PRWG    = 0.0362726   PRWB    = -0.293946
+WR      = 1           WINT    = 6.519911E-9 LINT    = 2.210804E-8
+XL      = 3E-8        XW      = 0           DWG     = -2.423118E-8
+DWB     = 3.052612E-8 VOFF    = -0.1161062  NFACTOR = 1.2546896
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 0.7241245   ETAB    = -0.3675267
+DSUB    = 1.1734643   PCLM    = 1.0837457   PDIBLC1 = 9.608442E-4
+PDIBLC2 = 0.0176785   PDIBLCB = -9.605935E-4 DROUT  = 0.0735541
+PSCBE1  = 1.579442E10 PSCBE2  = 6.707105E-9 PVAG    = 0.0409261
+DELTA   = 0.01        MOBMOD  = 1           PRT     = 0
+UTE     = -1.5        KT1     = -0.11       KT1L    = 0
+KT2     = 0.022       UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11    AT      = 3.3E4       WL      = 0
+WLN     = 1           WW      = 0           WWN     = 1
+WWL     = 0           LL      = 0           LLN     = 1
+LW      = 0           LWN     = 1           LWL     = 0
+CAPMOD  = 2           XPART   = 0.4         CGDO    = 5.11E-10
+CGSO    = 5.11E-10    CGBO    = 1E-11       CJ      = 1.882953E-3
+PB      = 0.99        MJ      = 0.4690946   CJSW    = 3.018356E-10
+PBSW    = 0.8137064   MJSW    = 0.3299497   CF      = 0
+PVTH0   = 5.268963E-3 PRDSW   = -2.2622317  PK2     = 3.952008E-3
+WKETA   = -7.69819E-3 LKETA   = -0.0119828  )
```

Adjustable Precision Analog Models – Table Lookup



- Objective

  Develop models having adjustable precision in ac and dc perfomrance using table lookup models.
- Advantages

  Usable at any level – device, circuit, or behavioral

  Quickly developed from experiment or process simulators

  Faster than analytical device models (BSIM)
- Disadvantages

  Requires approximately 10kbytes for a typical MOS model

  Can't be parameterized easily

Summary of MOSFET Models for Simulation

- Models are much improved for efficient computer simulation
- Output conductance model is greatly improved
- Poor results for narrow channel transistors
- Can have discontinuities at bin boundaries
- Fairly complex model, difficult to understand in detail

SEC. 3.10 – EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

Procedure for extracting short channel models:

1.) Extract the square-law model parameters for a transistor with length at least 10 times L_{min}.

2.) Using the values of K', V_T, λ, and γ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1+\theta(v_{GS}-V_T)]}\frac{W}{L}[v_{GS}-V_T]^2(1+\lambda v_{DS})$$

Adjust the values of K', V_T, and λ as needed.

EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

$$i_D = K\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_T)^2(1 + \lambda v_{DS}) \quad (1)$$

$$i_D = K\left(\frac{W_{\text{eff}}}{L_{\text{eff}}}\right)\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS}) \quad (2)$$

where

$$V_T = V_{T0} + \gamma\left[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\right] \quad (3)$$

Extraction of Model Parameters:

First assume that v_{DS} is chosen such that the λv_{DS} term in Eq. (2) is much less than one and v_{SB} is zero, so that $V_T = V_{T0}$.

Therefore, Eq. (2) simplifies to

$$i_D = K'\left(\frac{W_{\text{eff}}}{2L_{\text{eff}}}\right)(v_{GS} - V_{T0})^2 \tag{6}$$

This equation can be manipulated algebraically to obtain the following

$$i_D^{1/2} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} v_{GS} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{7}$$

which has the form

$$y = mx + b \tag{8}$$

This equation is easily recognized as the equation for a straight line with m as the slope and b as the y-intercept. Comparing Eq. (7) to Eq. (8) gives

$$y = i_D^{1/2} \tag{9}$$

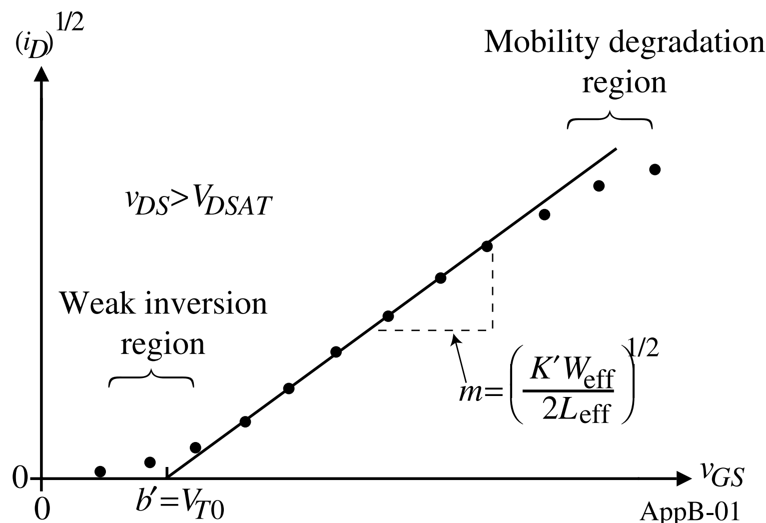
$$x = v_{GS} \tag{10}$$

$$m = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} \tag{11}$$

and

$$b = -\left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}}\right)^{1/2} V_{T0} \tag{12}$$

Illustration of K' and V_T Extraction



Comments:

- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than L_{min}

Example 3.10-1 – Extraction of K' and V_T Using Linear Regression

Given the following transistor data shown in Table 3.10-1 and linear regression formulas based on the form,

$$y = mx + b \tag{13}$$

and

$$m = \frac{\sum x_i y_i - (\sum x_i \sum y_i)/n}{\sum x_i^2 - (\sum x_i)^2/n} \tag{14}$$

determine V_{T0} and $K W/2L$. The data in Table B-1 also give $I_D^{1/2}$ as a function of V_{GS}.

Table 3.10-1 Data for Example 3.10-1

V_{GS} (V)	I_D (μA)	$\sqrt{I_D}$ (μA)$^{1/2}$	V_{SB} (V)
1.000	0.700	0.837	0.000
1.200	2.00	1.414	0.000
1.500	8.00	2.828	0.000
1.700	13.95	3.735	0.000
1.900	22.1	4.701	0.000

Example 3.10-1 – Continued

Solution

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

$$\text{Slope} = m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}}$$

Gives

$$m_1 = \frac{1.414 - 0.837}{0.2} = 2.885 \qquad m_2 = \frac{2.828 - 1.414}{0.3} = 4.713$$

$$m_3 = \frac{3.735 - 2.828}{0.2} = 4.535 \qquad m_4 = \frac{4.701 - 3.735}{0.2} = 4.830$$

These results indicate that the first (lowest value of V_{GS}) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

$$V_{T0} = 0.898 \text{ V} \qquad \text{and} \qquad \frac{K'W_{eff}}{2L_{eff}} = 21.92\ \mu\text{A/V}^2$$

Extraction of the Bulk-Threshold Parameter γ

Using the same techniques as before, the following equation

$$V_T = V_{T0} + \gamma\,[\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}\,]$$

is written in the linear form where

$$y = V_T \quad (18)$$

$$x = \sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|} \quad (19)$$

$$m = \gamma \quad (20)$$

$$b = V_{T0} \quad (21)$$

The term $2|\phi_F|$ is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for $2|\phi_F|$.

2.) Extract a value for γ.

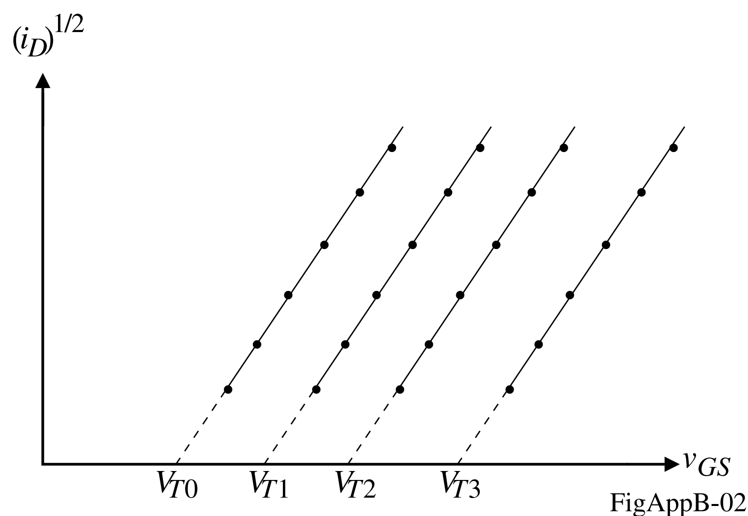
3.) Calculate N_{SUB} using the relationship, $\gamma = \dfrac{\sqrt{2\varepsilon_{si} q N_{SUB}}}{C_{ox}}$

4.) Calculate ϕ_F using the relationship, $\phi_F = -\dfrac{kT}{q}\ln\left(\dfrac{N_{SUB}}{n_i}\right)$

5.) Iterative procedures can be used to achieve the desired accuracy of γ and $2|\phi_F|$. Generally, an approximate value for $2|\phi_F|$ gives adequate results.

Illustration of the Procedure for Extracting γ

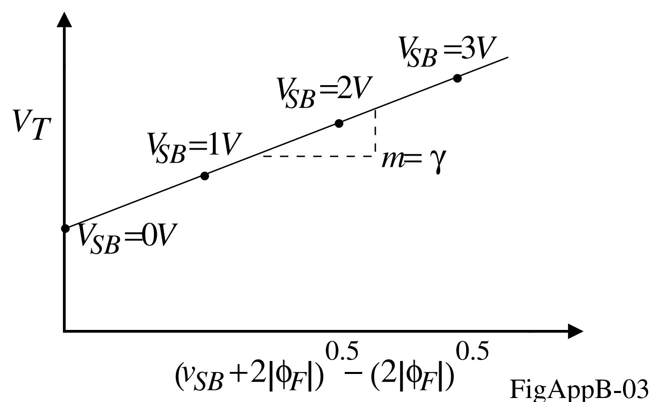
A plot of $\sqrt{i_D}$ versus v_{GS} for different values of v_{SB} used to determine γ is shown below.



By plotting V_T versus x of Eq. (19) one can measure the slope of the best fit line from which the parameter γ can be extracted. In order to do this, V_T must be determined at various values of v_{SB} using the technique previously described.

Illustration of the Procedure for Extracting γ - Continued

Each V_T determined above must be plotted against the v_{SB} term. The result is shown below. The slope m, measured from the best fit line, is the parameter γ.



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Example 3.10-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. B-1 and the following transistor data, determine the value of γ using linear regression techniques. Assume that $2|\phi_F|$ is 0.6 volts.

Table 3.10-2 Data for Example 3.10-2.

V_{SB} (V)	V_{GS} (V)	I_D (μA)
1.000	1.400	1.431
1.000	1.600	4.55
1.000	1.800	9.44
1.000	2.000	15.95
2.000	1.700	3.15
2.000	1.900	7.43
2.000	2.10	13.41
2.000	2.30	21.2

Solution

Table B-2 shows data for V_{SB} = 1 volt and V_{SB} = 2 volts. A quick check of the data in this table reveals that $\sqrt{I_D}$ versus V_{GS} is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. B-1, the following thresholds are determined: V_{T0} = 0.898 volts (from Ex. B-1), V_T = 1.143 volts (@V_{SB} = 1 V), and V_T = 1.322 V (@V_{SB} = 2 V). Table B-3 gives the value of V_T as a function of $[(2|\phi_F| + V_{SB})^{1/2} - (2|\phi_F|)^{1/2}]$ for the three values of V_{SB}.

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Example 3.10-2 - Continued

Table 3.10-3 Data for Example 3.10-2.

V_{SB} (V)	V_T (V)	$[\sqrt{2\lvert\phi_F\rvert + V_{SB}} - \sqrt{2\lvert\phi_F\rvert}]$ ($V^{1/2}$)
0.000	0.898	0.000
1.000	1.143	0.490
2.000	1.322	0.838

With these data, linear regression must be performed on the data of V_T versus $[(2|\phi_F| + V_{SB})^{0.5} - (2|\phi_F|)^{0.5}]$. The regression parameters of Eq. (13) are

$\Sigma x_i y_i = 1.668$

$\Sigma x_i y_i = 4.466$

$\Sigma x_i^2 = 0.9423$

$(\Sigma x_i)^2 = 1.764$

These values give $m = 0.506 = \gamma$.

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Extraction of the Channel Length Modulation Parameter, λ

The channel length modulation parameter λ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (2) is rewritten as

$$i_D = i'_D = \lambda' v_{DS} + i'_D \quad (22)$$

which is in the familiar linear form where

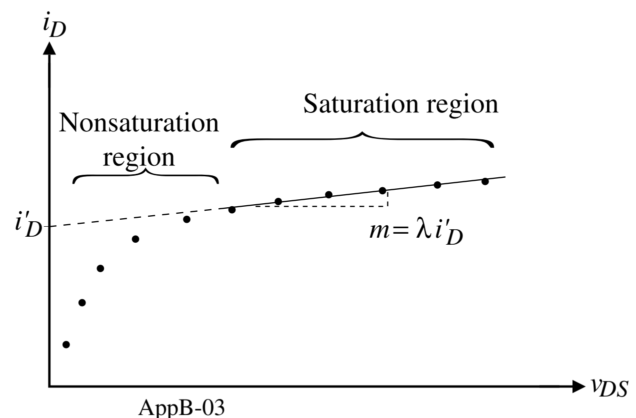
$y = i_D$ (Eq. (2)) 23)

$x = v_{DS}$ (24)

$m = \lambda i'_D$ (25)

$b = i'_D$ (Eq. (2) with $\lambda = 0$) (26)

By plotting i_D versus v_{DS}, measuring the slope of the data in the saturation region, and dividing that value by the y-intercept, λ can be determined. The procedure is illustrated in the figure shown.



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Example 3.10-3 – Extraction of the Channel Length Modulation Parameter

Given the data of I_D versus V_{DS} in Table 10.3-4, determine the parameter λ.

Table 10.3-4 Data for Example 3.10-3.

I_D (μA)	39.2	68.2	86.8	94.2	95.7	97.2	98.8	100.3
V_{DS} (V)	0.500	1.000	1.500	2.000	2.50	3.00	3.50	4.00

Solution

We note that the data of Table 3.10-4 covers both the saturation and nonsaturation regions of operation. A quick check shows that saturation is reached near V_{DS} = 2.0 V. To calculate λ, we shall use the data for V_{DS} greater than or equal to 2.5 V. The parameters of the linear regression are

$x_i y_i = 1277.85$ $\sum x_i \sum y_i = 5096.00$

$\sum x^2{}_i = 43.5$ $(\sum x_i)^2 = 169$

These values result in $m = \lambda I'_D = 3.08$ and $b = I'_D = 88$, giving $\lambda = 0.035\ \text{V}^{-1}$.

The slope in the saturation region is typically very small, making it necessary to be careful that two data points taken with low resolution are not subtracted (to obtain the slope) resulting in a number that is of the same order of magnitude as the resolution of the data point measured. If this occurs, then the value obtained will have significant and unacceptable error.

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EXTRACTION OF THE SIMPLE MODEL FOR SHORT CHANNEL MOSFETS

Extraction for Short Channel MOSFETS

The model proposed is the following one which is the square-law model modified by the velocity saturation influence.

$$i_D = \frac{K'}{2[1 + \theta(v_{GS}-V_T)]} \frac{W}{L} [\, v_{GS} - V_T]^2 (1+\lambda v_{DS})$$

Using the values of K', V_T, λ, and γ extracted previously, use an appropriate extraction procedure to find the value of θ adjusting the values of K', V_T, and λ as needed.

Comments:

- We will assume that the bulk will be connected to the source or the standard relationship between V_T and V_{BS} can be used.
- The saturation voltage is still given by

$$V_{DS}(\text{sat}) = V_{GS} - V_T$$

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Example of a Genetic Algorithm†

1.) To use this algorithm or any other, use the simulator and an appropriate short-channel model (BSIM3) to generate a set of data for the transconductance (i_D vs. v_{GS}) and output characteristics (i_D vs. v_{DS}) of the transistor with the desired W and L values.

2.) The best fit to the data is found using a genetic algorithm. The constraints on the parameters are obtained from experience with prior transitor parameters and are:

$$10E\text{-}6 < \beta < 610E\text{-}6, \quad 1 < \theta < 5, \quad 0 < V_T < 1, \quad \text{and } 0 < \lambda < 0.5$$

3,) The details of the genetic algorithm are:

Gene structure is $A = [\beta, \theta, V_T, \text{fitness}]$. A mutation was done by varying all four parameters. A weighted sum of the least square errors of the data curves was used as the error function. The fitness of a gene was chosen as 1/error.

4.) The results for an extraction run of 8000 iterations for an NMOS transistor is shown below.

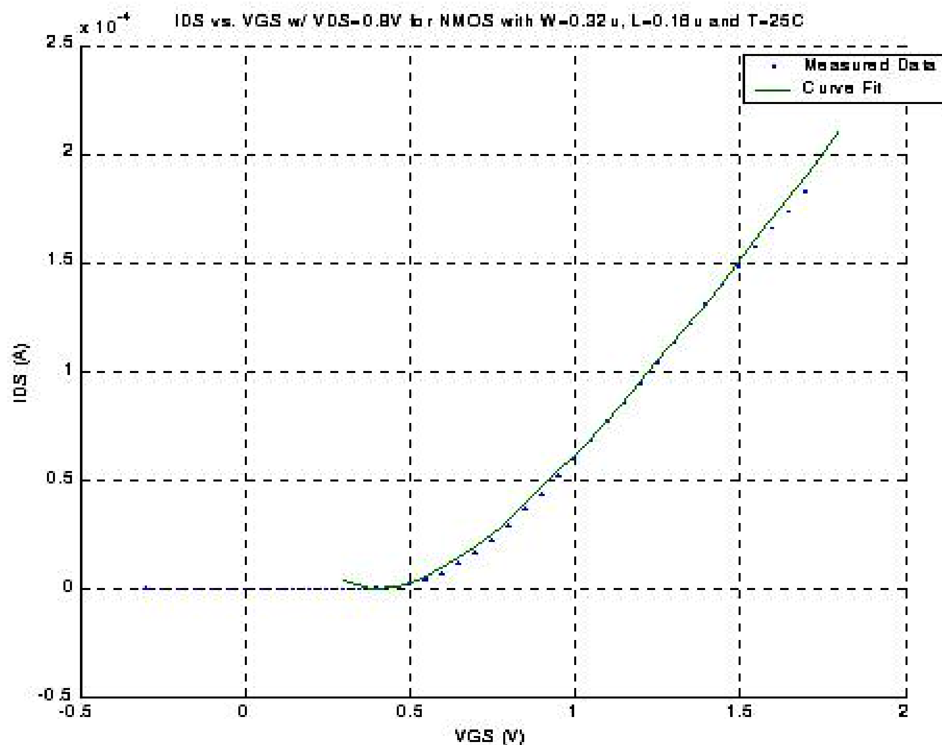
β(A/V^2)	θ	V_T(V)	λ(V^{-1})
294.1×10^{-6}	1.4564	0.4190	0.1437

5.) The results for a NMOS and PMOS transistor are shown on the following pages.

† Anurag Kaplish, "Parameter Optimization of Deep Submicron MOSFETS Using a Genetic Algorithm," May 4, 2000, Special Project Report, School of ECE, Georgia Tech.

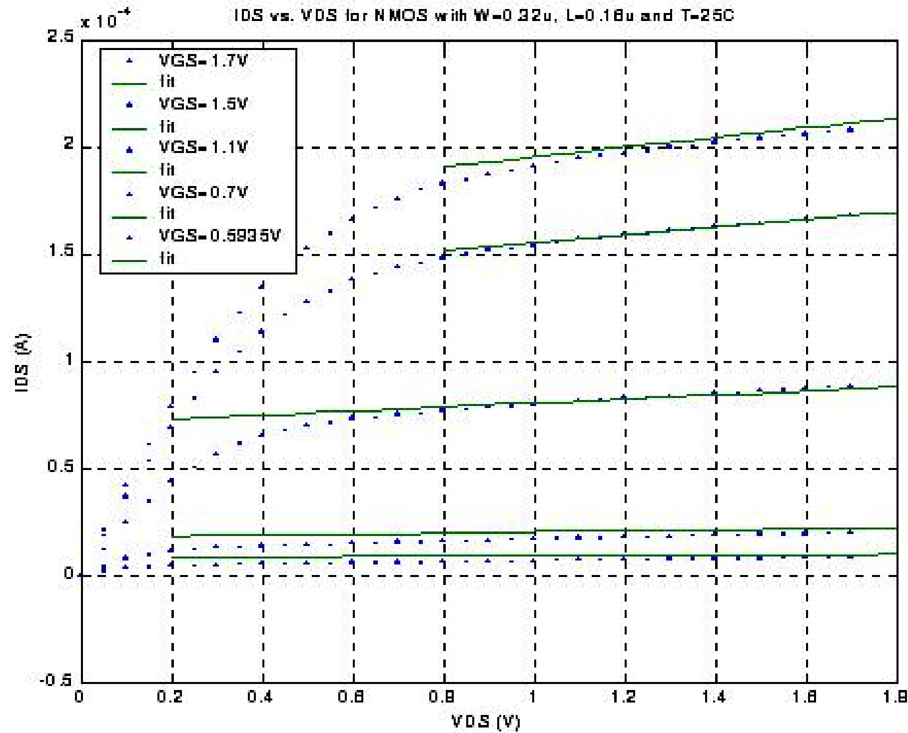
Extraction Results for an NMOS Transistor with W = 0.32µm and L = 0.18µm

Transconductance:



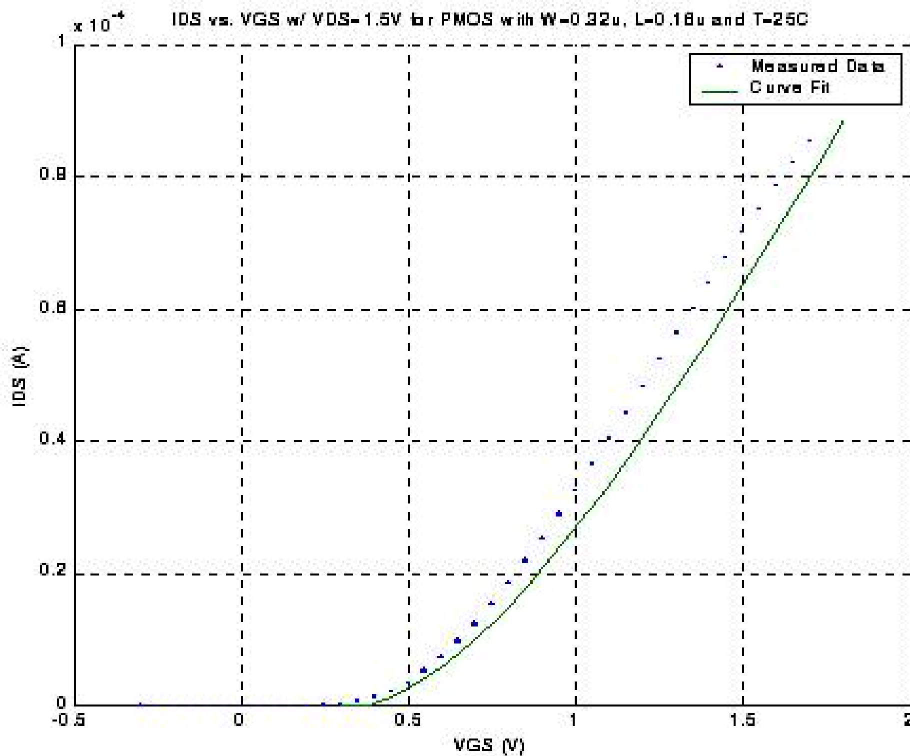
Extraction Results for an NMOS Transistor with W = 0.32μm and L = 0.18μm

Output:



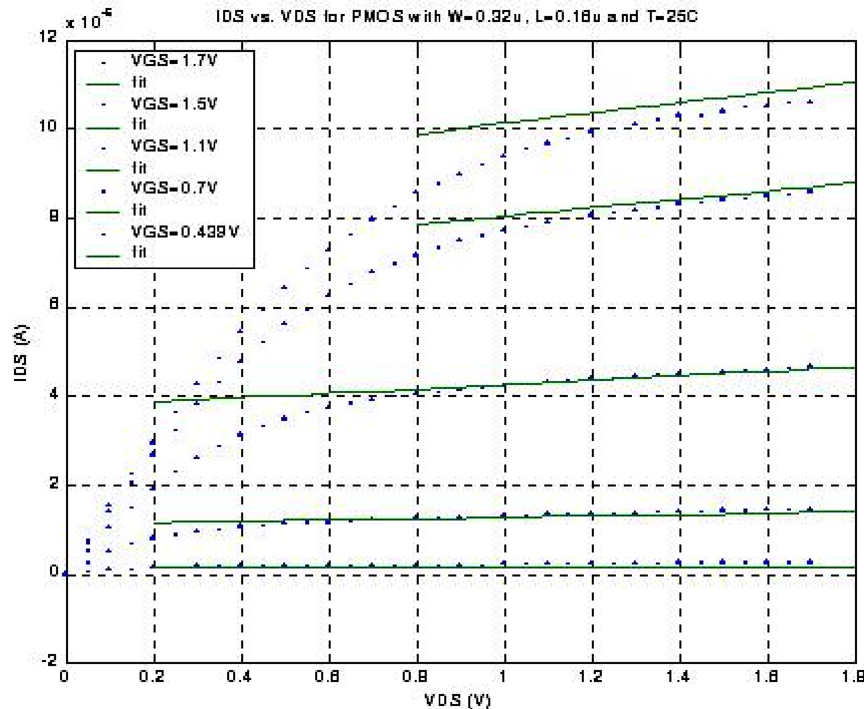
Extraction Results for an PMOS Transistor with W = 0.32μm and L = 0.18μm

Transconductance:



Extraction Results for an PMOS Transistor with W = 0.32µm and L = 0.18µm

Output:



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SEC. 3.11 - SUMMARY

- Model philosophy for analog IC design
  Use simple models for design and sophisticated models for verification
- Models have several parts
  Large signal static (dc variables)
  Small signal static (midband gains, resistances)
  Small signal dynamic (frequency response, noise)
  Large signal dynamic (slew rate)
- In addition models may include:
  Temperature
  Noise
  Process variations (Monte Carlo methods)
- Computer models
  Must be numerically efficient
  Quickly derived from new technology
- Analog Design “Tricks”
  Stay away from minimum channel length if possible
  - Larger $r_{ds} \rightarrow$ larger gains
  - Better agreement
  Don’t use the computer models for design, rather verification of design

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